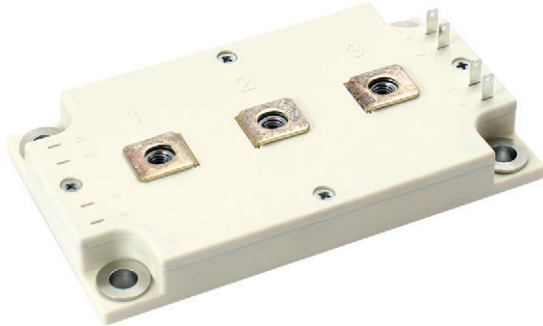


Dual INT-A-PAK Low Profile “Half Bridge” (Standard Speed IGBT), 400 A



Dual INT-A-PAK Low Profile

FEATURES

- TrenchStop IGBT technology
- Standard: optimized for hard switching speed
- Low $V_{CE(on)}$
- Square RBSOA
- Gen 4 FRED Pt[®] dices technology
- Industry standard package
- Al₂O₃ DBC
- UL approved file E78996
- Designed for industrial level
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT

PRIMARY CHARACTERISTICS	
V_{CES}	600 V
I_C DC at $T_C = 114\text{ }^\circ\text{C}$	400 A
$V_{CE(on)}$ (typical) at 400 A, 25 °C	1.14 V
Speed	DC to 1 kHz
Package	Dual INT-A-PAK low profile
Circuit configuration	Half bridge

BENEFITS

- Increased operating efficiency
- Performance optimized as output inverter stage for TIG welding machines
- Direct mounting on heatsink
- Very low junction to case thermal resistance

ABSOLUTE MAXIMUM RATINGS				
PARAMETER	SYMBOL	TEST CONDITIONS	MAX.	UNITS
Collector to emitter voltage	V_{CES}		600	V
Continuous collector current	I_C ⁽¹⁾	$T_C = 25\text{ }^\circ\text{C}$	711	A
		$T_C = 80\text{ }^\circ\text{C}$	532	
Pulsed collector current	I_{CM}	$T_C = 175\text{ }^\circ\text{C}$, $t_p = 6\text{ ms}$, $V_{GE} = 15\text{ V}$	1100	
Clamped inductive load current	I_{LM}		900	
Diode continuous forward current	I_F	$T_C = 25\text{ }^\circ\text{C}$	260	
		$T_C = 80\text{ }^\circ\text{C}$	192	
Gate to emitter voltage	V_{GE}		± 20	V
Maximum power dissipation (IGBT)	P_D	$T_C = 25\text{ }^\circ\text{C}$	1364	W
		$T_C = 80\text{ }^\circ\text{C}$	864	
Maximum power dissipation (Diode)	P_D	$T_C = 25\text{ }^\circ\text{C}$	441	W
		$T_C = 80\text{ }^\circ\text{C}$	279	
RMS isolation voltage	V_{ISOL}	Any terminal to case (V_{RMS} $t = 1\text{ s}$, $T_J = 25\text{ }^\circ\text{C}$)	3500	V

Note

⁽¹⁾ Maximum continuous collector current must be limited to 500 A to do not exceed the maximum temperature of terminals



ELECTRICAL SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise specified)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Collector to emitter breakdown voltage	$V_{BR(CES)}$	$V_{GE} = 0\text{ V}, I_C = 1.2\text{ mA}$	600	-	-	V
Collector to emitter voltage	$V_{CE(on)}$	$V_{GE} = 15\text{ V}, I_C = 400\text{ A}$	-	1.14	1.40	
		$V_{GE} = 15\text{ V}, I_C = 400\text{ A}, T_J = 125\text{ }^\circ\text{C}$	-	1.13	-	
Gate threshold voltage	$V_{GE(th)}$	$V_{CE} = V_{GE}, I_C = 6\text{ mA}$	3.8	4.7	6.3	mA
Collector to emitter leakage current	I_{CES}	$V_{GE} = 0\text{ V}, V_{CE} = 600\text{ V}$ $V_{GE} = 0\text{ V}, V_{CE} = 600\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	0.002	0.3	
Diode forward voltage drop	V_{FM}	$I_{FM} = 400\text{ A}$	-	1.65	2.26	V
		$I_{FM} = 400\text{ A}, T_J = 125\text{ }^\circ\text{C}$	-	1.58	-	
Gate to emitter leakage current	I_{GES}	$V_{GE} = \pm 20\text{ V}$	-	-	± 200	nA

SWITCHING CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise specified)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Total gate charge (turn-on)	Q_g	$I_C = 75\text{ A}, V_{CC} = 520\text{ V}, V_{GE} = 15\text{ V}$	-	2791	-	nC
Gate-to-emitter charge (turn-on)	Q_{ge}		-	428	-	
Gate-to-collector charge (turn-on)	Q_{gc}		-	711	-	
Turn-on switching loss	E_{on}	$I_C = 400\text{ A}, V_{CC} = 300\text{ V}, V_{GE} = 15\text{ V}, R_g = 1.5\text{ }\Omega, L = 500\text{ }\mu\text{H}, T_J = 25\text{ }^\circ\text{C}$	-	2.5	-	mJ
Turn-off switching loss	E_{off}		-	20.7	-	
Total switching loss	E_{tot}		-	23.2	-	
Turn-on switching loss	E_{on}		-	2.2	-	
Turn-off switching loss	E_{off}		-	27.6	-	
Total switching loss	E_{tot}		-	29.8	-	
Turn-on delay time	$t_{d(on)}$	$I_C = 400\text{ A}, V_{CC} = 300\text{ V}, V_{GE} = 15\text{ V}, R_g = 1.5\text{ }\Omega, L = 500\text{ }\mu\text{H}, T_J = 125\text{ }^\circ\text{C}$	-	24	-	ns
Rise time	t_r		-	104	-	
Turn-off delay time	$t_{d(off)}$		-	506	-	
Fall time	t_f		-	167	-	
Reverse bias safe operating area	RBSOA	$T_J = 175\text{ }^\circ\text{C}, I_C = 900\text{ A}, V_{CC} = 300\text{ V}, V_p = 600\text{ V}, R_g = 27\text{ }\Omega, V_{GE} = 15\text{ V to } -5\text{ V}, L = 500\text{ }\mu\text{H}$	Fullsquare			
Diode reverse recovery time	t_{rr}	$I_F = 50\text{ A}, di_F/dt = 500\text{ A}/\mu\text{s}, V_{CC} = 200\text{ V}, T_J = 25\text{ }^\circ\text{C}$	-	152	-	ns
Diode peak reverse current	I_{rr}		-	24	-	A
Diode recovery charge	Q_{rr}		-	1.82	-	μC
Diode reverse recovery time	t_{rr}	$I_F = 50\text{ A}, di_F/dt = 500\text{ A}/\mu\text{s}, V_{CC} = 200\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	200	-	ns
Diode peak reverse current	I_{rr}		-	39	-	A
Diode recovery charge	Q_{rr}		-	3.94	-	μC

THERMAL AND MECHANICAL SPECIFICATIONS						
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	
Operating junction and storage temperature range	T_J, T_{Stg}	-40	-	175	$^\circ\text{C}$	
Junction to case per leg	IGBT	-	-	0.11	$^\circ\text{C}/\text{W}$	
	Diode	-	-	0.34		
Case to sink per module	R_{thCS}	-	0.05	-		
Mounting torque	case to heatsink: M6 screw	4	-	6	Nm	
	case to terminal 1, 2, 3: M5 screw	2	-	5		
Weight		-	270	-	g	

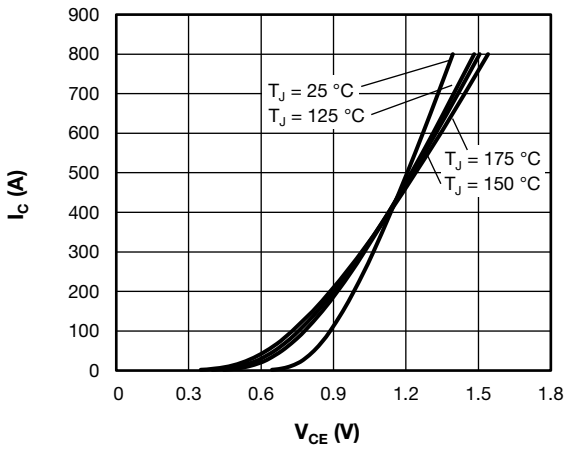


Fig. 1 - Typical Q1 to Q2 IGBT Output Characteristics, $V_{GE} = 15\text{ V}$

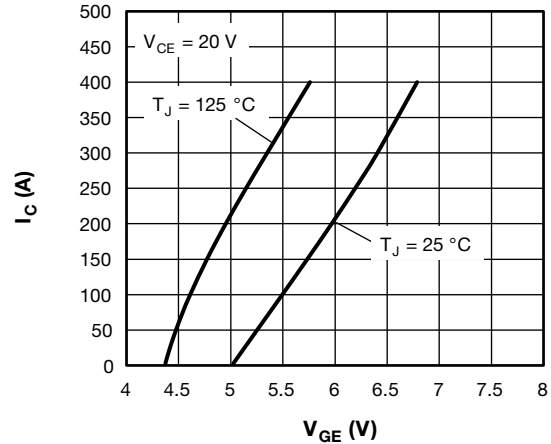


Fig. 4 - Typical Q1 to Q2 IGBT Transfer Characteristics

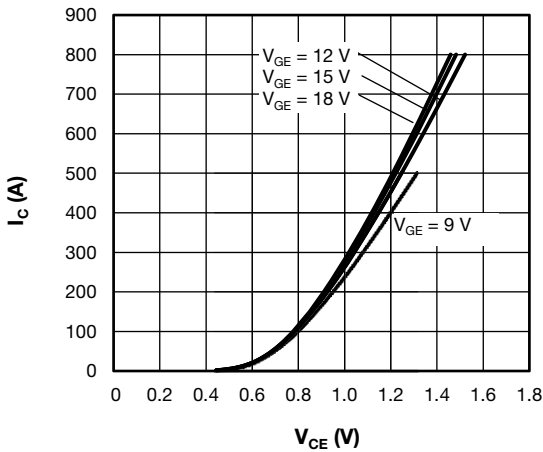


Fig. 2 - Typical Q1 to Q2 IGBT Output Characteristics, $T_J = 125\text{ °C}$

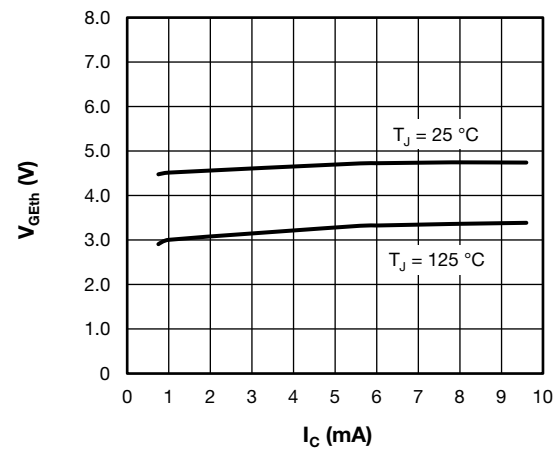


Fig. 5 - Typical Q1 to Q2 IGBT Gate Threshold Voltage

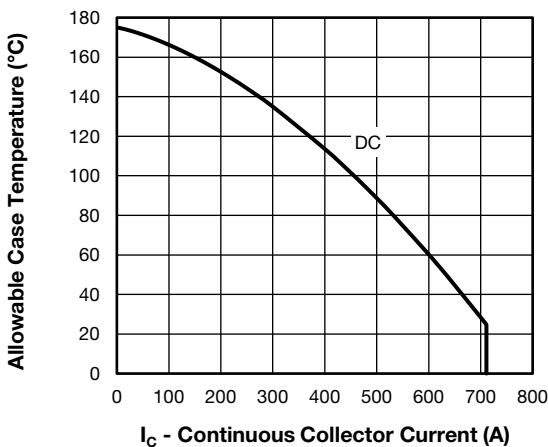


Fig. 3 - Maximum Q1 to Q2 IGBT Continuous Collector Current vs. Case Temperature

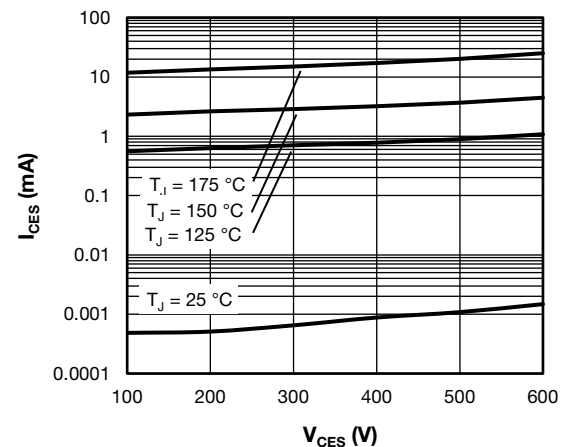


Fig. 6 - Typical Q1 to Q2 IGBT Zero Gate Voltage Collector Current

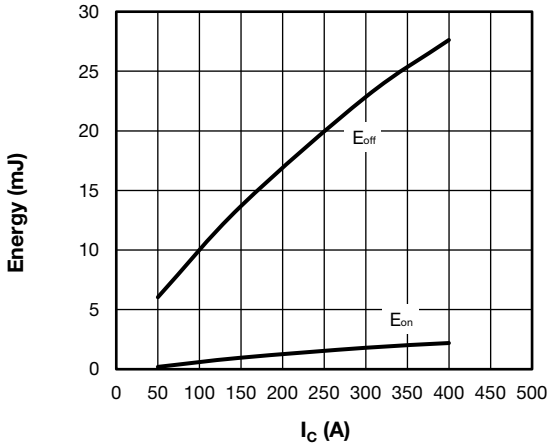


Fig. 7 - Typical Q1 to Q2 IGBT
Energy Loss vs. I_C (with D1 to D2 Antiparallel Diode)
 $T_J = 125^\circ\text{C}$, $V_{CC} = 300\text{ V}$, $R_g = 1.5\ \Omega$, $V_{GE} = +15\text{ V}/-15\text{ V}$, $L = 500\ \mu\text{H}$

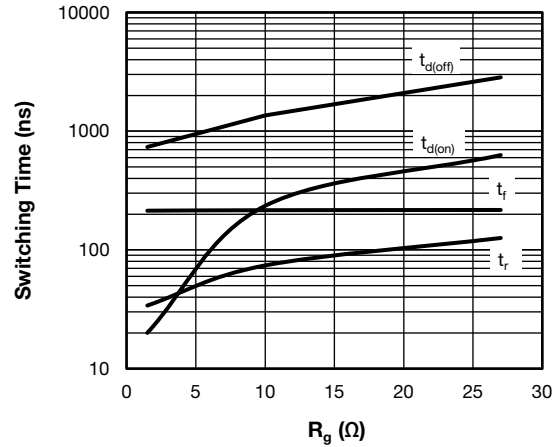


Fig. 10 - Typical Q1 to Q2 IGBT
Switching Time vs. R_g (with D1 to D2 Antiparallel Diode)
 $T_J = 125^\circ\text{C}$, $V_{CC} = 300\text{ V}$, $I_C = 400\text{ A}$, $V_{GE} = +15\text{ V}/-15\text{ V}$, $L = 500\ \mu\text{H}$

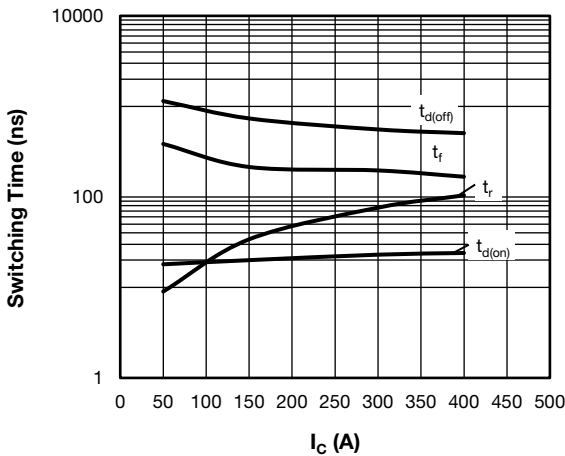


Fig. 8 - Typical Q1 to Q2 IGBT
Switching Time vs. I_C (with D1 to D2 Antiparallel Diode)

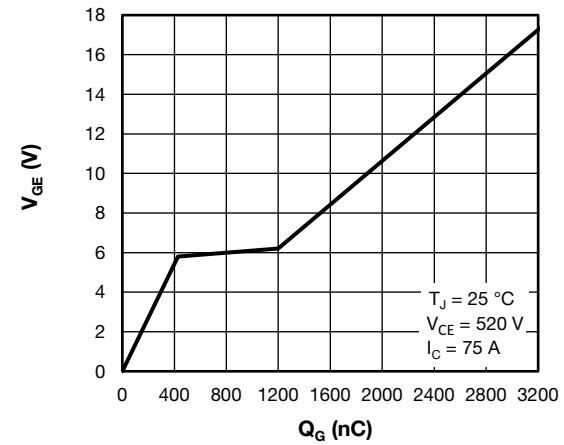


Fig. 11 - Typical Q1 to Q2 IGBT
Gate Charge vs. Gate to Emitter Voltage

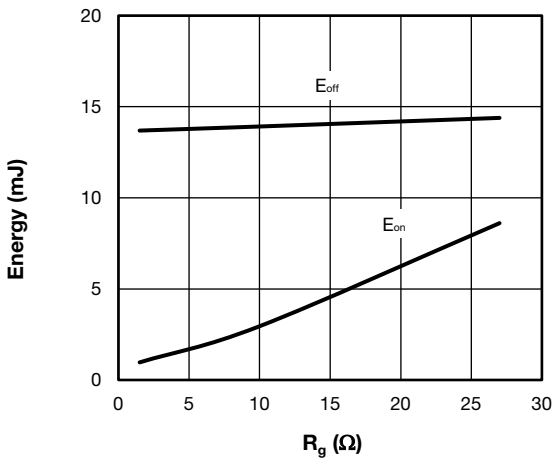


Fig. 9 - Typical Q1 to Q2 IGBT
Energy Loss vs. R_g (with D1 to D2 Antiparallel Diode)

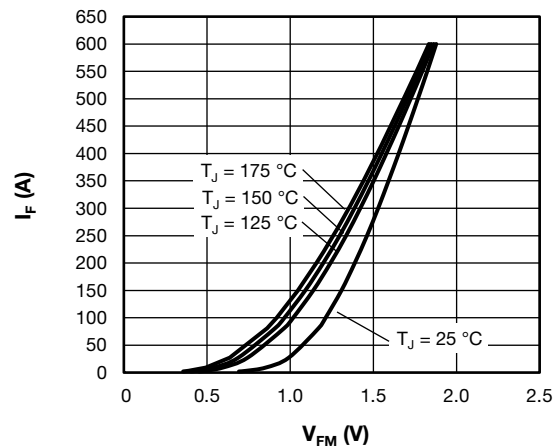


Fig. 12 - Typical D1 to D2 Antiparallel Diode
Forward Characteristics

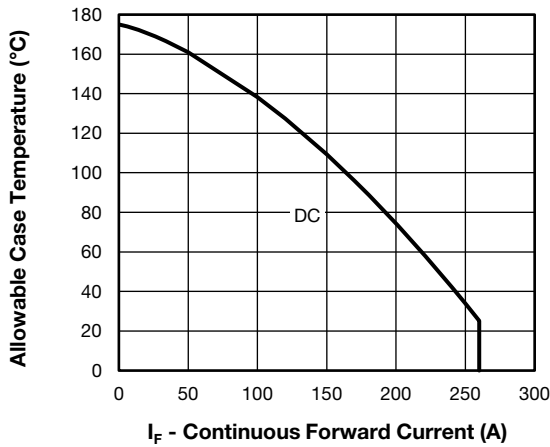


Fig. 13 - Maximum D1 to D2 Antiparallel Diode Continuous Forward Current vs. Case Temperature

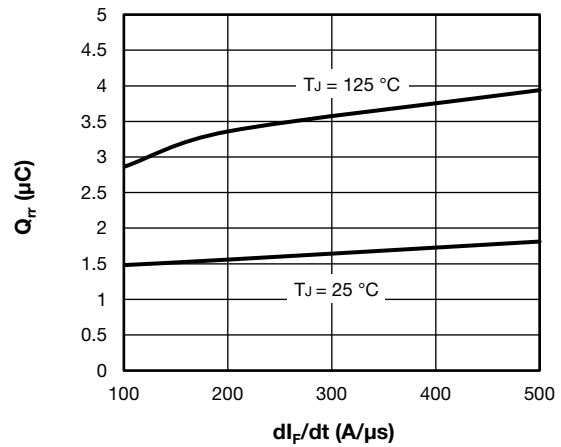


Fig. 16 - Typical D1 to D2 Antiparallel Diode Reverse Recovery Charge vs. di_F/dt , $V_{rr} = 200$ V, $I_F = 50$ A

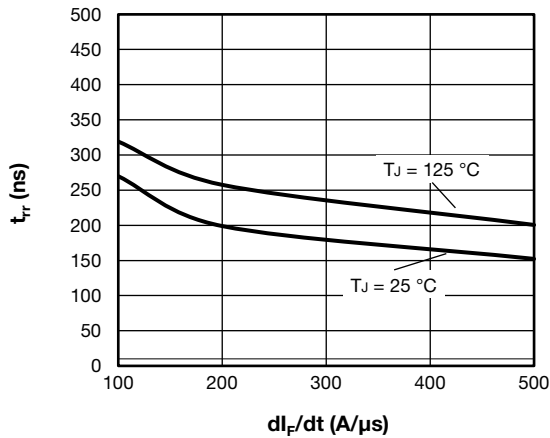


Fig. 14 - Typical D1 to D2 Antiparallel Diode Reverse Recovery Time vs. di_F/dt

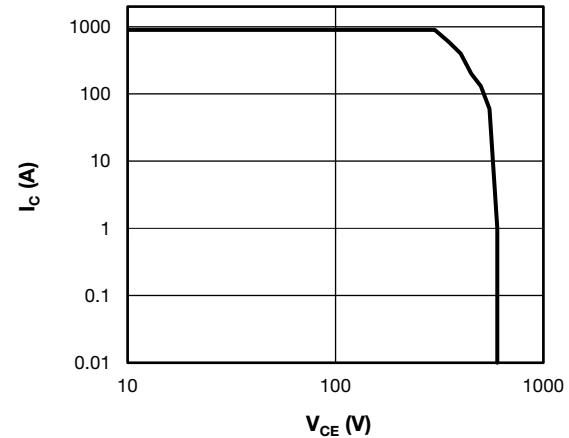


Fig. 17 - Q1 to Q2 IGBT Reverse BIAS SOA
 $T_J = 175$ °C, $I_C = 900$ A, $R_g = 27\Omega$, $V_{GE} = +15$ V / -5 V, $V_{CC} = 300$ V, $V_p = 600$ V

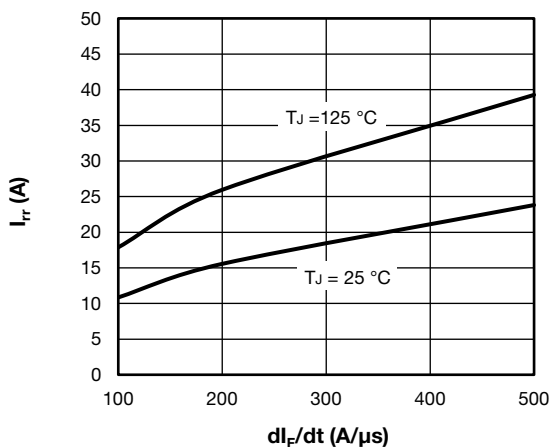


Fig. 15 - Typical D1 to D2 Antiparallel Diode Reverse Recovery Current vs. di_F/dt , $V_{rr} = 200$ V, $I_F = 50$ A

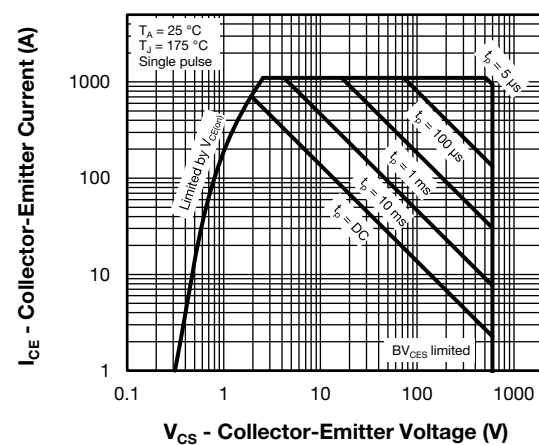


Fig. 18 - Q1 to Q2 IGBT Safe Operating Area

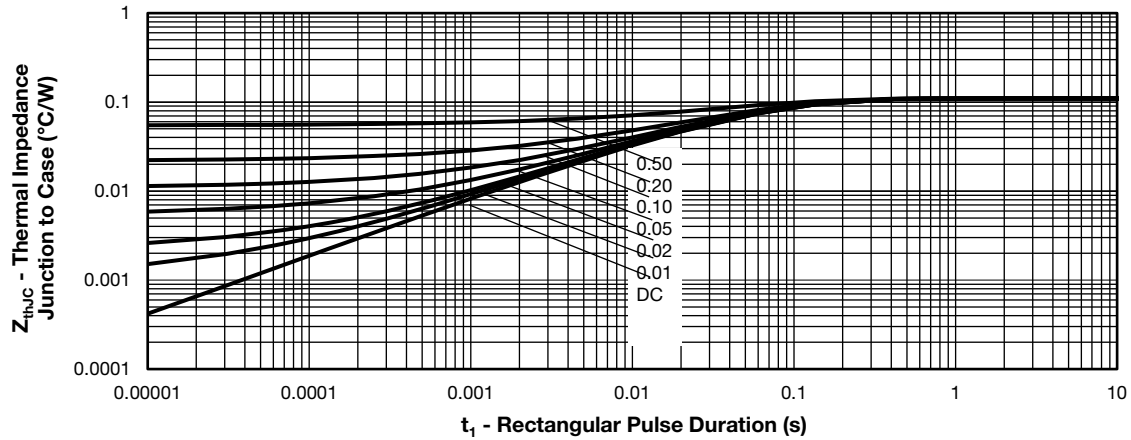


Fig. 19 - Maximum Thermal Impedance Z_{thJC} Characteristics - (Q1 to Q2 IGBT)

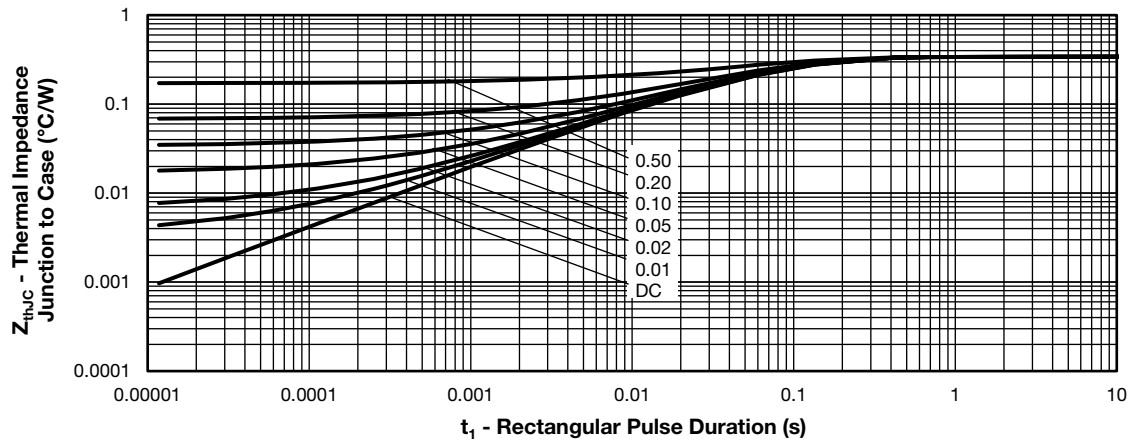


Fig. 20 - Maximum Thermal Impedance Z_{thJC} Characteristics - (D1 to D2 Antiparallel Diode)

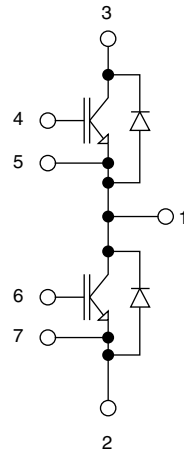
ORDERING INFORMATION TABLE

Device code	G	T	400	T	D	60	S
	①	②	③	④	⑤	⑥	⑦
	①	②	③	④	⑤	⑥	⑦
	①	②	③	④	⑤	⑥	⑦
	①	②	③	④	⑤	⑥	⑦
	①	②	③	④	⑤	⑥	⑦
	①	②	③	④	⑤	⑥	⑦
	①	②	③	④	⑤	⑥	⑦

- ① - Insulated gate bipolar transistor (IGBT)
- ② - T = Trench IGBT technology
- ③ - Current rating (400 = 400 A)
- ④ - Circuit configuration (T = half-bridge)
- ⑤ - Package indicator (D = dual INT-A-PAK low profile)
- ⑥ - Voltage rating (60 = 600 V)
- ⑦ - Speed / type (S = standard speed IGBT)



CIRCUIT CONFIGURATION

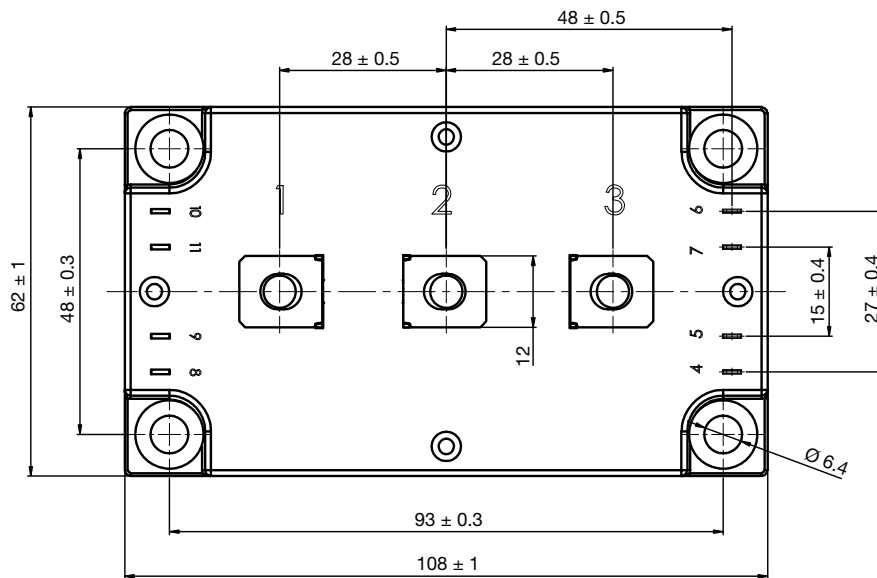
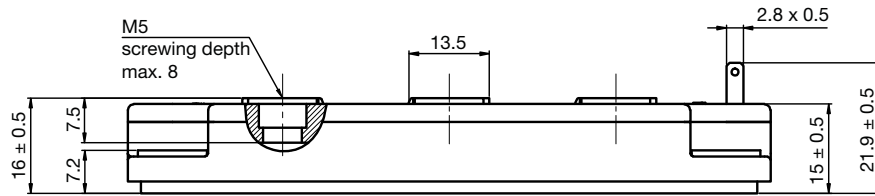


LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95435



Dual INT-A-PAK Low Profile

DIMENSIONS in millimeters





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