Photocouplers Infrared LED & Photo IC

TLP2210

1. Applications

- Programmable Logic Controllers (PLCs)
- Solar Micro-Inverters
- I/O Interface Boards

2. General

The TLP2210 consists of a high-output infrared LED coupled with a high-speed photodetectors. It is housed in a thin SO8L package of 2.35 mm (max). The SO8L package keeps 5000 Vrms isolation voltage and compliant with international safety standards for reinforced insulation. It has two circuits built into a single SO8L package, which contributes to reduce the mounting area.

This product guarantees operation at up to 125 ℃ and on supplies from 2.7 V to 5.5 V. The low supply current (I_{DDL}/I_{DDH}) of 0.6 mA, and the low threshold input current (I_{FLH}) of 1.3 mA (T_a = 125 ℃) provides energy saving of sets, and enables TLP2210 to be driven from a microcomputer directly.

The TLP2210 has an internal Faraday shield that provides a guaranteed common-mode transient immunity of ±25 kV/μs.

3. Features

(1) Buffer logic type (totem pole output)

(2) Package: SO8L(LF4)

(3) Operating temperature: -40 to 125 ℃

(4) Supply voltage: 2.7 to 5.5 V

(5) Data transfer rate: 5 Mbps (typ.)

(6) Threshold input current: 1.3 mA (max)

(7) Supply current: 0.6 mA (max)

(8) Common-mode transient immunity: ±25 kV/μs (min)

(9) Isolation voltage: 5000 Vrms (min)

(10) Safety standards

UL-recognized: UL 1577, File No.E67349

cUL-recognized: CSA Component Acceptance Service No.5A File No.E67349

VDE-approved: EN 60747-5-5, EN 62368-1 **(Note 1)**

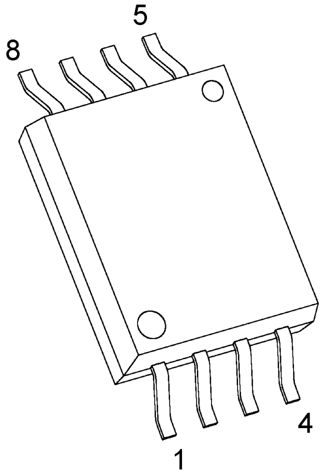
CQC-approved: GB4943.1, GB8898 Japan Factory (Pending)

Note 1: When a VDE approved type is needed, please designate the **Option (D4)**.

Start of commercial production

2020-01

4. Packaging and Pin Assignment



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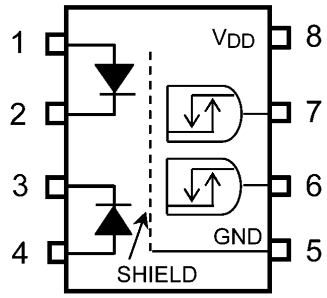
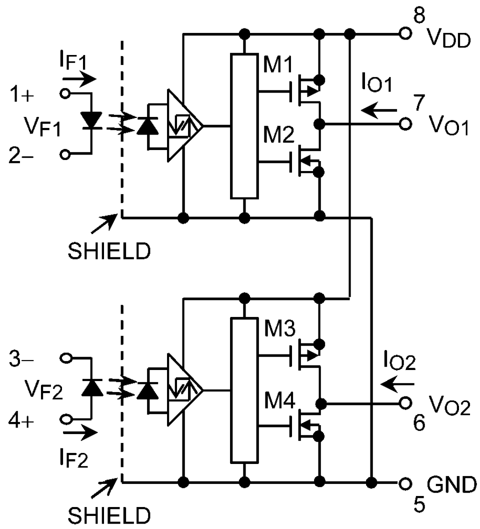


1: Anode 1
2: Cathode 1
3: Cathode 2
4: Anode 2
5: GND
6: V_O 2 (output 2)
7: V_O 1 (output 1)
8: V_{DD}

5. Internal Circuit (Note)



Note: A 0.1-μF bypass capacitor must be connected between pin 8 and pin 5.

6. Principle of Operation

6.1. Truth Table

Input	LED1 (2)	M1 (3)	M2 (4)	Output 1 (2)
H	ON	ON	OFF	H
L	OFF	OFF	ON	L

6.2. Mechanical Parameters

Characteristics	Min	Unit
Creepage distances	8.0	mm
Clearance	8.0	
Internal isolation thickness	0.4	

7. Absolute Maximum Ratings (Note) (Unless otherwise specified, T_a = 25 °C)

	Characteristics		Symbol	Note	Rating	Unit
LED	Input forward current		I_F	(Note 1)	8	mA
	Input forward current derating	($T_a \geq$ 110 °C)	$\Delta I_F/\Delta T_a$	(Note 1)	-0.32	mA/°C
	Input forward current (pulsed)		I_{FP}	(Note 1), (Note 2)	16	mA
	Input forward current derating (pulsed)	($T_a \geq$ 110 °C)	$\Delta I_{FP}/\Delta T_a$	(Note 1)	-0.64	mA/°C
	Peak transient input forward current		I_{FPT}	(Note 1), (Note 3)	1	A
	Peak transient input forward current derating	($T_a \geq$ 110 °C)	$\Delta I_{FPT}/\Delta T_a$	(Note 1)	-40	mA/°C
	Input power dissipation		P_D	(Note 1)	20	mW
	Input power dissipation derating	($T_a \geq$ 110 °C)	$\Delta P_D/\Delta T_a$	(Note 1)	-0.5	mW/°C
	Input reverse voltage		V_R	(Note 1)	5	V
Detector	Output current		I_O	(Note 1)	10	mA
	Output voltage		V_O	(Note 1)	-0.5 to 6	V
	Supply voltage		V_{DD}		-0.5 to 6	
	Output power dissipation		P_O	(Note 1)	20	mW
	Output power dissipation derating	($T_a \geq$ 110 °C)	$\Delta P_O/\Delta T_a$	(Note 1)	-0.5	mW/°C
Common	Operating temperature		T_{opr}		-40 to 125	°C
	Storage temperature		T_{stg}		-55 to 125	
	Lead soldering temperature	(10 s)	T_{sol}		260	
	Isolation voltage	(AC, 60 s, R.H. ≤ 60 %)	BV_S	(Note 4)	5000	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Each channel

Note 2: Pulse width (PW) ≤ 1 ms, duty = 50 %

Note 3: Pulse width (PW) ≤ 1 μs, 300 pps

Note 4: This device is considered as a two-terminal device: Pins 1, 2, 3 and 4 are shorted together, and pins 5, 6, 7 and 8 are shorted together.

8. Recommended Operating Conditions (Note)

Characteristics	Symbol	Note	Min	Typ.	Max	Unit
Input on-state current	$I_{F(ON)}$	(Note 1), (Note 2)	2	—	6	mA
Input off-state voltage	$V_{F(OFF)}$	(Note 1)	0	—	0.8	V
Supply voltage	V_{DD}	(Note 3)	2.7	3.3 / 5.0	5.5	
Operating temperature	T_{opr}	(Note 3)	-40	—	125	°C

Note: The recommended operating conditions are given as a design guide necessary to obtain the intended performance of the device. Each parameter is an independent value. When creating a system design using this device, the electrical characteristics specified in this data sheet should also be considered.

Note: A ceramic capacitor (0.1 μF) should be connected between pin 8 and pin 5 to stabilize the operation of a high-gain linear amplifier. Otherwise, this photocoupler may not switch properly. The bypass capacitor should be placed within 1 cm of each pin.

Note 1: Each channel

Note 2: The rise and fall times of the input on-current should be less than 0.5 μs.

Note 3: Denotes the operating range, not the recommended operating condition.

9. Electrical Characteristics (Note) (Unless otherwise specified, T_a = -40 to 125 °C, V_{DD} = 2.7 to 5.5 V)

Characteristics	Symbol	Note	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input forward voltage	V_F	(Note 1)		I_F = 2 mA	1.2	—	1.9	V
				I_F = 2 mA, T_a = 25 °C	1.4	1.53	1.7	
Input forward voltage temperature coefficient	$\Delta V_F/\Delta T_a$	(Note 1)		I_F = 2 mA	—	-1.58	—	mV/°C
Input reverse current	I_R	(Note 1)		V_R = 5 V, T_a = 25 °C	—	—	10	μA
Input capacitance	C_t	(Note 1)		V = 0 V, f = 1 MHz , T_a = 25 °C	—	22	—	pF
Low-level output voltage	V_{OL}	(Note 1)	Fig. 12.1.1	V_F = 0.8 V, I_O = 20 μA	—	0.0008	0.1	V
	V_{OL}			V_F = 0.8 V, I_O = 3.2 mA	—	0.13	0.4	
High-level output voltage	V_{OH}	(Note 1)	Fig. 12.1.2	I_F = 2 mA, I_O = -20 μA	V_{DD} - 0.1	V_{DD} - 0.002	—	
	V_{OH}			I_F = 2 mA, I_O = -3.2 mA	V_{DD} - 1.0	V_{DD} - 0.25	—	
Low-level supply current	I_{DDL}		Fig. 12.1.3	I_{F1} = I_{F2} = 0 mA	—	0.4	0.6	mA
High-level supply current	I_{DDH}		Fig. 12.1.4	I_{F1} = I_{F2} = 2 mA	—	0.41	0.6	
Threshold input current (L/H)	I_{FLH}	(Note 1)		I_O = -3.2 mA, V_O > 1.7 V	—	0.58	1.3	

Note: All typical values are at V_{DD} = 5 V, T_a = 25 °C, unless otherwise noted.
Note 1: Each channel

10. Isolation Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Note	Test Condition	Min	Typ.	Max	Unit
Total capacitance (input to output)	C_S	(Note 1)	V = 0 V, f = 1 MHz	—	0.8	—	pF
Isolation resistance	R_S	(Note 1)	V = 500 V, R.H. ≤ 60 %	10^{12}	10^{14}	—	Ω
Isolation voltage	BV_S	(Note 1)	AC, 60 s	5000	—	—	Vrms

Note 1: This device is considered as a two-terminal device: Pins 1, 2, 3 and 4 are shorted together, and pins 5, 6, 7 and 8 are shorted together.

11. Switching Characteristics (Note) (Unless otherwise specified, T_a = -40 to 125 °C, V_{DD} = 2.7 to 5.5 V)

Characteristics	Symbol	Note	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time (L/H)	t_{pLH}	(Note 1)	Fig. 12.1.5	V_{IN} = 3.3 V, R_T = 820 Ω	80	140	250	ns
Propagation delay time (H/L)	t_{pHL}				60	120	250	
Pulse width distortion	$\|t_{pHL}-t_{pLH}\|$				—	20	50	
Propagation delay skew (device to device)	t_{psk}	(Note 1), (Note 2)			-65	—	65	
Propagation delay skew (channel to channel)	$t_{psk(ch)}$	(Note 1), (Note 3)			-40	—	40	
Rise time	t_r	(Note 1)			—	11	—	
Fall time	t_f				—	13	—	
Propagation delay time (L/H)	t_{pLH}			V_{IN} = 5 V, R_T = 1.6 kΩ	80	140	250	
Propagation delay time (H/L)	t_{pHL}				60	120	250	
Pulse width distortion	$\|t_{pHL}-t_{pLH}\|$				—	20	50	
Propagation delay skew (device to device)	t_{psk}	(Note 1), (Note 2)			-65	—	65	
Propagation delay skew (channel to channel)	$t_{psk(ch)}$	(Note 1), (Note 3)			-40	—	40	
Rise time	t_r	(Note 1)			—	11	—	
Fall time	t_f				—	13	—	
Propagation delay time (L/H)	t_{pLH}		Fig. 12.1.6	I_F = 2 mA, R = 100 Ω	80	135	250	
Propagation delay time (H/L)	t_{pHL}				60	120	250	
Pulse width distortion	$\|t_{pHL}-t_{pLH}\|$				—	15	30	
Propagation delay skew (device to device)	t_{psk}	(Note 1), (Note 2)			-65	—	65	
Propagation delay skew (channel to channel)	$t_{psk(ch)}$	(Note 1), (Note 3)			-40	—	40	
Rise time	t_r	(Note 1)			—	11	—	
Fall time	t_f				—	13	—	
High-level common-mode transient immunity	CM_H		Fig. 12.1.7	V_{IN} = 3.3 V, 5 V, V_{DD} = 3.3 V, 5 V, V_{CM} = 1000 V_{p-p}, T_a = 25 °C	±25	±50	—	kV/μs
Low-level common-mode transient immunity	CM_L				±25	±50	—	

Note: All typical values are at V_{DD} = 5 V, T_a = 25 °C, unless otherwise noted.

Note: Each channel

Note: Recommended input resistance conditions

- V_{IN} = 3.3 V : R_1 = R_2 = 430 Ω
- V_{IN} = 5 V : R_1 = R_2 = 820 Ω

Note 1: f = 250 kHz, duty = 50 %, input current t_r = t_f = less than 5 ns, C_L is less than 15 pF which includes probe and stray wiring capacitance.

Note 2: The propagation delay skew (device to device), t_{psk}, is equal to the magnitude of the worst-case difference in t_{pHL} and/or t_{pLH} that will be seen between units at the same given conditions (supply voltage, input current, temperature, etc.).

Note 3: The propagation delay skew (channel to channel), $t_{psk(ch)}$, is equal to the magnitude of the worst-case difference in t_{pHL} and/or t_{pLH} that will be seen between different channels of a unit at the same given conditions (supply voltage, input current, temperature, etc.).

12. Test Circuits and Characteristics Curves

12.1. Test Circuits

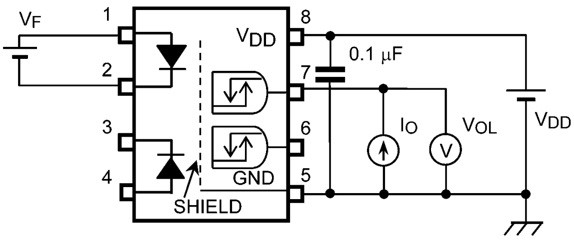


Fig. 12.1.1 V_{OL} Test Circuit

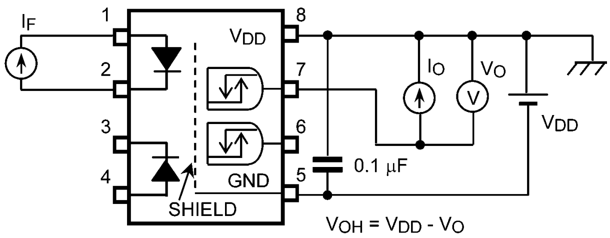


Fig. 12.1.2 V_{OH} Test Circuit

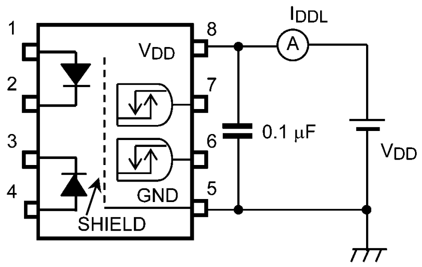


Fig. 12.1.3 I_{DDL} Test Circuit

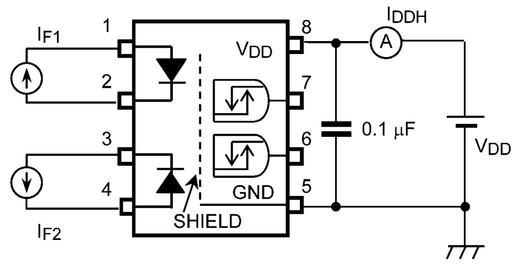
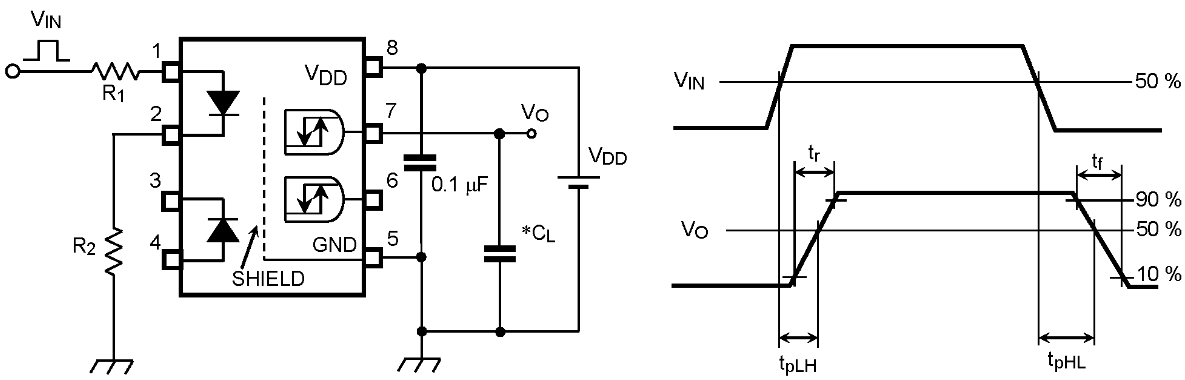


Fig. 12.1.4 I_{DDH} Test Circuit

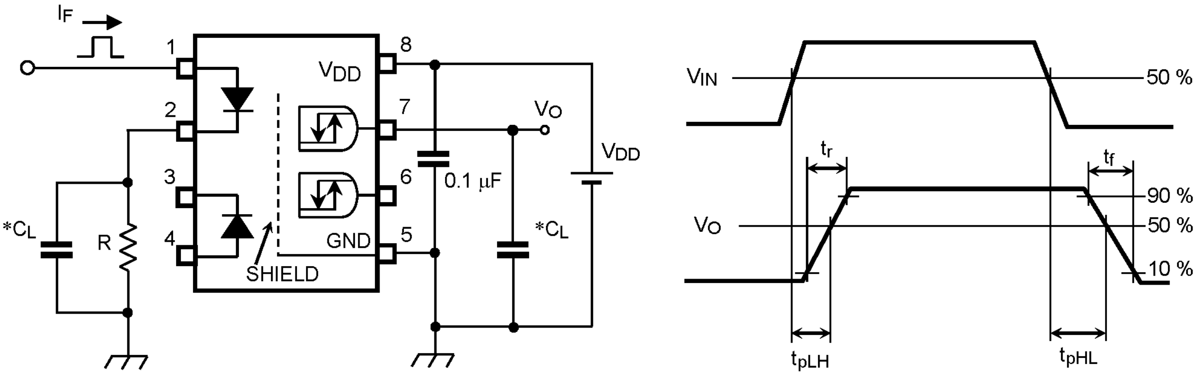
V_{IN} = 3.3 V / 5 V (P.G.)
(f = 250 kHz, duty = 50 %, tr = tf = 5 ns or less)



$R_T = R_1 + R_2$
P.G: Pulse generator
*C_L is less than 15 pF which includes probe and stray wiring capacitance

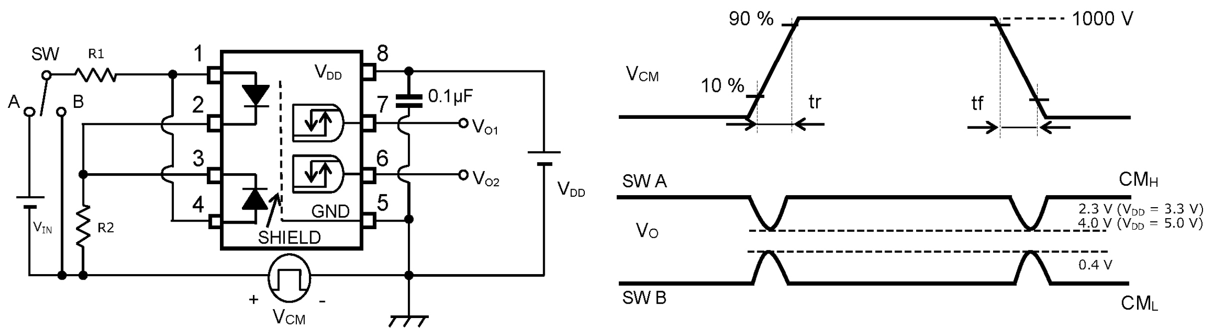
Fig. 12.1.5 Switching Time Test Circuit and Waveform

I_F = 2 mA (P.G.)
(f = 250 kHz, duty = 50 %, tr = tf = 5 ns or less)



$R_T = R_1 + R_2$
P.G: Pulse generator
*C_L is less than 15 pF which includes probe and stray wiring capacitance

Fig. 12.1.6 Switching Time Test Circuit and Waveform



V_{IN} = 3.3 V : R1 = R2 = 430 Ω
V_{IN} = 5 V : R1 = R2 = 820 Ω

$$CM_H = \frac{800\ (V)}{t_r\ (\mu s)} \text{ or } \frac{-800\ (V)}{t_f\ (\mu s)}$$

$$CM_L = \frac{800\ (V)}{t_r\ (\mu s)} \text{ or } \frac{-800\ (V)}{t_f\ (\mu s)}$$

Fig. 12.1.7 Common-Mode Transient Immunity Test Circuit and Waveform

12.2. Characteristics Curves (Note)

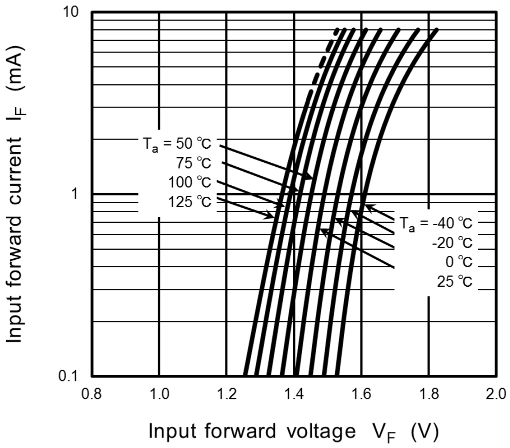


Fig. 12.2.1 I_F - V_F

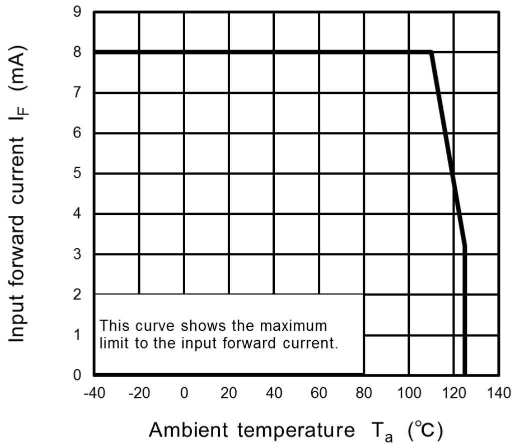


Fig. 12.2.2 I_F - T_a

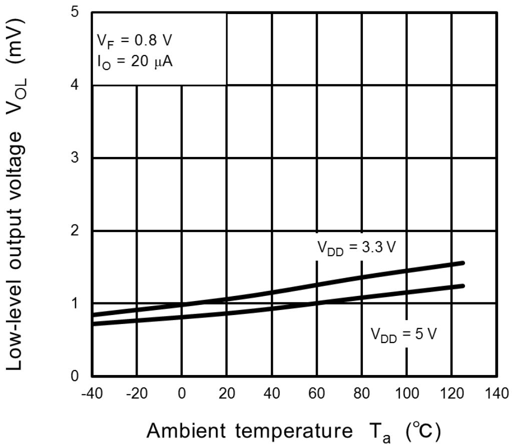


Fig. 12.2.3 V_{OL} - T_a

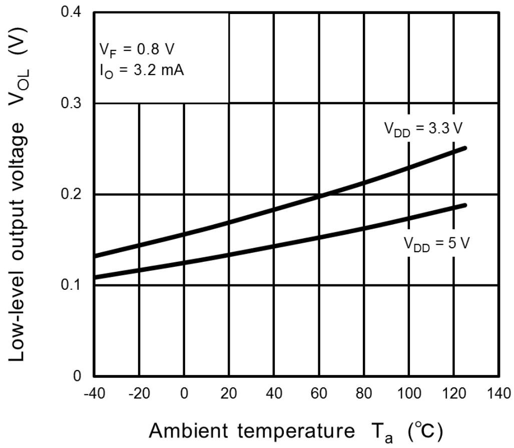


Fig. 12.2.4 V_{OL} - T_a

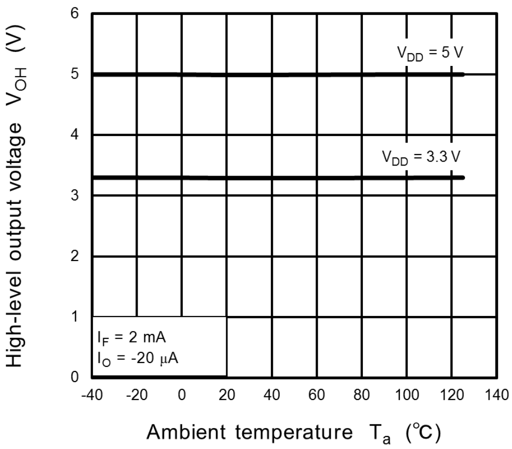


Fig. 12.2.5 V_{OH} - T_a

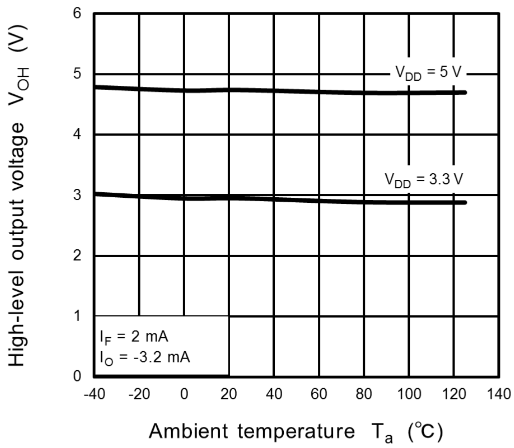


Fig. 12.2.6 V_{OH} - T_a

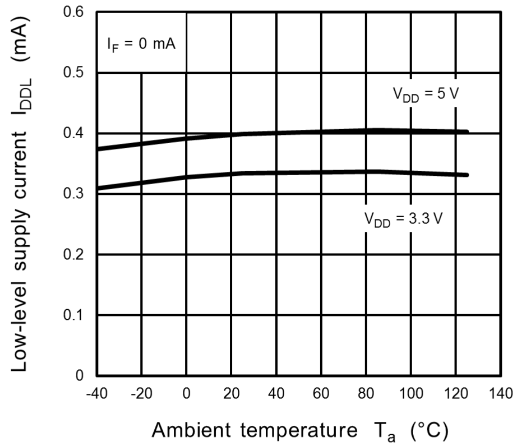


Fig. 12.2.7 I_{DDL} - T_a

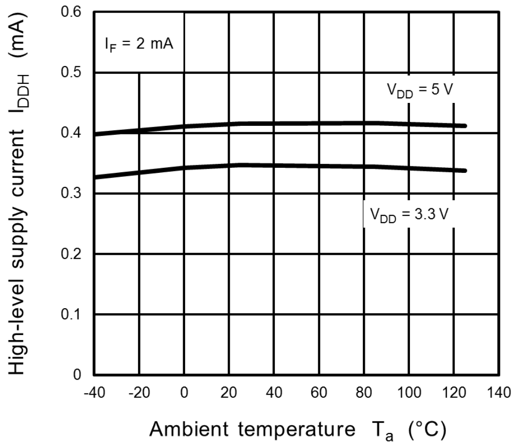


Fig. 12.2.8 I_{DDH} - T_a

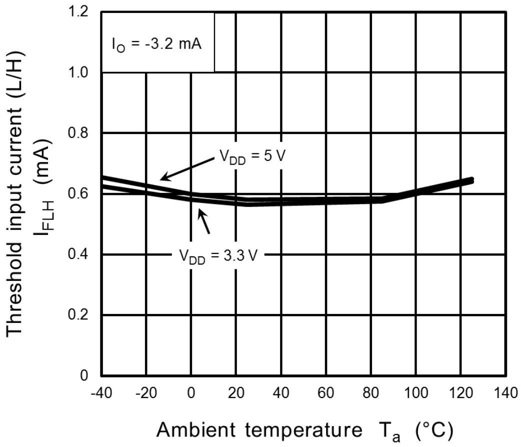


Fig. 12.2.9 I_{FLH} - T_a

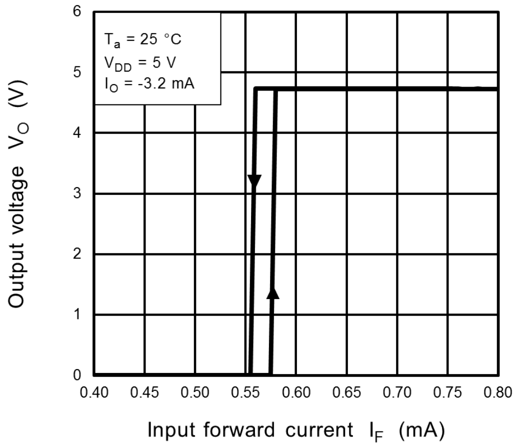


Fig. 12.2.10 V_O - I_F

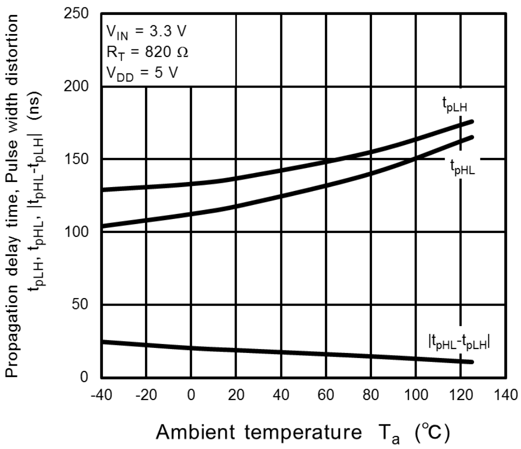


Fig. 12.2.11 t_{pLH}, t_{pHL}, $|t_{pHL} - t_{pLH}|$ - T_a

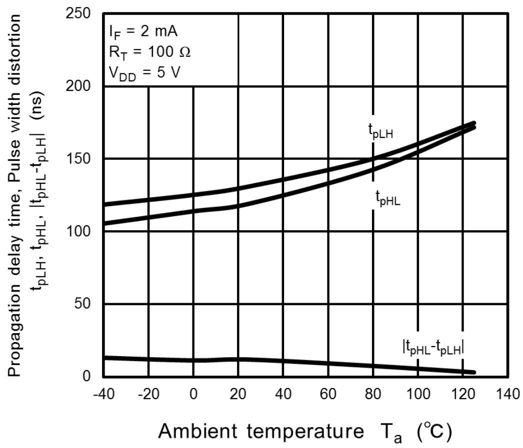


Fig. 12.2.12 t_{pLH}, t_{pHL}, $|t_{pHL} - t_{pLH}|$ - T_a

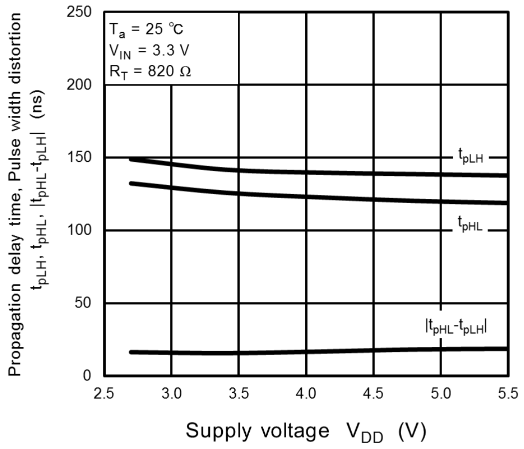


Fig. 12.2.13 t_{pLH}, t_{pHL}, $|t_{pHL} - t_{pLH}|$ - V_{DD}

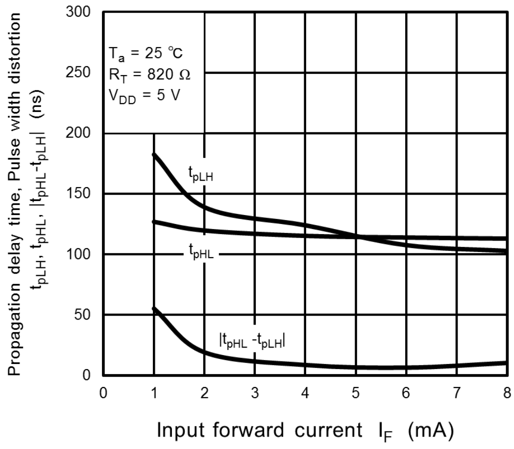


Fig. 12.2.14 t_{pLH}, t_{pHL}, $|t_{pHL} - t_{pLH}|$ - I_F

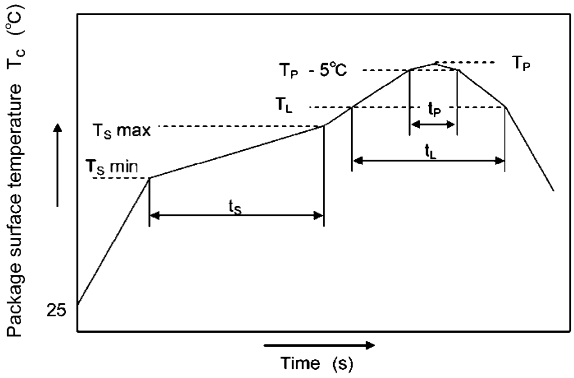
Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

13. Soldering and Storage

13.1. Precautions for Soldering

The soldering temperature should be controlled as closely as possible to the conditions shown below, irrespective of whether a soldering iron or a reflow soldering method is used.

- When using soldering reflow.
  The soldering temperature profile is based on the package surface temperature.
  (See the figure shown below, which is based on the package surface temperature.)
  Reflow soldering must be performed once or twice.
  The mounting should be completed with the interval from the first to the last mountings being 2 weeks.



	Symbol	Min	Max	Unit
Preheat temperature	T_S	150	200	°C
Preheat time	t_S	60	120	s
Ramp-up rate (T_L to T_P)			3	°C/s
Liquidus temperature	T_L	217		°C
Time above T_L	t_L	60	150	s
Peak temperature	T_P		260	°C
Time during which T_c is between (T_P – 5) and T_P	t_P		30	s
Ramp-down rate (T_P to T_L)			6	°C/s

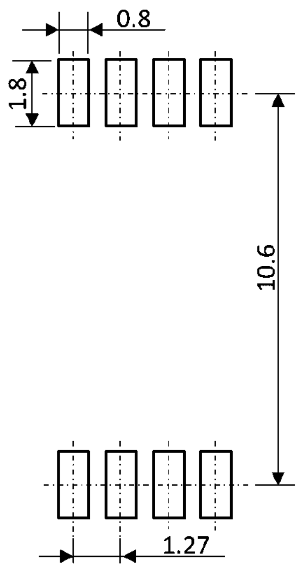
An Example of a Temperature Profile When Lead(Pb)-Free Solder Is Used

- When using soldering flow
  Preheat the device at a temperature of 150 °C (package surface temperature) for 60 to 120 seconds.
  Mounting condition of 260 °C within 10 seconds is recommended.
  Flow soldering must be performed once.
- When using soldering Iron
  Complete soldering within 10 seconds for lead temperature not exceeding 260 °C or within 3 seconds not exceeding 350 °C
  Heating by soldering iron must be done only once per lead.

13.2. Precautions for General Storage

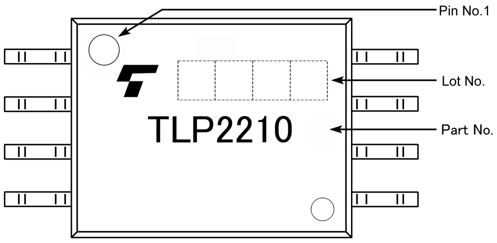
- Avoid storage locations where devices may be exposed to moisture or direct sunlight.
- Follow the precautions printed on the packing label of the device for transportation and storage.
- Keep the storage location temperature and humidity within a range of 5 °C to 35 °C and 45 % to 75 %, respectively.
- Do not store the products in locations with poisonous gases (especially corrosive gases) or in dusty conditions.
- Store the products in locations with minimal temperature fluctuations. Rapid temperature changes during storage can cause condensation, resulting in lead oxidation or corrosion, which will deteriorate the solderability of the leads.
- When restoring devices after removal from their packing, use anti-static containers.
- Do not allow loads to be applied directly to devices while they are in storage.
- If devices have been stored for more than two years under normal storage conditions, it is recommended that you check the leads for ease of soldering prior to use.

14. Land Pattern Dimensions (for reference only)



Unit: mm

15. Marking



16. EN 60747-5-5 Option (D4) Specification

- Part number: TLP2210 **(Note 1)**
- The following part naming conventions are used for the devices that have been qualified according to option (D4) of EN 60747.

  Example: TLP2210(D4-TP4,E

  D4: EN 60747 option
  TP4: Tape type
  E: [[G]]/RoHS COMPATIBLE **(Note 2)**

Note 1: Use TOSHIBA standard type number for safety standard application.
e.g., TLP2210(D4-TP4,E → TLP2210

Note 2: Please contact your Toshiba sales representative for details on environmental information such as the product's RoHS compatibility.
RoHS is the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

Description	Symbol	Rating	Unit
Application classification for rated mains voltage ≤ 150 Vrms for rated mains voltage ≤ 300 Vrms		I-IV I-III	—
Climatic classification		40 / 125 / 21	—
Pollution degree		2	—
Maximum operating insulation voltage	V_{IORM}	1230	Vpeak
Input to output test voltage, Method A V_{pr} = 1.6 × V_{IORM}, type and sample test t_p = 10 s, partial discharge < 5 pC	V_{pr}	1970	Vpeak
Input to output test voltage, Method B V_{pr} =1.875 × V_{IORM}, 100 % production test t_p = 1 s, partial discharge < 5 pC	V_{pr}	2310	Vpeak
Highest permissible overvoltage (transient overvoltage, t_{pr} = 60 s)	V_{TR}	8000	Vpeak
Safety limiting values (max. permissible ratings in case of fault, also refer to thermal derating curve) current (input current I_F, P_{SO} = 0) power (output or total power dissipation) temperature	 I_{si} P_{so} T_s	 300 700 150	 mA mW °C
Insulation resistance — V_{IO} = 500 V, T_a = 25 °C V_{IO} = 500 V, T_a = 100 °C V_{IO} = 500 V, T_a = T_s	R_{si}	$\geq 10^{12}$ $\geq 10^{11}$ $\geq 10^{9}$	Ω

Fig. 16.1 EN 60747 Isolation Characteristics

Minimum creepage distance	Cr	8.0 mm
Minimum clearance	Cl	8.0 mm
Minimum insulation thickness	ti	0.4 mm
Comparative tracking index	CTI	500

Fig. 16.2 Insulation Related Specifications (Note)

Note: This photocoupler is suitable for **safe electrical isolation** only within the safety limit data.
Maintenance of the safety data shall be ensured by means of protective circuits.

Fig. 16.3 Marking on Packing

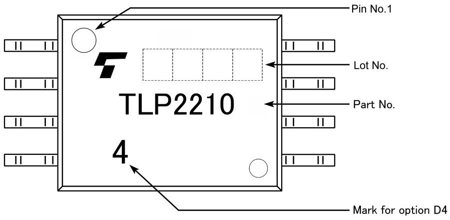


Fig. 16.4 Marking Example (Note)

Note: The above marking is applied to the photocouplers that have been qualified according to option (D4) of EN 60747.

Figure 1 Partial discharge measurement procedure according to EN 60747
Destructive test for qualification and sampling tests.

Method A

(for type and sampling tests, destructive tests)

t_1, t_2	= 1 to 10 s
t_3, t_4	= 1 s
t_p (Measuring time for partial discharge)	= 10 s
t_b	= 12 s
t_{ini}	= 60 s

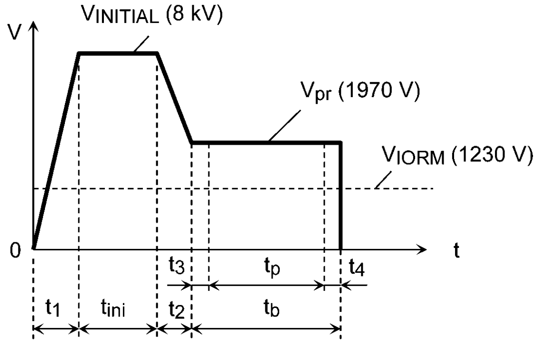


Figure 2 Partial discharge measurement procedure according to EN 60747
Non-destructive test for 100 % inspection.

Method B

(for sample test,non-destructive test)

t_3, t_4	= 0.1 s
t_p (Measuring time for partial discharge)	= 1 s
t_b	= 1.2 s

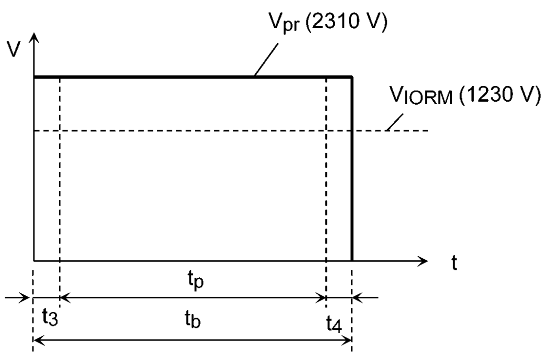


Figure 3 Dependency of maximum safety ratings on ambient temperature

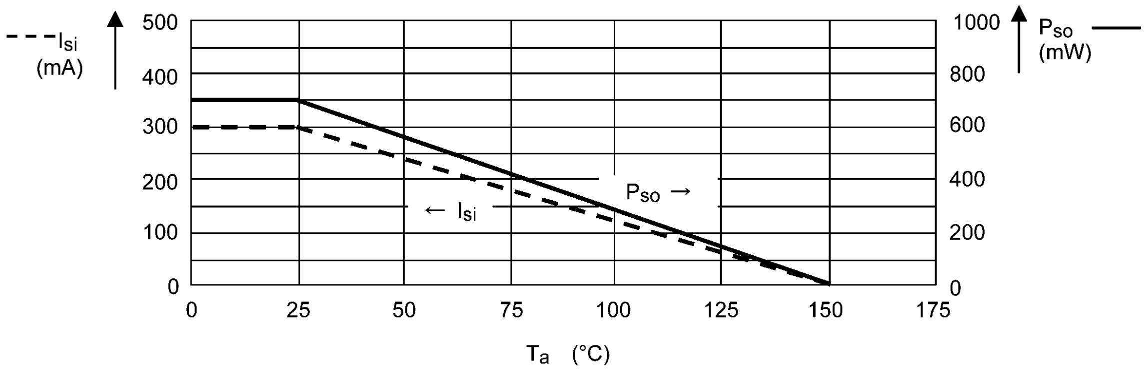


Fig. 16.5 Measurement Procedure

17. Ordering Information

When placing an order, please specify the part number, tape type and quantity as shown in the following example.

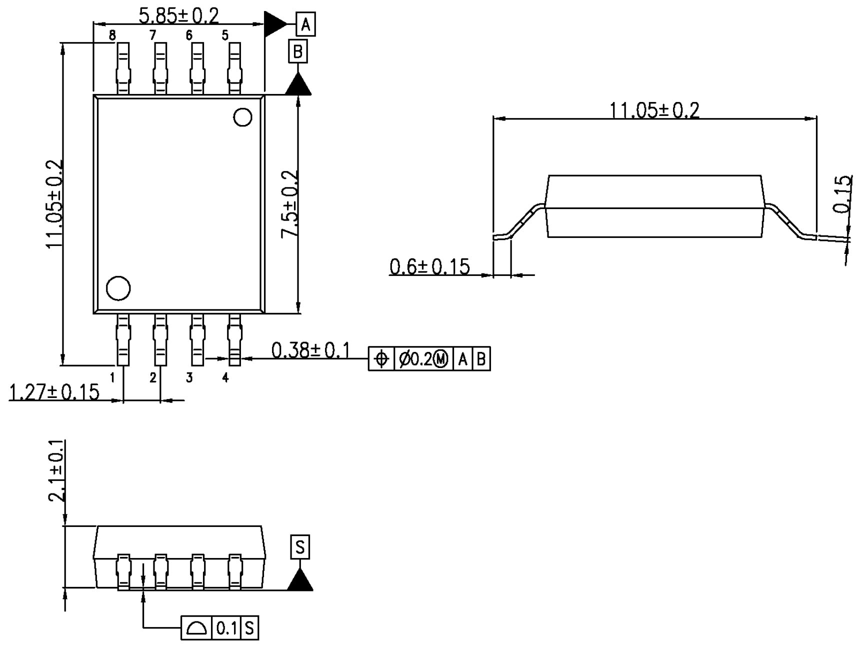
Example) TLP2210(TP4,E 1500 pcs

Part number: TLP2210
Tape type: TP4
[[G]]/RoHS COMPATIBLE: E **(Note 1)**
Quantity (must be a multiple of 1500): 1500 pcs

Note 1: Please contact your Toshiba sales representative for details on environmental information such as the product's RoHS compatibility.
RoHS is the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

Package Dimensions

Unit: mm



Weight: 0.203 g (typ.)

Package Name(s)
TOSHIBA: 11-6B1A

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