



RVT101HVBFWN00

## EVE4 IPS 10.1" LCD TFT DATASHEET

Rev.1.2

2021-07-16

ITEM	CONTENTS	UNIT
LCD Type	TFT/Transmissive/Normally Black/IPS	/
Size	10.1	Inch
Viewing Direction	Free	/
Outside Dimensions (W x H x D)	246.66 x 151.30 x 12.05	mm
Active Area (W x H)	216.96 x 135.60	mm
Pixel Pitch (W x H)	0.1695 x 0.1695	mm
Resolution	1280 x 800	/
Brightness	1000	cd/m <sup>2</sup>
Color Depth	16.7 M	/
Pixel Arrangement	RGB Vertical Stripe	/
Driver IC of Board	BT817Q	/
Interface	SPI/QSPI	/
Host Connector	RiBUS, ZIF 20 pin, 0.5mm pitch, down-side contact	/
With/Without Touch	Without Touch Panel	/
Supply Voltage for Module	3.3	V
Supply Voltage for Backlight	5.0 ÷ 12.0	V
Weight	560	g

**Note 1:** RoHS3 compliant

**Note 2:** LCM weight tolerance: ± 5%.



## 1. REVISION RECORD

REV NO.	REV DATE	CONTENTS	REMARKS
1.0	2021-04-19	Initial Release	
1.1	2021-06-03	Adding assembly guide	
1.2	2021-07-16	Updating the drawing (dimensions in inches, adding the speaker), New template	



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### 3. MODULE CLASSIFICATION INFORMATION

RV	T	101	H	V	B	F	W	N	00
1.	2.	3.	4.	5.	6.	7.	8.	9.	10.

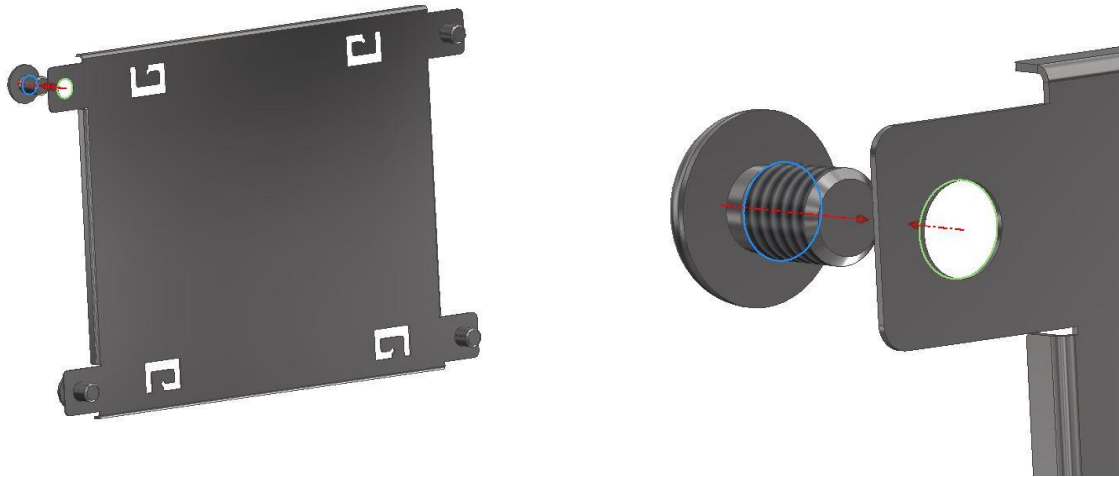
NO.	PARAMETER	SYMBOL
1.	BRAND	RV – Riverdi
2.	PRODUCT TYPE	T – TFT Standard
3.	DISPLAY SIZE	101 – 10.1"
4.	MODEL SERIAL NO.	H – High Brightness, IPS
5.	RESOLUTION	V – 1280 x 800 px
6.	INTERFACE	B – SPI/QSPI
7.	FRAME	F – With Mounting Metal Frame
8.	BACKLIGHT TYPE	W – LED White
9.	TOUCH PANEL	N – Without Touch Panel
10.	VERSION	00 – (00-99)

## 4. ASSEMBLY GUIDE

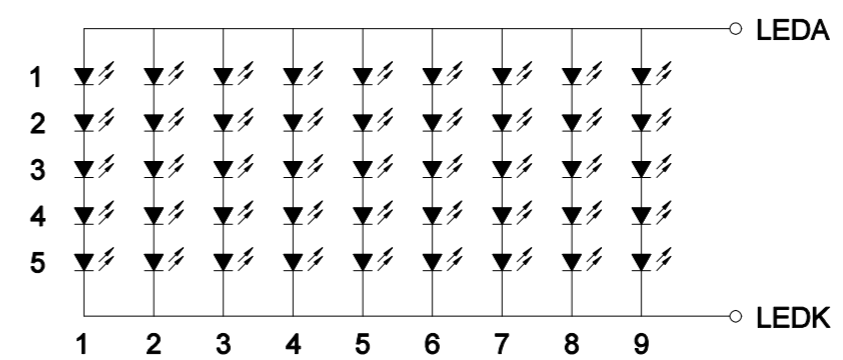
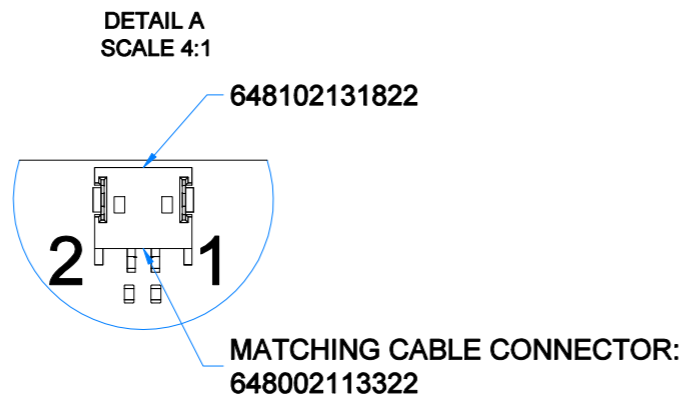
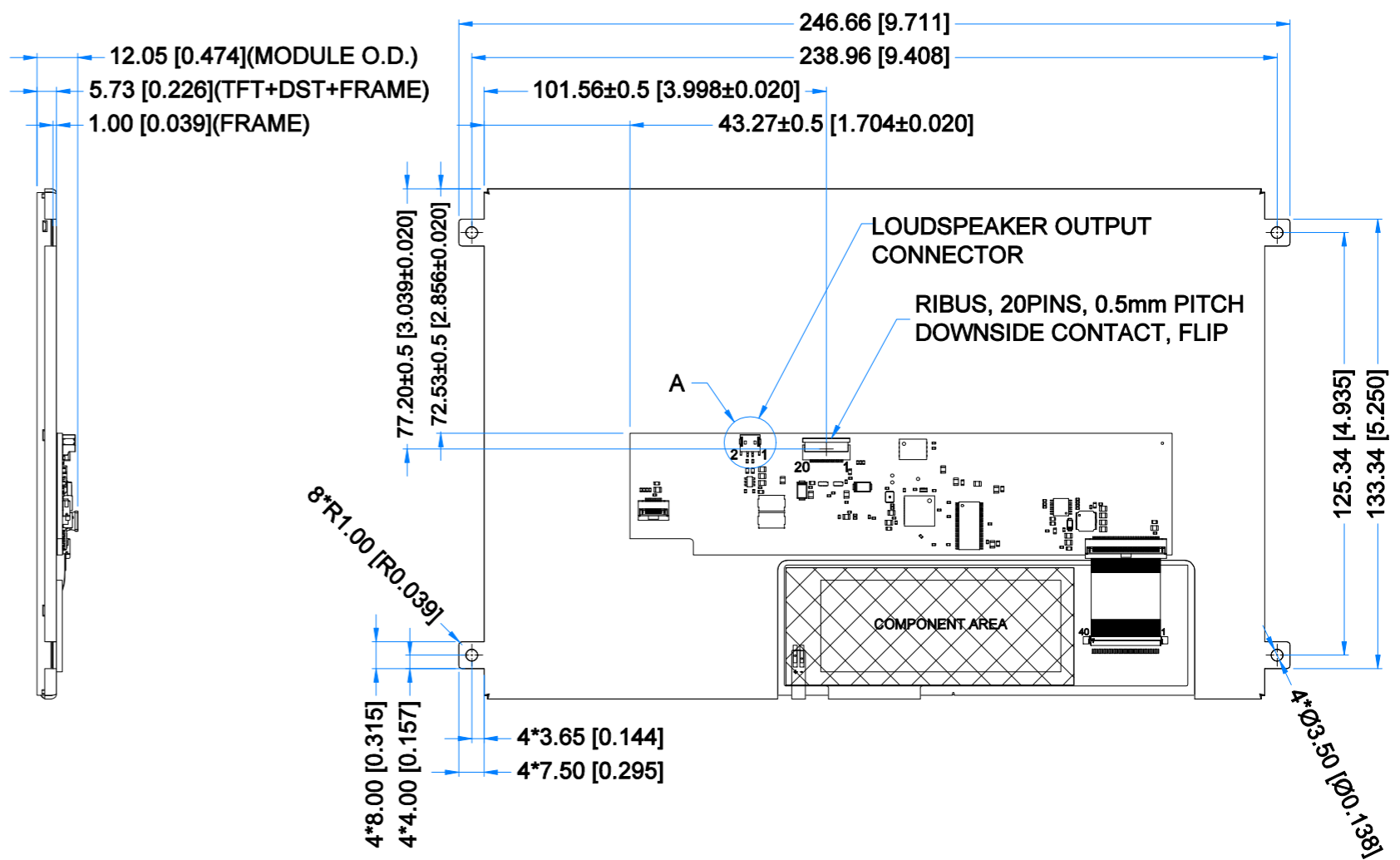
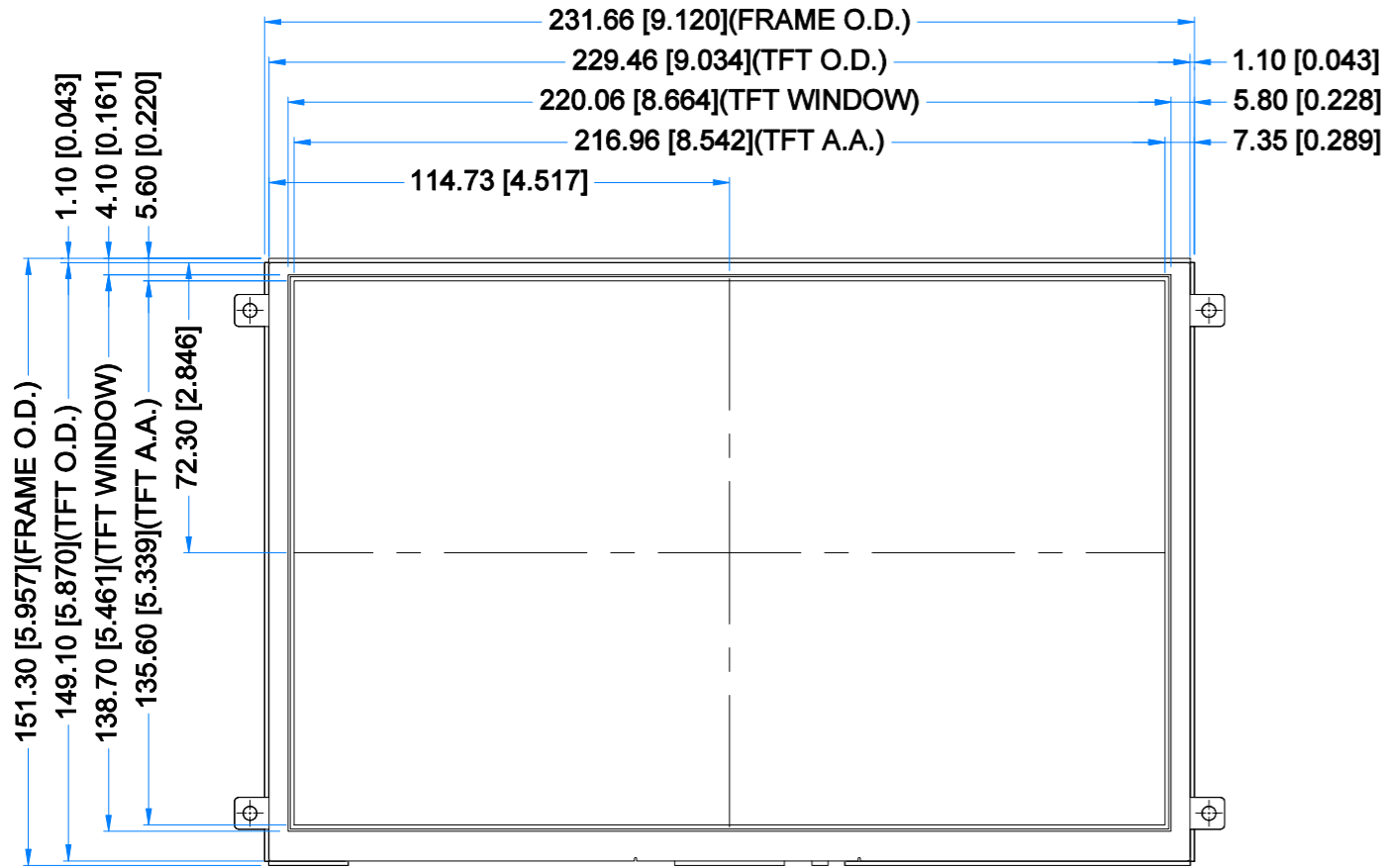
### 4.1 Mounting frame

For dimensions 3.5", 4.3", 5.0", 7.0" and 10.1", the product with mounting frame version is available. Thanks to the four catches attached to the side, frame provides strong assembly to the surface by mounting element (like the screw, see Figure 1). The frames are specially designed to fit Riverdi products perfectly. The diameter of the mounting hole is 3.5mm.

Figure 1. Mounting frame



Revision:	Changes:	Date:
1.0	Initial Case	2021.04.15
1.1	Adding Speaker PN And Matching Connector PN	2021.07.08



LED Diagram Circuit

**LCD NOTES:**  
1. LCD TYPE: TRANSMISSIVE, NORMALLY BLACK, IPS  
2. RESOLUTION: 1280x800  
3. VIEWING ANGLE: FREE  
4. SURFACE LUMINANCE: 1000cd/m<sup>2</sup>  
5. DRIVER IC ON BOARD: BT817Q  
6. INTERFACE: SPI/QSPI  
7. SUPPLY VOLTAGE FOR MODULE: 3.3 V  
8. SUPPLY VOLTAGE FOR BACKLIGHT: 5.0 + 12.0 V, BUILT-IN LED INVERTER

**GENERAL NOTES:**  
1. ZERO BAD PIXELS FOR TFT  
2. OPERATING TEMPERATURE: -20°C ~ 70°C  
3. STORAGE TEMPERATURE: -30°C ~ 80°C  
4. WITHOUT INDIVIDUAL TOLERANCE: ±0.3mm  
5. RoHS3 COMPLIANT

PN: RVT101HVBFWN00			
SN:			
DRAWN: M.Natywa	2021.04.15	1:1.87	
CHECKED: K.Brodacka	2021.07.08	[mm]	
APPR:		ISO A3	



## 6. ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTE
Supply Voltage for Module	VDD	0	3.6	V	NOTE 1
Digital I/O signals (SPI/QSPI/GPIO) Voltage	-	-0.5	3.3		NOTE 1, 2
Supply voltage for Backlight	BLVDD	-0.3	14.0		NOTE 1
Operating Temperature	T <sub>OP</sub>	-20	70	°C	
Storage Temperature	T <sub>ST</sub>	-30	80	°C	
Storage Humidity (@ 25 ± 5°C)	H <sub>ST</sub>	10	-	% RH	
Operating Ambient Humidity (@ 25 ± 5°C)	H <sub>OP</sub>	10	-	% RH	

**Note 1.** Exceeding maximum values may cause improper operation or permanent damage to the unit.

**Note 2.** Digital I/O signals are to be connected to pins 3 ÷ 9, 11 and 12 pins at RiBUS connector (P1).

## 7. ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Supply Voltage for Module	VDD	3.0	3.3	3.6	V	
Current Drawn from VDD	I <sub>VDD</sub>	270	500	TBD	mA	NOTE 1
Input Voltage "H" Level	V <sub>IH</sub>	2.0	-	3.3	V	
Input Voltage "L" Level	V <sub>IL</sub>	-	-	0.8	V	

**Note 1.** The minimum current drawn from VDD is defined with the condition that there is no communication on SPI and the backlight is off.

The maximum current drawn from VDD is defined with the condition that the LCD displays a white screen with 100% of the backlight.

## 8. BACKLIGHT ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Supply Voltage for Backlight	BLVDD	5.0	9.0	14.0	V	
Current drawn from BLVDD @5.0V	I <sub>BLVDD=5.0V</sub>	TBD	1370	TBD	mA	
Current drawn from BLVDD @7.0V	I <sub>BLVDD=7.0V</sub>	TBD	860	TBD		
Current drawn from BLVDD @9.0V	I <sub>BLVDD=9.0V</sub>	TBD	670	TBD		
Current drawn from BLVDD @12.0V	I <sub>BLVDD=12.0V</sub>	TBD	470	TBD		
Lifetime	-	-	50.000	-	hours	NOTE 1

**Note 1.** Operating life means the period in which the LED brightness goes down to 50% of the initial brightness. Typical operating lifetime is the estimated parameter.



## 9. ELECTRO-OPTICAL CHARACTERISTICS

ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT	RMK	NOTE
Response Time	Tr+Tf	$\theta=0^\circ$ $\varnothing=0^\circ$ Ta=25 °C	-	25	35	ms	FIG 2.	4
Contrast Ratio	Cr		800	1000	-	---	FIG 3.	1
Luminance Uniformity	$\delta$ WHITE		-	75	-	%	FIG 3.	3
Surface Luminance	Lv		-	1000	-	cd/m <sup>2</sup>	FIG 3.	2
Viewing Angle Range	$\theta$	$\varnothing = 90^\circ$	75	85	-	deg	FIG 4.	6
		$\varnothing = 270^\circ$	75	85	-	deg	FIG 4.	
		$\varnothing = 0^\circ$	75	85	-	deg	FIG 4.	
		$\varnothing = 180^\circ$	75	85	-	deg	FIG 4.	
CIE (x, y) Chromaticity	Rx	$\theta=0^\circ$ $\varnothing=0^\circ$ Ta=25 °C	0.22	0.26	0.30	-	FIG 3.	5
	Ry		0.20	0.24	0.28	-		
	Gx		0.34	0.38	0.42	-		
	Gy		0.50	0.54	0.58	-		
	Bx		0.10	0.14	0.18	-		
	By		0.09	0.13	0.17	-		
	Wx		0.28	0.32	0.36	-		
	Wy		0.29	0.33	0.37	-		

**Note 1.** Contrast Ratio (CR) is defined mathematically as below, for more information see Figure 3.

$$\text{Contrast Ratio} = \frac{\text{Average Surface Luminance with all white pixels (P1, P2, P3, P4, P5)}}{\text{Average Surface Luminance with all black pixels (P1, P2, P3, P4, P5)}}$$

**Note 2.** Surface luminance is the LCD surface from the surface with all pixels displaying white. For more information see Figure 3.

$$L_v = \text{Average Surface Luminance with all white pixels (P1, P2, P3, P4, P5)}$$

**Note 3.** The uniformity in surface luminance  $\delta$  WHITE is determined by measuring luminance at each test position 1 through 5, and then dividing the minimum luminance of 5 points luminance by maximum luminance of 5 points luminance. For more information see Figure 3.

$$\delta \text{ WHITE} = \frac{\text{Minimum Surface Luminance with all white pixels (P1, P2, P3, P4, P5)}}{\text{Maximum Surface Luminance with all white pixels (P1, P2, P3, P4, P5)}}$$

**Note 4.** Response time is the time required for the display to transition from white to black (Rise Time, Tr) and from black to white (Decay Time, Tf). For additional information see Figure 2. The test equipment is Autronic-Melchers's ConoScope series.

**Note 5.** CIE (x, y) chromaticity, the x, y value is determined by measuring luminance at each test position 1 through 5, and then calculating the average value.

**Note 6.** Viewing angle is the angle at which the contrast ratio is greater than 2. For TFT module the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to LCD surface. For more information see Figure 4.



**Note 7.** For viewing angle and response time testing, the testing data is based on Autronic-Melchers's ConoScope series. Instruments for Contrast Ratio, Surface Luminance, Luminance Uniformity, CIE the test data is based on TOPCON's BM-5 photo detector.

Figure 2. The definition of response time

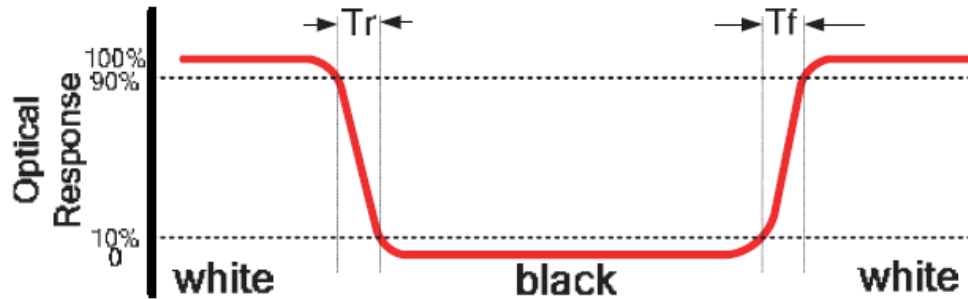
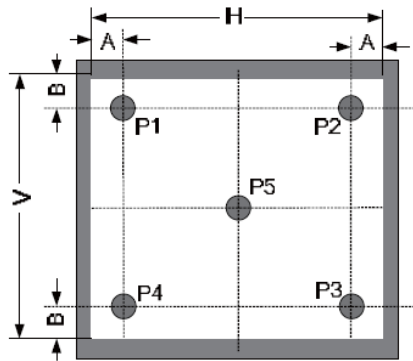


Figure 3. Measuring method for Contrast ratio, surface luminance, Luminance uniformity, CIE (x, y) chromaticity



A: 5mm

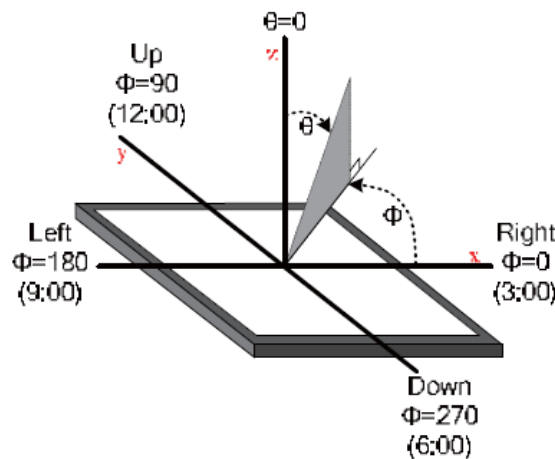
B: 5mm

H, V: Active Area

Light spot size  $\varnothing=5\text{mm}$ , 500mm distance from the LCD surface to detector lens.

Measurement instrument is TOPCON'S luminance meter BM-5

Figure 4. The definition of viewing angle





## 10. INTERFACES DESCRIPTION

### 10.1 P1 connector - RiBUS description

PIN NO.	CONNECTOR	DESCRIPTION	NOTE
1	VDD	Supply voltage for module; TYP 3.3 V	
2	GND	Ground	
3	SPI_SCLK	SPI SCK signal	
4	MISO/ IO.1	SPI MISO signal / SPI Quad mode: SPI data line 1	
5	MOSI/ IO.0	SPI MOSI signal / SPI Quad mode: SPI data line 0	
6	CS	SPI chip select signal	
7	INT	Interrupt signal from device to the system, Active Low, Internally 47k Pull UP	
8	RST/PD	Reset / Power down signal, Active Low, Internally Pulled UP 47k	
9	GPIO.0	GPIO.0	
10	DISP_AUDIO	Display audio in/out	NOTE 1
11	GPIO.1/IO.2	SPI Single/Dual mode: General purpose IO0. QSPI mode: SPI data line 2	
12	GPIO.2/IO.3	SPI Single/Dual mode: General purpose IO1. QSPI mode: SPI data line 3	
13	NC	Not connected	
14	NC	Not connected	
15	NC	Not connected	
16	NC	Not connected	
17	BLVDD	Supply voltage for backlight	
18	BLVDD	Supply voltage for backlight	
19	BLGND	Backlight Ground, Internally connected to GND	
20	BLGND	Backlight Ground, Internally connected to GND	

**Note 1.** Requirements for audio external signal voltage will be announced after samples have been tested.

### 10.2 P2 connector description

PIN NO.	SYMBOL	DESCRIPTION	NOTE
1	SPEAKER +	Speaker coil "+" terminal	NOTE 1
2	SPEAKER -	Speaker coil "-" terminal	

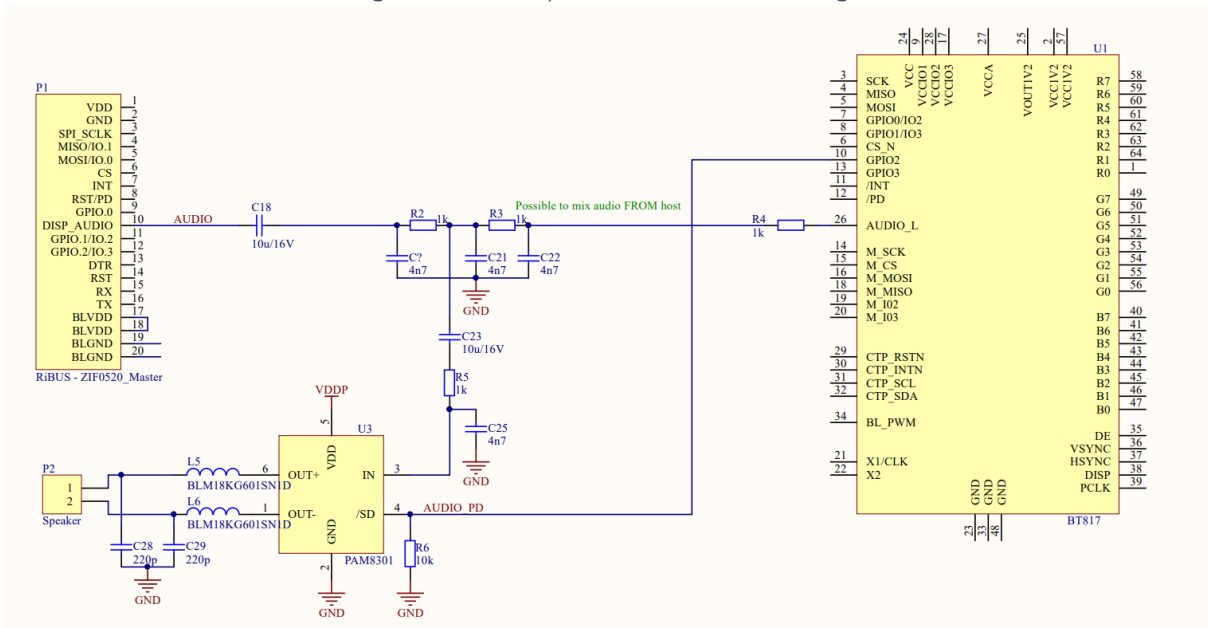
The audio circuit allows for the following 3 things:

1. To play sounds from BT817Q on internal amplifier U3.
2. To play sounds from host on internal amplifier U3.
3. To play sounds from BT817Q on external amplifier.

**Note 1.** The loudspeaker assembly (loudspeaker + cables + plug compatible with P2 connector) will be sold separately. The documentation of the loudspeaker assembly will be released soon.



Figure 5. The simplified audio circuit design



**Note 2.** Controller board in RVT101HVBFWN00 is equipped with the separate 512Mb flash memory chip, which allows to store up to 110 full resolution (1280 \* 800 pixels, JPG) images. If you need to change the memory size, please contact us: [contact@riverdi.com](mailto:contact@riverdi.com)

## 11. BT817Q CONTROLLER SPECIFICATION

BT817Q or EVE4 (Embedded Video Engine 4) simplifies the system architecture for advanced human machine interfaces (HMIs) by providing functionality for display, audio, and touch as well as an object-oriented architecture approach that extends from display creation to the rendering of the graphics.

### 11.1 Serial host interface

Figure 6. SPI single/dual interface connection

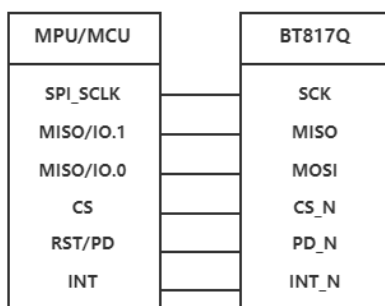
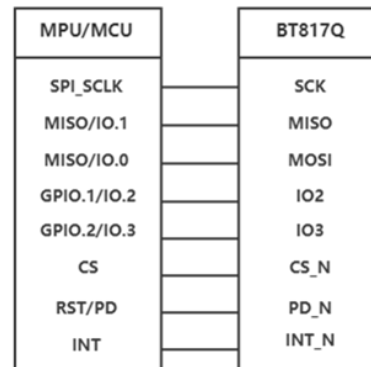


Figure 7. QSPI interface connection



**SPI Interface** – the SPI slave interface operates up to 30MHz (It depends on EVE4 system clock frequency and needs verification in Riverdi lab).

Only SPI mode 0 is supported. The SPI interface is selected by default.

**QSPI Interface** – the QSPI slave interface operates up to 30MHz (It depends on EVE 4 system clock frequency and will be verified in Riverdi lab). Only SPI mode 0 is supported.

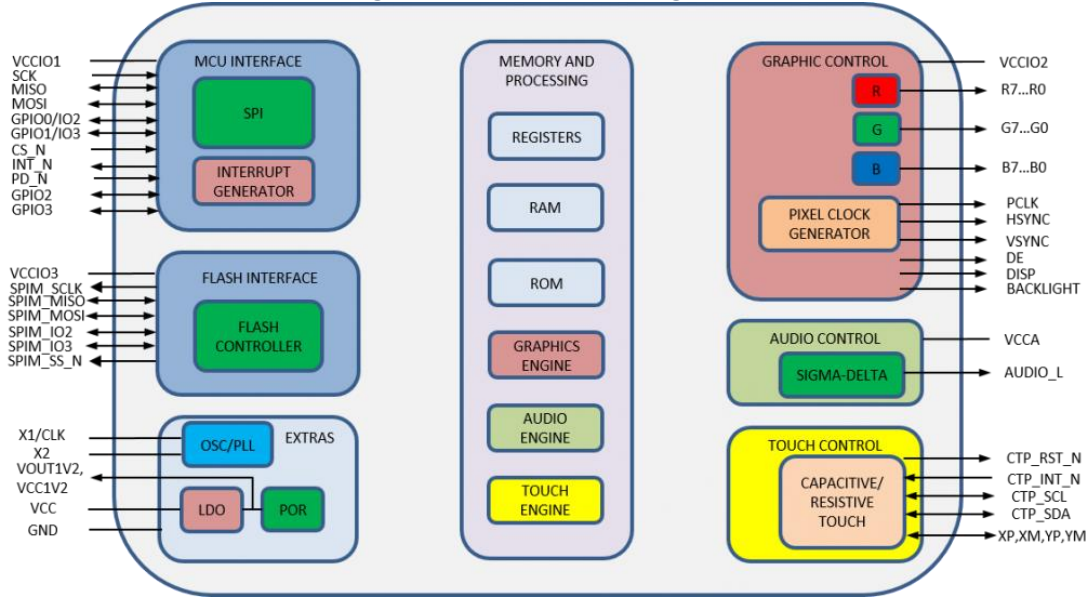
The QSPI can be configured as a SPI slave in SINGLE, DUAL or QUAD channel modes.



By default, the SPI slave operates in the SINGLE channel mode with MOSI as input from the master and MISO as output to the master. DUAL and QUAD channel modes can be configured through the SPI slave itself. To change the channel modes, write to register REG\_SPL\_WIDTH.

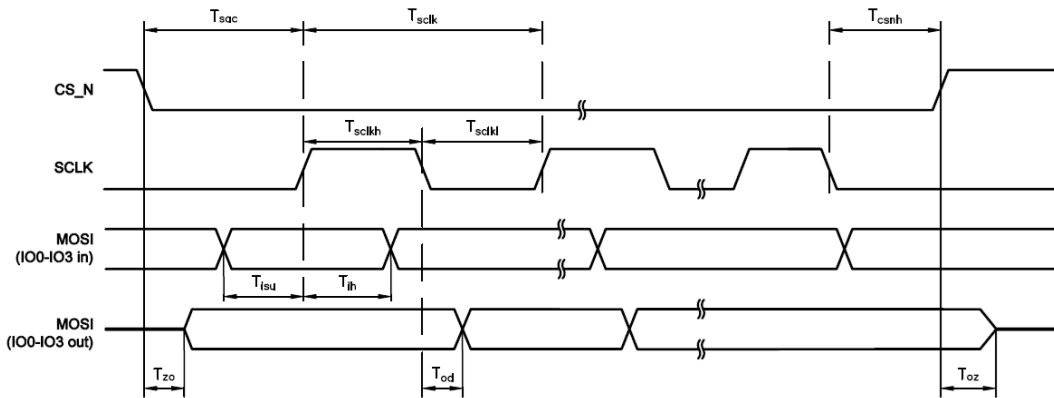
### 11.2 Block diagram

Figure 8. BT817Q Block diagram



### 11.3 Host interface SPI mode 0

Figure 9. SPI timing diagram



The meanings of the timings in the Figure 9 are defined in the table below.



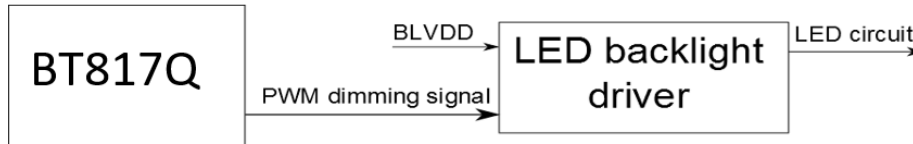
PARAMETER	DESCRIPTION	VCCIO=1.8V		VCCIO=2.5V		VCCIO=3.3V		UNIT
		Min	Max	Min	Max	Min	Max	
T <sub>sclk</sub>	SPI clock period	33.3	-	33.3	-	33.3	-	ns
T <sub>sckl</sub>	SPI clock low duration	13	-	13	-	13	-	
T <sub>sckh</sub>	SPI clock high duration	13	-	13	-	13	-	
T <sub>sac</sub>	SPI access time	4	-	3.5	-	3	-	
T <sub>isu</sub>	Input Setup	4	-	3.5	-	3	-	
T <sub>ih</sub>	Input Hold	0	-	0	-	0	-	
T <sub>zo</sub>	Output enable delay	-	16	-	13	11	-	
T <sub>oz</sub>	Output disable delay	-	13	-	11	10	-	
T <sub>od</sub>	Output data delay	-	15	-	12	11	-	
T <sub>csnh</sub>	CSN hold time	0	-	0	-	0	-	

For more information about BT817Q controller please go to official BT81x website.  
<https://brtchip.com/bt81x/>

### 11.4 Backlight driver block diagram

Backlight enable signal is internally connected to BT817Q backlight control pin. This pin is controlled by two BT817Q's registers. One of them specifies the PWM output frequency, second one specifies the duty cycle. Refer to BT817Q datasheet for more information. After we have done the test on samples, more detailed description will be given in this document.

Figure 10. Backlight driver block diagram



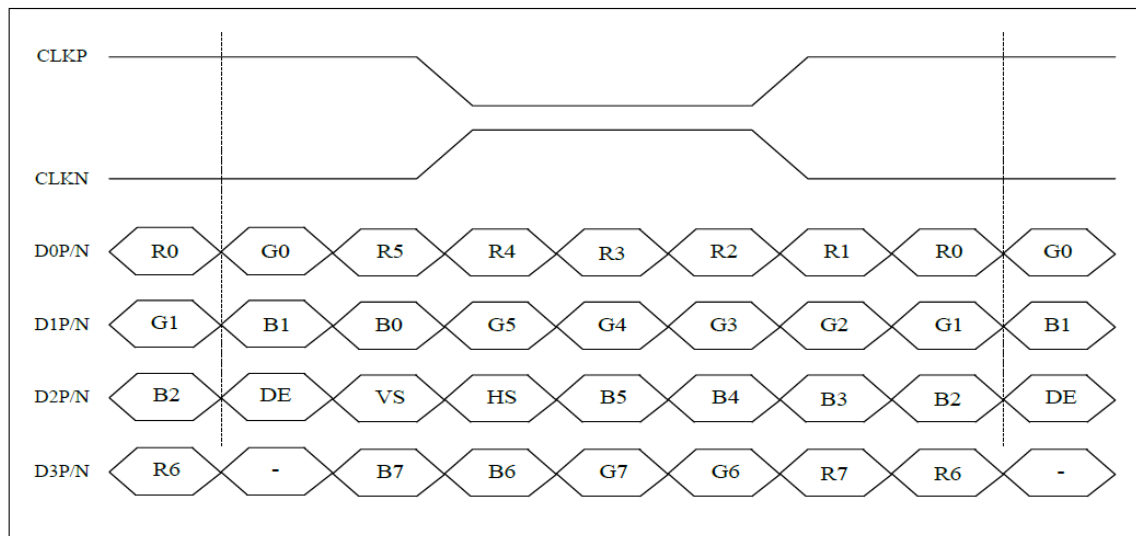
The LED backlight driver used in this module does not burst the LED current. Therefore, it does not generate audible noises on the output capacitor. It is equipped with soft start subsystem, which increases LED lifetime, as LED current peaks are reduced significantly.



## 12. TIMING CHARACTERISTICS

### 12.1 LVDS interface characteristic

VESA Format: 8-bit LVDS input, (LVBIT=H, LVFMT=H)



**Note 1: Control signals** DE VS HS: Active Low

### 12.2 Timing table

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Clock Frequency (Rate=60Hz (LVDS))	$F_{DCLK}$	66.3	72.4	78.9	MHz
HSYNC Period Time	$T_H$	1380	1440	1500	DCLK
Horizontal Display area	$T_{HD}$	1280			DCLK
Hsync Pulse Width	$T_{HPW}$	1	-	40	Tc
Hsync Back Porch (With pulse width)	$T_{HBP}$	88	88	88	DCLK
Hsync Front Porch	$T_{HFP}$	12	72	132	DCLK
VSYNC Period Time	$T_V$	824	838	872	H
Vertical Display area	$T_{VD}$	800			
Vsync Pulse Width	$T_{VW}$	1	-	20	
Vsync Back Porch (With pulse width)	$T_{VBP}$	23	23	23	
Vsync Front Porch	$T_{VFP}$	1	15	49	



### 13. MODULE INITIALIZATION

1. Initialization data, timings and example codes are available on the Riverdi GitHub, at address: <https://github.com/riverdi/riverdi-eye>

2. REGISTER VALUES:

REG_HSIZE	1280
REG_VSIZE	800
REG_HCYCLE	1440
REG_HOFFSET	88
REG_HSYNCO	0
REG_HSYNC1	20
REG_VCYCLE	838
REG_VOFFSET	23
REG_VSYNCO	0
REG_VSYNC1	10
REG_PCLK	1
REG_SWIZZLE	0
REG_PCLK_POL	1
REG_CSPREAD	0
REG_DITHER	0
REG_PCLK_FREQ	0x8c1
REG_PCLK_2X	1

## 14. INSPECTION

Standard acceptance/rejection criteria for TFT module

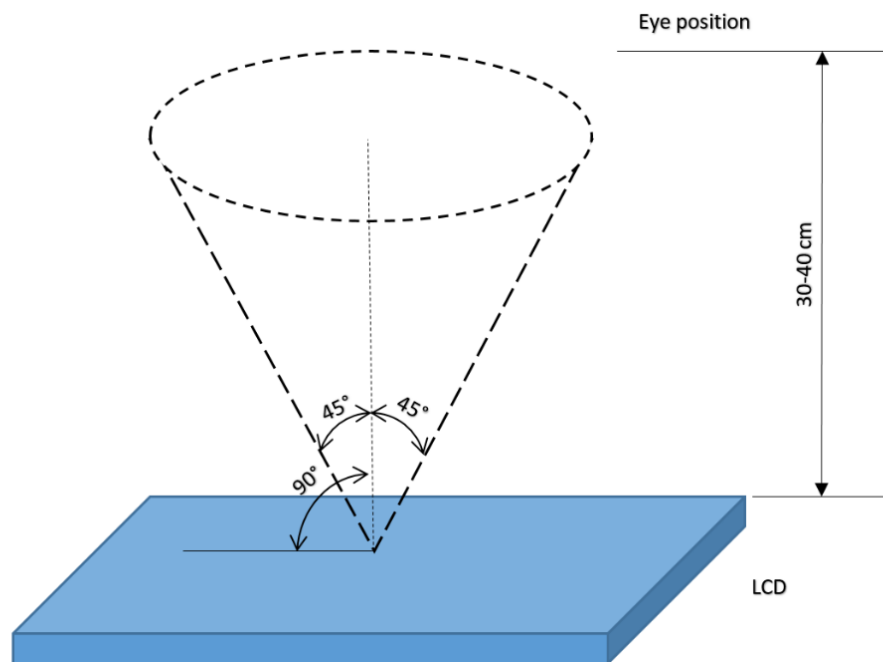
### 14.1 Inspection condition

Ambient conditions:

- Temperature:  $25 \pm 2^{\circ}\text{C}$
- Humidity:  $(60 \pm 10) \%RH$
- Illumination: Single fluorescent lamp non-directive (300 to 700 lux)

Viewing distance:  $35 \pm 5\text{cm}$  between inspector bare eye and LCD.

Viewing Angle: U/D:  $45^{\circ}/45^{\circ}$ , L/R:  $45^{\circ}/45^{\circ}$

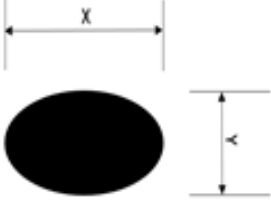
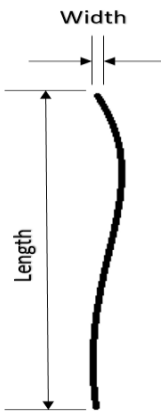






### 14.2 Inspection standard

The LCD TFT has zero bad pixels. Please refer the item “Bright/Dark dots”.

ITEM		CRITERION		
Black spots, white spots, light leakage, Foreign Particle (round Type)	 $D=(x+y)/2$ Spots density: 10 mm	Size =10.1"		
		Average Diameter	Qualified Qty	
		$D \leq 0.2$ mm	Ignored	
		$0.2 \text{ mm} < D \leq 0.3 \text{ mm}$	$N \leq 4$	
		$0.5 \text{ mm} < D$	$N = 0$	
LCD black spots, white spots, light leakage (line Type)	 Spots density: 10 mm	Size =10.1"		
		Length	Width	Qualified Qty
		-	$W \leq 0.05$	Ignored
		$L \leq 5.0$	$0.05 < W \leq 0.1$	$N \leq 3$
		$5.0 < L$	$0.10 < W$ $5.0 < L$	$N = 0$
Bright/Dark Dots	Size =10.1"			
	Item	Qualified Qty		
	Bright dots	0		
	Dark dots	0		
	Cluster Bright Dots or Dark Dots	0		
Total Bright and Dark Dots		0		
Clear spots	Size $\geq 5$ "			
	Average Diameter	Qualified Qty		
	$D < 0.2$ mm	Ignored		
	$0.2 \text{ mm} < D < 0.3 \text{ mm}$	4		
	$0.3 \text{ mm} < D < 0.5 \text{ mm}$	2		
	$0.5 \text{ mm} < D$	0		
Spots density: 10 mm				



## 15. RELIABILITY TEST

NO.	TEST ITEM	TEST CONDITION	NOTE
1	High Temperature Storage	80°C/120 hours	Note 1
2	Low Temperature Storage	-30°C/120 hours	
3	High Temperature Operating	70 °C /120 hours	
4	Low Temperature Operating	-20°C/120 hours	
5	High Temperature and High Humidity	Humidity 40°C, 90%RH, 120Hrs	
6	Thermal Cycling Test (No operation)	-20°C for 30min, 70°C for 30 min. 100 cycles. Then test at room temperature after 1 hour	Note 2
7	Vibration Test	Frequency: 10 ÷ 55 Hz. Stroke: 1.5 mm. Sweep: 10Hz ÷ 55Hz ÷ 10 Hz. 2 hours for each direction of X, Y, Z (Total 6 hours)	
8	Package Drop Test	Height: 60 cm 1 corner, 3 edges, 6 surfaces	

**Note 1.** Sample quantity for each test item is 5 ÷ 10 pcs.

**Note 2.** Before cosmetic and function test, the product must have enough recovery time, at least 2 hours at room temperature.



## 16.LEGAL INFORMATION

Riverdi grants the guarantee for the proper operation of the goods for a period of 12 months from the date of possession of the goods. If in a consequence of this guaranteed execution the customer has received the defects-free item as replacement for the defective item, the effectiveness period of this guarantee shall start anew from the moment the customer receives the defects-free item.

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