



MICRO SPIDER (ORG4475) GPS RECEIVER MODULE

Datasheet

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1. SCOPE

This document describes the features and specifications of Micro Spider ORG4475 GPS receiver module.

2. DISCLAIMER

All trademarks are properties of their respective owners.

Performance characteristics listed in this document do not constitute a warranty or guarantee of product performance. OriginGPS assumes no liability or responsibility for any claims or damages arising out of the use of this document, or from the use of integrated circuits based on this document.

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OriginGPS reserves the right to conduct, from time to time, and at its sole discretion, firmware upgrades. As long as those FW improvements have no material change on end customers, PCN may not be issued. OriginGPS navigation products are not recommended to use in life saving or life sustaining applications.

3. SAFETY INFORMATION

Improper handling and use can cause permanent damage to the product.

4. ESD SENSITIVITY

This product is ESD sensitive device and must be handled with care.



5. CONTACT INFORMATION

Support - info@origingps.com or [Online Form](#)

Marketing and sales - marketing@origingps.com

Web – www.origingps.com

6. RELATED DOCUMENTATION

No	DOCUMENT NAME
1	Micro Spider – ORG4475 Evaluation Kit Datasheet
2	Micro Spider – ORG4475 Product Change Notification
3	Spider and Hornet - Software User Manual for CSR® based receivers
4	Spider and Hornet - NMEA Protocol Reference Manual for CSR® based receivers
5	Spider and Hornet - One Socket Protocol Reference Manual for CSR® based receivers
6	Spider and Hornet - Host Interface Application Note
7	Spider and Hornet - Low Power Modes Application Note
8	Spider and Hornet - Jammer Detector and Remover Application Note
9	Spider and Hornet - Client Generated Extended Ephemeris Application Note
10	Spider and Hornet - Server Generated Extended Ephemeris Application Note
11	Spider and Hornet - Ephemeris Push Application Note

TABLE 1 – RELATED DOCUMENTATION

7. REVISION HISTORY

REVISION	DATE	CHANGE DESCRIPTION
A00	June 1, 2012	First release
2.0	April 1, 2014	Format update, content update according to PCN

TABLE 2 – REVISION HISTORY

8. GLOSSARY

A-GNSS Assisted **GNSS**

BPF Band Pass Filter

CE European Community conformity mark

CGEE™ Client Generated Extended Ephemeris

CMOS Complementary **Metal-Oxide Semiconductor**

COMPASS PRC GNSS (same as **BDS BeiDou-2 Navigation Satellite System**)

EGNOS European **Geostationary Navigation Overlay Service**

EMC Electro-**Magnetic Compatibility**

ESD Electro-**Static Discharge**

EVB Evaluation **Board**

EVK Evaluation **Kit**

FCC Federal **Communications Commission**

GALILEO EU GNSS

GLONASS **Global Navigation Satellite System**

GNSS **Global Navigation Satellite System**

GPS **Global Positioning System**

I²C **Inter-Integrated Circuit**

IC **Integrated Circuit**

ISO **International Organization for Standardization**

LDO **Low Dropout** regulator

LGA **Land Grid Array**

LNA **Low Noise Amplifier**

MSAS **Multi-functional Satellite Augmentation System**

MSL **Moisture Sensitivity Level**

NFZ™ **Noise-Free Zones System**

NMEA **National Marine Electronics Association**

MEMS **MicroElectroMechanical Systems**

PCB **Printed Circuit Board**

PPS **Pulse Per Second**

QZSS **Quasi-Zenith Satellite System**

REACH **Registration, Evaluation, Authorisation and Restriction of Chemical substances**

RF **Radio Frequency**

RHCP **Right-Hand Circular Polarized**

RoHS **Restriction of Hazardous Substances directive**

ROM **Read-Only Memory**

RTC **Real-Time Clock**

SAW **Surface Acoustic Wave**

SBAS **Satellite-Based Augmentation Systems**

SGEE™ **Server Generated Extended Ephemeris**

SIP **System In Package**

SMD **Surface Mounted Device**

SMT **Surface-Mount Technology**

SOC **System On Chip**

SPI **Serial Peripheral Interface**

TCXO **Temperature-Compensated Crystal Oscillator**

TTF **Time To First Fix**

TTL **Transistor-Transistor Logic**

UART **Universal Asynchronous Receiver/Transmitter**

WAAS **Wide Area Augmentation System**

9. ABOUT SPIDER FAMILY

OriginGPS GNSS receiver modules have been designed to address markets where size, weight, stand-alone operation, highest level of integration, power consumption and design flexibility - all are very important.

OriginGPS' Spider family breaks size barrier, offering the industry's smallest fully-integrated, highly-sensitive GPS and GNSS modules.

Spider family features OriginGPS' proprietary NFZ™ technology for high sensitivity and noise immunity even under marginal signal condition, commonly found in urban canyons, under dense foliage or when the receiver's position in space rapidly changes.

Spider family enables the shortest TTM (Time-To-Market) with minimal design risks.

Just connect an antenna and power supply on a 2-layer PCB.

10. ABOUT MICRO SPIDER MODULE

Micro Spider is a complete SiP featuring LGA SMT footprint designed to commit unique integration features for high volume cost sensitive applications.

Designed to support ultra-compact applications such as smart watches, wearable devices, trackers and digital cameras, Micro Spider ORG4475 module is a miniature multi-channel GPS with SBAS, QZSS and other regional overlay systems receiver that continuously tracks all satellites in view, providing real-time positioning data in industry's standard NMEA format.

Micro Spider ORG4475 module offers superior sensitivity and outstanding performance, achieving rapid TTFF in less than one second, accuracy of approximately two meters, and tracking sensitivity of -163dBm.

Sized only 5.6mm x 5.6mm Micro Spider ORG4475 module is industry's small sized, record breaking solution.

ORG4475 module integrates LNA, SAW filter, TCXO, RTC crystal and RF shield with market-leading SiRFstarIV™ GPS SoC.

Micro Spider ORG4475 module is introducing industry's lowest energy per fix ratio, unparalleled accuracy and extremely fast fixes even under challenging signal conditions, such as in built-up urban areas, dense foliage or even indoor.

Integrated GPS SoC incorporating high-performance microprocessor and sophisticated firmware keeps positioning payload off the host, allowing integration in embedded solutions with low computing resources.

Innovative architecture can detect changes in context, temperature, and satellite signals to achieve a state of near continuous availability by maintaining and opportunistically updating its internal fine time, frequency, and satellite ephemeris data while consuming mere microwatts of battery power.

11. ABOUT ORIGINGPS

OriginGPS is a world leading designer, manufacturer and supplier of miniature positioning modules, antenna modules and antenna solutions.

OriginGPS modules introduce unparalleled sensitivity and noise immunity by incorporating Noise Free Zone system (NFZ™) proprietary technology for faster position fix and navigation stability even under challenging satellite signal conditions.

Founded in 2006, OriginGPS is specializing in development of unique technologies that miniaturize RF modules, thereby addressing the market need for smaller wireless solutions.

12. DESCRIPTION

12.1. FEATURES

- + Autonomous operation
- + OriginGPS Noise Free Zone System (NFZ™) technology
- + Fully integrating:
 - LNA, SAW Filter, TCXO, RTC Crystal, RF Shield, GPS SoC, Power Management Unit
- + Active or Passive antenna support
- + GPS L1 1575.42 frequency, C/A code
- + SBAS (WAAS, EGNOS, MSAS) and QZSS support
- + 48 channels
- + Ultra-high Sensitivity down to -163dBm enabling Indoor Tracking
- + TTFF of < 1s in 50% of trials under Hot Start conditions
- + Low Power Consumption of < 9mW in ATP™ mode
- + High Accuracy of < 2.5m in 50% of trials
- + High update rate of 5Hz, 1Hz by default
- + Autonomous A-GPS by Client Generated Extended Ephemeris (CGEE™) for non-networked devices
- + Predictive A-GPS by Server Generated Extended Ephemeris (SGEE™) for connected devices
- + Ephemeris Push™ for storing and loading broadcast ephemeris
- + Host controlled power saving mode
- + Self-managed low power modes - ATP™, PTF™, APM™ and SiRFAware™ MPM
- + Almanac Based Positioning (ABP™)
- + Multipath and cross-correlation mitigation
- + Active Jammer Detector and Remover
- + Fast Time Synchronization for rapid single satellite time solution
- + ARM7® microprocessor system
- + Selectable UART, SPI or I²C host interface
- + NMEA protocol by default, switchable into One Socket Protocol (OSP™)
- + Programmable baud rate and messages rate
- + 1PPS output
- + Antenna input DC blocked and matched 50Ω
- + Single voltage supply
- + Ultra-small LGA footprint of 5.6mm x 5.6mm
- + Surface Mount Device (SMD)
- + Optimized for automatic assembly and reflow processes
- + Operating from -40°C to +85°C
- + FCC, CE, VCCI certified
- + RoHS II/REACH compliant

12.2. ARCHITECTURE

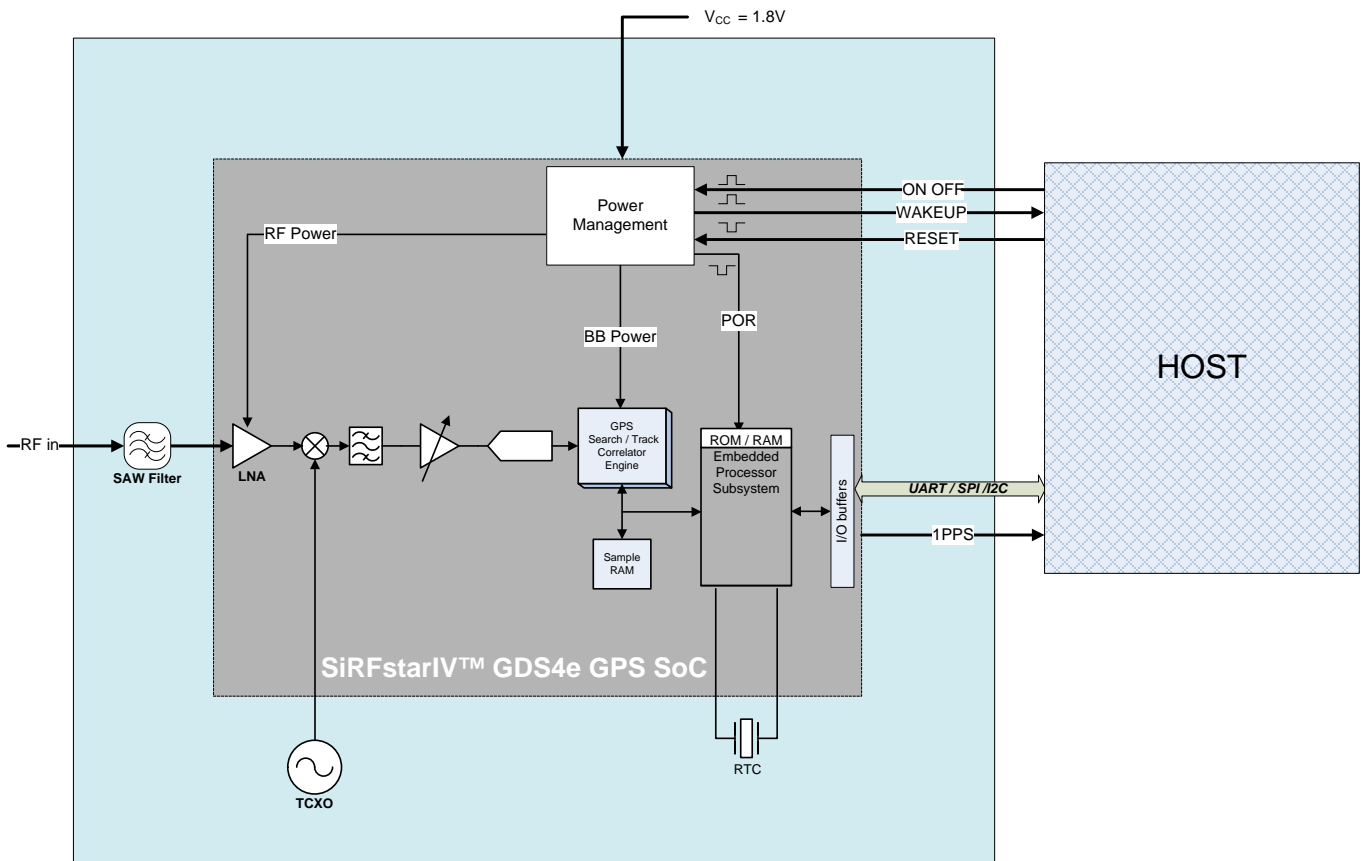


FIGURE 1 – ORG4475 ARCHITECTURE

+ SAW Filter

Band-Pass SAW filter eliminates out-of-band signals that may interfere to GPS reception. SAW filter is optimized for low insertion-loss in GPS band and low return-loss outside it.

+ LNA

Integrated LNA amplifies GPS signals to meet RF down converter input threshold. Noise Figure optimized design was implemented to provide maximum sensitivity.

+ TCXO

Highly stable 16.369 MHz oscillator controls the down conversion process in RF block of the GPS SoC. Characteristics of this component are important factors for higher sensitivity, shorter TTFF and better navigation stability.

+ RTC crystal

Tuning fork 32.768 KHz quartz crystal with very tight specifications is necessary for maintaining Hot Start and Warm Start capabilities of the module.

+ RF Shield

RF enclosure avoids external interference from compromising sensitive circuitry inside the module. RF shield also blocks module's internal high frequency emissions from being radiated.

+ SiRFstarIV™ GSD4e GPS SoC

SiRFstarIV™ GSD4e is full SoC built on a low-power RF CMOS single-die, incorporating GPS RF, baseband, integrated navigation solution software and ARM® processor.

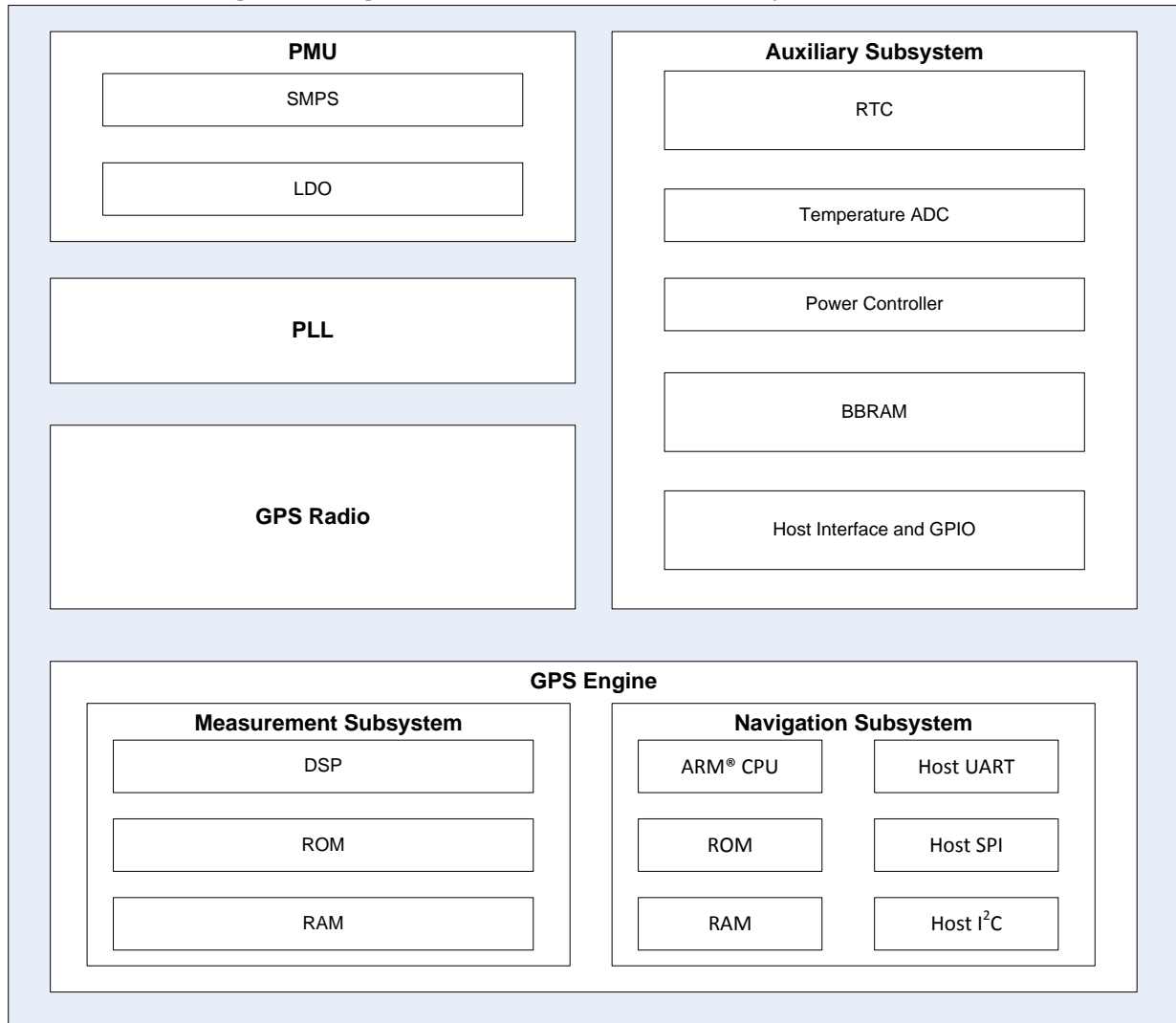


FIGURE 2 – SiRFstarIV™ GSD4e GPS SoC BLOCK DIAGRAM

SiRFstarIV™ GSD4e SoC includes the following units:

- + GPS radio subsystem containing LNA, harmonic-reject double balanced mixer, fractional-N synthesizer, integrated self-calibrating filters, IF VGA with AGC, high-sample rate ADCs with adaptive dynamic range.
- + Measurement subsystem including DSP core for GPS signals acquisition and tracking, interference scanner and detector, wideband and narrowband interference removers, multipath and cross-correlation detectors, dedicated DSP code ROM and DSP cache RAM. Measurement subsystem interfaces GPS radio subsystem.
- + Navigation subsystem comprising ARM7® microprocessor system for position, velocity and time solution, program ROM, data RAM, cache and patch RAM, host interface UART, SPI and I²C drivers. Navigation subsystem interfaces measurement subsystem.
- + Auxiliary subsystem containing RTC block and health monitor, temperature sensor for reference clock compensation, battery-backed SRAM for satellite data storage, voltage supervisor with POR, PLL controller, GPIO controller, 48-bit RTC timer and alarms, CPU watchdog monitor. Auxiliary subsystem interfaces navigation subsystem, PLL and PMU subsystems.
- + PMU subsystem containing voltage regulators for RF and baseband domains.



13. ELECTRICAL SPECIFICATIONS

13.1. ABSOLUTE MAXIMUM RATINGS

Stresses exceeding Absolute Maximum Ratings may damage the device.

PARAMETER		SYMBOL	MIN	MAX	UNIT	
Power Supply Voltage		V_{CC}	-0.30	+2.20	V	
Power Supply Current ¹		I_{CC}		100	mA	
RF Input Voltage		V_{RF}	-10	+10	V	
I/O Voltage		V_{IO}	-0.30	+3.65	V	
I/O Source/Sink Current		I_{IO}	-4	+4	mA	
ESD Rating	I/O pads	HBM ² method	$V_{IO(ESD)}$	-2000	+2000	V
		CDM ³ method		-400	+400	V
	RF input pad	HBM ² method	$V_{RF(ESD)}$	-500	+500	V
		CDM ³ method		-100	+100	V
RF Input Power	$f_{IN} = 1560\text{MHz} \div 1590\text{MHz}$	P_{RF}		+10	dBm	
	$f_{IN} < 1560\text{MHz}, > 1590\text{MHz}$			+30	dBm	
Power Dissipation		P_D		220	mW	
Operating Temperature		T_{AMB}	-45	+90	°C	
Storage Temperature		T_{ST}	-55	+150	°C	
Lead Temperature ⁴		T_{LEAD}		+260	°C	

TABLE 3 – ABSOLUTE MAXIMUM RATINGS

Notes:

1. Inrush current of up to 100mA for about 20μs duration.
2. Human Body Model (HBM) contact discharge per EIA/JEDEC JESD22-A114D.
3. Charged Device Model (CDM) contact discharge per EIA/JEDEC JESD22-C101.
4. Lead temperature at 1mm from case for 10s duration.

13.2. RECOMMENDED OPERATING CONDITIONS

Exposure to stresses above the Recommended Operating Conditions may affect device reliability.

PARAMETER	SYMBOL	MODE / PAD	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power supply voltage	V_{CC}	V_{CC}		+1.71	+1.80	+1.89	V
Power Supply Current ¹	I_{CC}	Acquisition		37	40	43	mA
		Tracking		5		33	mA
		ATP™ Tracking ²			5		mA
		CPU only ³			14		mA
		Standby ³			90		μA
		MPM™ ⁴			125		μA
		Hibernate		9	14	15	μA
Input Voltage Low State	V_{IL}	GPIO		-0.40		+0.45	V
Input Voltage High State	V_{IH}			$0.70 \cdot V_{CC}$		+3.60	V
Output Voltage Low State	V_{OL}		$I_{OL} = 2\text{mA}$			+0.40	V
Output Voltage High State	V_{OH}		$I_{OH} = -2\text{mA}$	$0.75 \cdot V_{CC}$			V
Input Capacitance	C_{IN}				5		pF
Internal Pull-up Resistor	R_{PU}			50	86	157	kΩ
Internal Pull-down Resistor	R_{PD}			51	91	180	kΩ
Input Leakage Current	$I_{IN(leak)}$		$V_{IN} = 1.8\text{V or }0\text{V}$	-10		+10	μA
Output Leakage Current	$I_{OUT(leak)}$		$V_{OUT} = 1.8\text{V or }0\text{V}$	-10		+10	μA
Input Impedance	Z_{IN}		RF Input	$f_{IN} = 1575.5\text{MHz}$		50	
Input Return Loss	R_{LIN}				-8		dB
Input Power Range	P_{IN}	-165				-110	dBm
Input Frequency Range	f_{IN}				1575.42		MHz
Operating Temperature ⁵	T_{AMB}			-40	+25	+85	°C
Storage Temperature	T_{ST}			-55	+25	+125	°C
Relative Humidity	RH		T_{AMB}	5		95	%

TABLE 4 – RECOMMENDED OPERATING CONDITIONS

Notes:

1. Typical I_{CC} values are under signal conditions of -130dBm and ambient temperature of +25°C.
2. Adaptive Trickle Power (ATP™) mode 100:1.
3. Transitional states of ATP™ power saving mode.
4. Average current during SiRFaware™ Micro Power Mode (MPM™) with valid satellite ephemeris data.
5. Longer TTF is expected while operating below -30°C to -40°C.



14. PERFORMANCE

14.1. ACQUISITION TIME

TTFF (Time To First Fix) – is the period of time from the module’s power-up till position estimation.

14.1.1. HOT START

Hot Start results either from a software reset after a period of continuous navigation or a return from a short idle period that was preceded by a period of continuous navigation.

During Hot Start all critical data (position, velocity, time, and satellite ephemeris) is valid to the specified accuracy and available in RAM.

14.1.2. WARM START

Warm Start typically results from user-supplied position and time initialization data or continuous RTC operation with an accurate last known position available in RAM.

In this state position and time data are present and valid, but satellite ephemeris data validity has expired.

14.1.3. COLD START

Cold Start occurs when satellite ephemeris data, position and time data are unknown.

14.1.4. AIDED START

Aided Start is a method of effectively reducing TTFF by making every start Hot or Warm.

OPERATION ¹	VALUE	UNIT
Hot Start	< 1	s
Aided Start	< 10	s
Warm Start	< 32	s
Cold Start	< 35	s
Signal Reacquisition	< 1	s

TABLE 5 – ACQUISITION TIME

14.2. SENSITIVITY

OPERATION	VALUE	UNIT
Tracking	-163	dBm
Navigation	-161	dBm
Aided Start	-156	dBm
Cold Start	-148	dBm

TABLE 6 – SENSITIVITY

Notes:

1. Module is static under signal conditions of -130dBm and ambient temperature of +25°C.



14.3. ACCURACY

PARAMETER		FORMAT	MODE	VALUE	UNIT
Position ¹	Horizontal	CEP (50%)	GPS + SBAS	< 2.0	m
			GPS	< 2.5	m
		2dRMS (95%)	GPS + SBAS	< 4.0	m
			GPS	< 5.0	m
	Vertical	VEP (50%)	GPS + SBAS	< 3.5	m
			GPS	< 4.0	m
		2dRMS (95%)	GPS + SBAS	< 6.5	m
			GPS	< 7.5	m
Velocity ²	over ground	50% of samples		< 0.01	m/s
Heading	to north	50% of samples		< 0.01	°
Time ¹		RMS jitter	1 PPS	≤ 30	ns

TABLE 7 – ACCURACY

14.4. DYNAMIC CONSTRAINS

PARAMETER ³	MAXIMUM	
Velocity	515 m/s	1,000 knots
Acceleration	4g	
Altitude	18,288 m	60,000 ft.

TABLE 8 – DYNAMIC CONSTRAINS

Notes:

1. Module is 24-hrs. static under signal conditions of -130dBm and ambient temperature of +25°C.
2. Speed over ground ≤ 30m/s.
3. Standard dynamic constrains according to regulatory limitations.



15. POWER MANAGEMENT

15.1. POWER CONSUMPTION

OPERATION	VALUE	UNIT
Acquisition	72	mW
Tracking	59	mW
Low Power Tracking – ATP™ 100ms Full Power : 1s tracking	9	mW
Basic Power saving mode – 5min. Hibernate : 10s tracking	1.9	mW
Hibernate	25	μW

TABLE 9 – POWER CONSUMPTION

15.2. POWER STATES

15.2.1. FULL POWER ACQUISITION

ORG4475 module stays in Full Power Acquisition state until a reliable position solution is made.

15.2.2. FULL POWER TRACKING

Full Power Tracking state is entered after a reliable position solution is achieved.

During this state the processing is less intense compared to Full Power Acquisition, therefore power consumption is lower. Full Power Tracking state with navigation update rate at 5Hz consumes more power compared to default 1Hz navigation.

15.2.3. CPU ONLY

CPU Only is the transitional state of ATP™ power saving mode when the RF and DSP sections are partially powered off. This state is entered when the satellites measurements have been acquired, but navigation solution still needs to be computed.

15.2.4. STANDBY

Standby is the transitional state of ATP™ power saving mode when RF and DSP sections are completely powered off and baseband clock is stopped.

15.2.5. HIBERNATE

ORG4475 module boots into Hibernate state after power supply applied, drawing only 9μA. When Hibernate state is following Full Power Tracking state current consumption is about 14μA. During this state RF, DSP and baseband sections are completely powered off leaving only RTC and Battery-Backed RAM running.

Module will perform Hot Start if stayed in Hibernate state less than 4 hours from last valid position solution.

15.3. BASIC POWER SAVING MODE

Basic power saving mode is elaborating host in straightforward way for controlling transfers between Full Power and Hibernate states.

Current profile of this mode has no hidden cycles of satellite data refresh.

Host may condition transfers by tracking duration, accuracy, satellites in-view or other parameters.

15.4. SELF MANAGED POWER SAVING MODES

Micro Spider module has several self-managed power saving modes tailored for different use cases. These modes provide several levels of power saving with degradation level of position accuracy. Initial operation in Full Power state is a prerequisite for accumulation of satellite data determining location, fine time and calibration of reference clocks.

15.4.1. ADAPTIVE TRICKLE POWER (ATP™)

ATP™ is best suited for applications that require navigation solutions at a fixed rate as well as low power consumption and an ability to track weak signals.

This power saving mode provides the most accurate position among self-managed modes.

In this mode module is intelligently cycled between Full Power state, CPU Only state consuming 14mA and Standby state consuming 90µA, therefore optimizing current profile for low power operation.

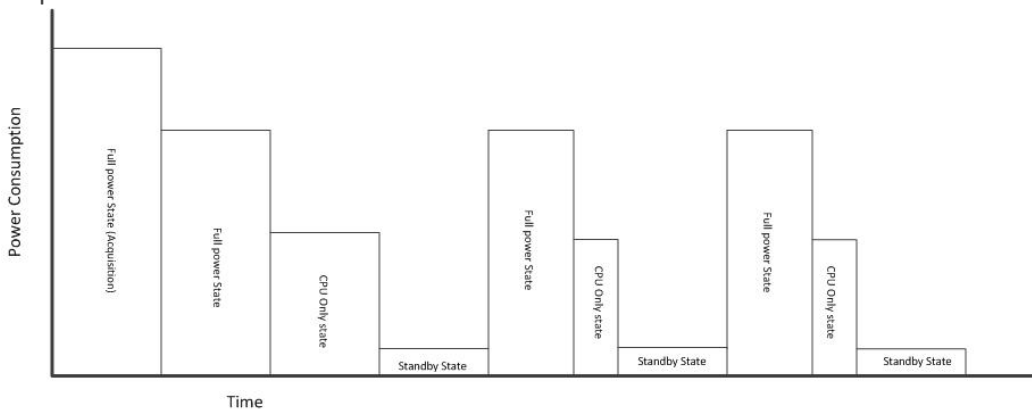


FIGURE 3 – ATP™ TIMING

15.4.2. PUSH TO FIX (PTF™)

PTF™ is best suited for applications that require infrequent navigation solutions.

In this mode ORG4475 module is mostly in Hibernate state, drawing < 15µA of current, waking up for satellite ephemeris data refresh in fixed periods of time.

PTF™ period can be anywhere between 10 seconds and 2 hours.

Host can initiate an instant position report by toggle the ON_OFF pad to wake up the module.

During fix trial ORG4475 will stay in Full Power state until good position solution is estimated or pre-configured timeout for it has expired.

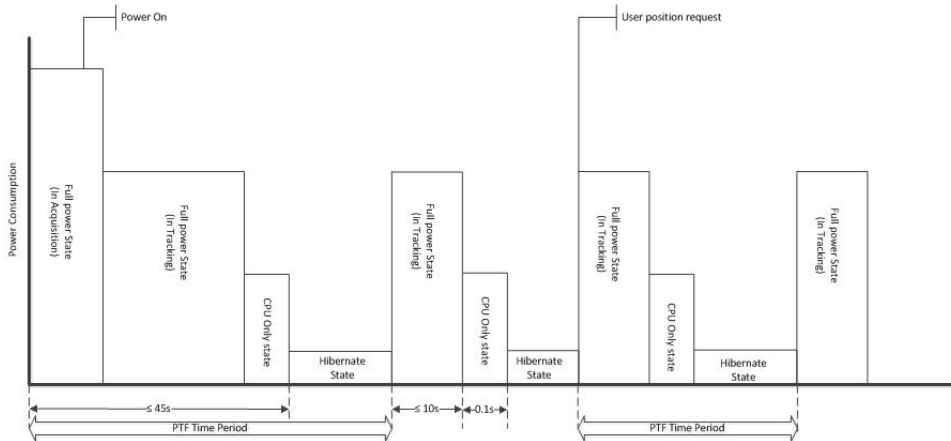


FIGURE 4 – PTF™ TIMING

15.4.3. ADVANCED POWER MANAGEMENT (APM™)

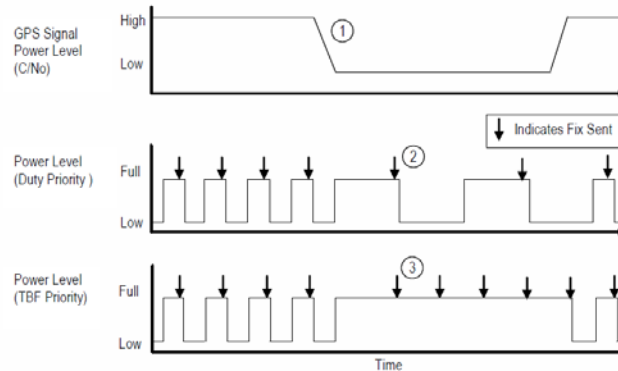
APM™ allows power savings while ensuring that the **Quality of the Solution (QoS)** is maintained when signals level drop.

In APM™ mode the module is intelligently cycled between Full Power and Hibernate states. In addition to setting the position report interval, a QoS specification is available that sets allowable error estimates and selects priorities between position report interval and more power saving.

The user may select between Duty Cycle Priority for more power saving and **Time Between Fixes (TBF)** priority with defined or undefined maximum horizontal error.

TBF range is from 10s to 180s between fixes, Power Duty Cycle range is between 5% to 100%. Maximum position error is configurable between 1 to 160m.

The number of APM™ fixes is configurable up to 255 or set to continuous.



1. GPS signal level drops (e.g. user walks indoors)
2. Lower signal results in longer ON time. To maintain Duty Cycle Priority, OFF time is increased.
3. Lower signal means missed fix. To maintain future TBFs, the module goes into Full Power state until signal levels improve.

FIGURE 5 – APM™ TIMING

15.4.4. SiRFAWARE™ MICRO POWER MODE (MPM™)

While in SiRFAware™ MPM the module determines how much signal processing to do and how often to do it, so that the module is always able to do a fast hot start (TTFF < 2 s) on demand.

ORG4475 will wake up (typically twice an hour) for 18-24s to collect new ephemeris data. Ephemeris data collection operation consumes power equal to Full Power state.

Additionally, ORG4475 will wake up once every 1 to 10 minutes for 250ms to update internal navigation state and clocks calibration. Capture/Update operation consumes about 0.2mA, rest of time ORG4475 stays in Hibernate state, drawing 14µA.

Host toggles ON_OFF to wake-up the module and initiates fix trial.

After valid fix is available, the host can turn the module back into MPM™ by re-sending the command.

Average current consumption over long period during MPM™ is about 125µA.

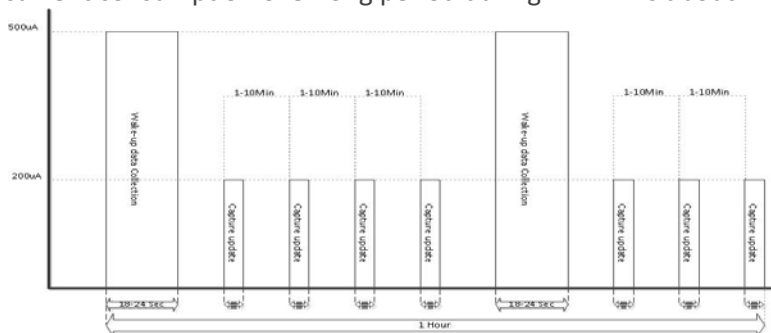


FIGURE 6 – MPM™ TIMING



16. EXTENDED FEATURES

16.1. ALMANAC BASED POSITIONING (ABP™)

With ABP™ mode enabled, the user can get shorter Cold Start TTFF as tradeoff with position accuracy. When no sufficient ephemeris data is available to calculate an accurate solution, a coarse solution will be provided where the position is calculated based on one or more of the GPS satellites, having their states derived from the almanac data.

Data source for ABP™ may be either stored factory almanac, broadcasted or pushed almanac.

16.2. ACTIVE JAMMER DETECTOR AND REMOVER

Jamming Detector is embedded DSP software that detects interference signals in GPS L1 band.

Jamming Remover is another DPS software that sort-out Jamming Detector output mitigating up to 8 interference signals of Continuous Wave (CW) type up to 80dB-Hz each.

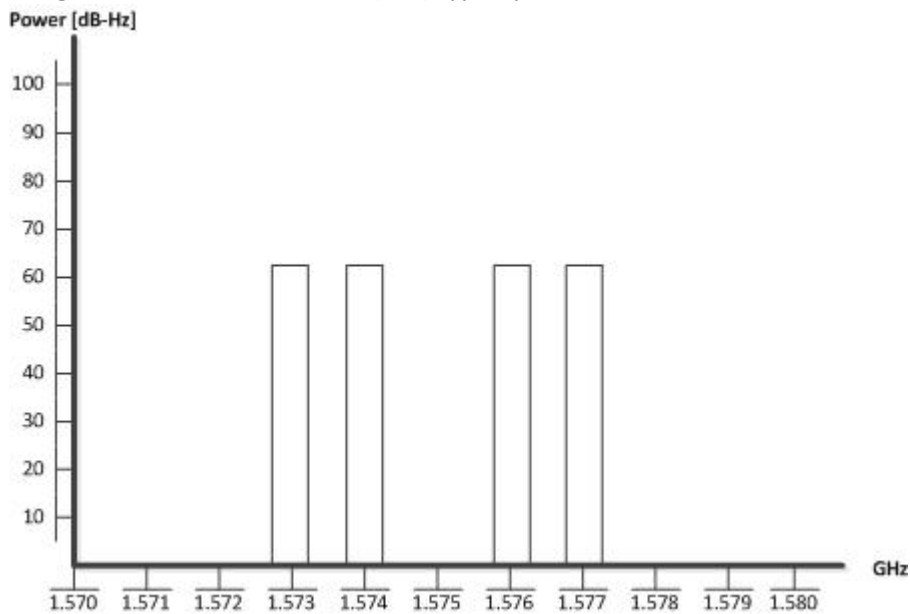


FIGURE 7 – ACTIVE JAMMER DETECTOR FREQUENCY PLOT

16.3. CLIENT GENERATED EXTENDED EPHEMERIS (CGEE™)

CGEE™ feature allows shorter TTFFs by providing predicted (synthetic) ephemeris files created within a lost host system from previously received satellite ephemeris data.

The prediction process requires good receipt of broadcast ephemeris data for all satellites.

EE files created this way are good for up to 3 days and then expire.

CGEE™ feature requires avoidance of power supply removal.

CGEE™ data files are stored and managed by host.

16.4. SERVER GENERATED EXTENDED EPHEMERIS (SGEE™)

SGEE™ enables shorter TTFFs by fetching Extended Ephemeris (EE) file downloaded from web server.

Host is initiating periodic network sessions of EE file downloads, storage and provision to module.

There is an SOW based one-time NRE charge for set-up, access to OriginGPS EE distribution server and end-end testing for re-distribution purposes, or there is a per-unit charge for each module within direct SGEE™ deployment.

EE files are provided with look-ahead of 1, 3, 7, 14 or 31 days.



17. INTERFACE

17.1. PAD ASSIGNMENT

PAD	NAME	FUNCTION			DIRECTION
1	GND	System Ground			Power
2	WAKEUP	Power Status			Output
3	$\overline{\text{CTS}}$	Interface Select 1	UART Clear To Send	SPI Clock	Bi-directional
4	V _{CC}	System Power			Power
5	$\overline{\text{RESET}}$	Asynchronous Reset			Input
6	$\overline{\text{RTS}}$	Interface Select 2	UART Ready To Send	SPI Chip Select	Bi-directional
7	RX	UART Receive	SPI Data In	I ² C Data	Bi-directional
8	GND	System Ground			Power
9	1PPS	UTC Time Mark			Output
10	ON_OFF	Power State Control			Input
11	NC	Not Connected			
12	GND	System Ground			Power
13	NC	Not Connected			
14	TX	UART Transmit	SPI Data Out	I ² C Clock	Bi-directional
15	NC	Not Connected			
16	NC	Not Connected			
17	GND	RF Ground			Power
18	RF_IN	Antenna Signal Input			Analog Input
19	GND	RF Ground			Power

TABLE 10 – PIN-OUT

BOTTOM VIEW

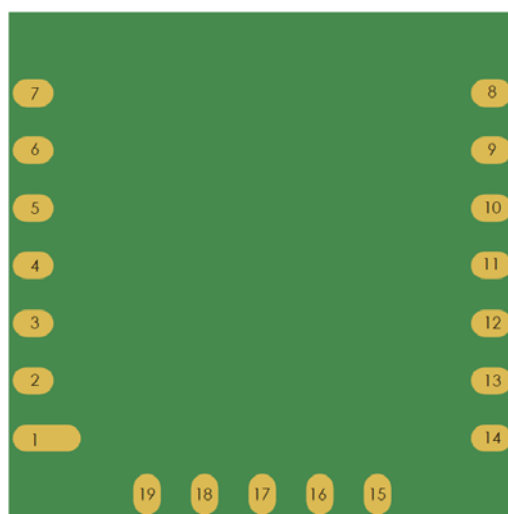


FIGURE 8 – PAD ASSIGNMENT



17.2. POWER SUPPLY

It is recommended to keep the power supply on all the time in order to maintain RTC block active and keep satellite data in RAM for fastest possible TTFF.

When V_{CC} is removed settings are reset to factory default and the receiver performs Cold Start on next power up.

17.2.1. V_{CC}

V_{CC} is 1.8V \pm 5% DC and must be provided from regulated power supply.

Typical I_{CC} is 40mA during acquisition.

Inrush current can be up to 100mA for about 20 μ s duration, whilst VCC can drop down to 1.7V.

Maximum I_{CC} current in Hibernate state is 15 μ A, while all I/O lines externally held in Hi-Z state.

Output capacitors are critical when powering module from switch-mode power supply.

Filtering is important to manage high alternating current flows on the power input connection.

An additional LC filter on module power input may be needed to reduce system noise.

The high rate of module input current change requires low ESR bypass capacitors.

Additional higher ESR output capacitors can provide input stability damping.

The ESR and size of the output capacitors directly define the output ripple voltage with a given inductor size. Large low ESR output capacitors are beneficial for low noise.

Voltage ripple below 50mV_{p-p} is allowed for frequencies between 100KHz to 1MHz.

Voltage ripple below 15mV_{p-p} is allowed for frequencies above 1MHz.

Voltage ripple higher than allowed may compromise sensitivity parameter.

17.2.2. GROUND

Ground pads must be connected to host PCB Ground with shortest possible traces or vias.

17.3. RF INPUT

RF input impedance is 50 Ω , DC blocked up to 10V.

Micro Spider ORG4475 module supports active or passive antenna.

17.3.1. PASSIVE ANTENNA

In design with passive antenna attention should be paid on antenna layout.

Short trace of 50 Ω controlled impedance should conduct GPS signal from antenna to RF_IN pad.

Micro Spider ORG4475 is designed to track GPS signal levels in a range down to close to the thermal noise floor. At low signal levels, control of external noise sources is a significant factor in achieving the best performance of the receiver.

Designing with passive antenna require RF layout skills and can be challenging.

17.3.2. ACTIVE ANTENNA

Active antenna net gain including conduction losses should not exceed +25dB.

DC bias voltage for active antenna can be externally applied on RF_IN trace through bias-T.

DC bias voltage can be controlled by WAKEUP output through MOSFET or load switch.

17.4. CONTROL INTERFACE

17.4.1. ON_OFF

ON_OFF input is used to switch ORG4475 between different power states:

- While in Hibernate state, ON_OFF pulse will initiate transfer into Full Power state.
- While in ATP™ mode, ON_OFF pulse will initiate transfer into Full Power state.
- While in PTF™ mode, ON_OFF pulse will initiate one PTF™ request.
- While in Full Power state, ON_OFF pulse will initiate orderly shutdown into Hibernate state.

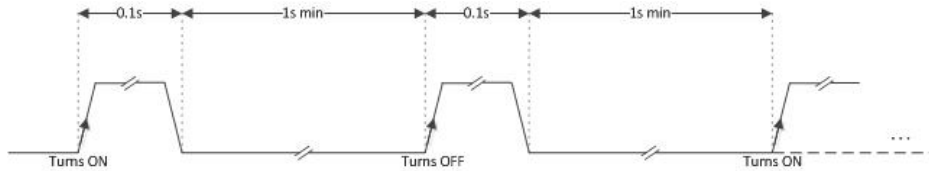


FIGURE 9 – ON_OFF TIMING

ON_OFF detector set requires a rising edge and high logic level that persists for at least 100μs.

ON_OFF detector reset requires ON_OFF asserted to low logic level for at least 100μs.

Recommended ON_OFF Low-High-Low pulse length is 100ms.

ON_OFF pulses with less than 1s intervals are not recommended.

Multiple switch bounce pulses are recommended to be filtered out.

Pull-down resistor of 10kΩ-33kΩ is recommended to avoid accidental power mode change.

ON_OFF input is tolerable up to 3.6V.

Do not drive high permanently or pull-up this input.

This line must be connected to host.

17.4.2. WAKEUP

WAKEUP output from ORG4475 is used to indicate power state.

A low logic level indicates that the module is in one of its low-power states - Hibernate or Standby. A high logic level indicates that the module is in Full Power state.

In addition WAKEUP output can be used to control auxiliary devices, like Enable of external LNA or Load Switch of active antenna DC bias.

Wakeup output is LVCMOS 1.8V compatible.

Do not connect if not in use.

17.4.3. RESET

Power-on-Reset (POR) sequence is generated internally.

In addition, external reset is available through $\overline{\text{RESET}}$ pad.

Resetting ORG4475 clears the state machine of self-managed power saving modes to default.

$\overline{\text{RESET}}$ signal should be applied for at least 1μs.

$\overline{\text{RESET}}$ input is active low and has internal pull-up resistor of 86kΩ to internal 1.2V domain.

Do not drive this input high.

Do not connect if not in use.

17.4.4. 1PPS

Pulse-Per-Second (PPS) output provides a pulse signal for timing purposes.

PPS output starts when position solution has been obtained using 5 or more GPS satellites.

PPS output stops when 3D position solution is lost.

Pulse length (high state) is 200ms with rising edge is less than 30ns synchronized to UTC epoch.

The correspondent UTC time message is generated and put into output FIFO 300ms after the PPS signal. The exact time between PPS and UTC time message delivery depends on message rate, message queue and communication baud rate.

1PPS output is LVCMOS 1.8V compatible.

1PPS output is LVCMOS 1.8V compatible.

Do not connect if not in use.



17.5. DATA INTERFACE

ORG4475 module has 3 types of interface ports to connect to host - UART, SPI or I²C – all multiplexed on a shared set of pads. At system reset host port interface lines are disabled, so no conflict occurs.

Logic values on $\overline{\text{CTS}}$ and $\overline{\text{RTS}}$ are read by the module during startup and define host port type.

External resistor of 10k Ω is recommended. Pull-up resistor is referenced to 1.8V.

PORT TYPE	$\overline{\text{CTS}}$	$\overline{\text{RTS}}$
UART	External pull-up	Internal pull-up
SPI (default)	Internal pull-down	Internal pull-up
I ² C	Internal pull-down	External pull-down

TABLE 11 – HOST INTERFACE SELECT

17.5.1. UART

UART host interface features are:

- TX used for GPS data reports. Output logic high voltage level is LVCMOS 1.8V compatible.
- RX used for receiver control. Input logic high voltage level is 1.45V, tolerable up to 3.6V.
- UART flow control using $\overline{\text{CTS}}$ and $\overline{\text{RTS}}$ lines is disabled by default.
Can be turned on by sending OSP Message ID 178, Sub ID 2 input command.

17.5.2. SPI

SPI host interface features are:

- Slave SPI Mode 1, supports clock up to 6.8MHz.
- RX and TX have independent 2-byte idle patterns of '0xA7 0xB4'.
- TX and RX each have independent 1024 byte FIFO buffers.
- TX FIFO is disabled when empty and transmits its idle pattern until re-enabled.
- RX FIFO detects a software specified number of idle pattern repeats and then disables FIFO input until the idle pattern is broken.
- FIFO buffers can generate an interrupt at any fill level.
- SPI detects synchronization errors and can be reset by software.
- Output is LVCMOS 1.8V compatible. Inputs are tolerable up to 3.6V.

17.5.3. I²C

I²C host interface features are:

- I²C Multi-Master Mode - module initiates clock and data, operating speed 400kbps.
- I²C address '0x60' for RX and '0x62' for TX.
- Individual transmit and receive FIFO length of 64 bytes.
- I²C host interface mode can be switched slave (Multi-master default), clock rate can be switched 100KHz (default 400KHz), address can be changed (default 0x62 for TX FIFO and 0x60 for RX FIFO) by sending OSP Message ID 178, Sub ID 2 input command.
- SCL and SDA are pseudo open-drain lines, therefore require external pull-up resistors of 2.2k Ω to 1.8V, or 3.3k Ω to 3.3V.

18. TYPICAL APPLICATION CIRCUIT

18.1. PASSIVE ANTENNA

Designing with passive antenna require RF layout skills and can be challenging.

Contact OriginGPS for application specific recommendations and design review services.

18.2. PASSIVE ANTENNA WITH EXTERNAL LNA

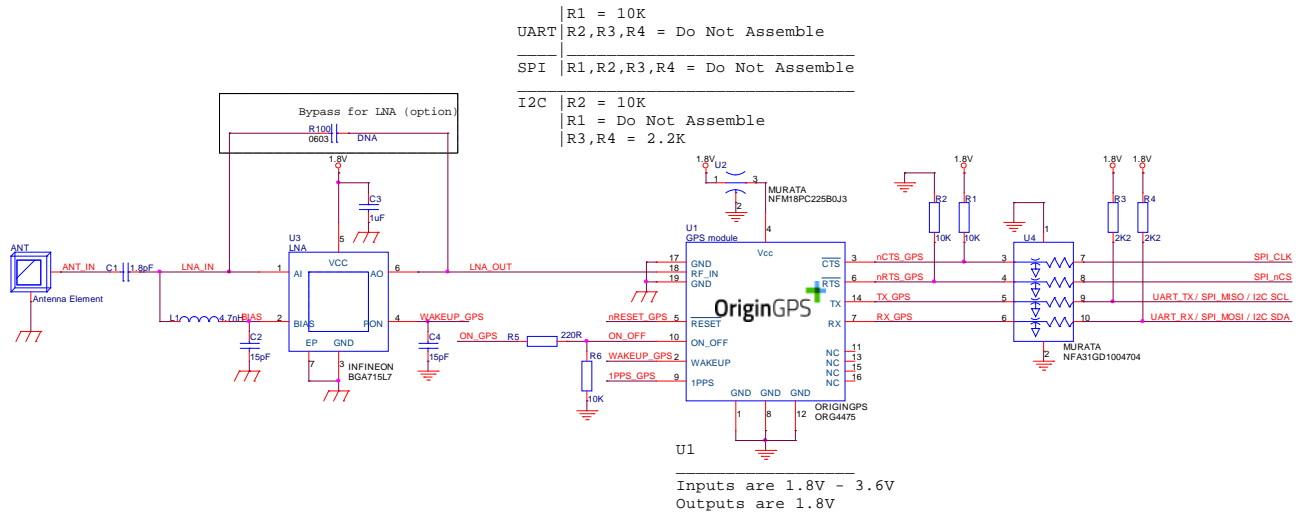


FIGURE 10 – SCHEMATIC DIAGRAM OF PASSIVE ANTENNA WITH EXTERNAL LNA

18.3. ACTIVE ANTENNA

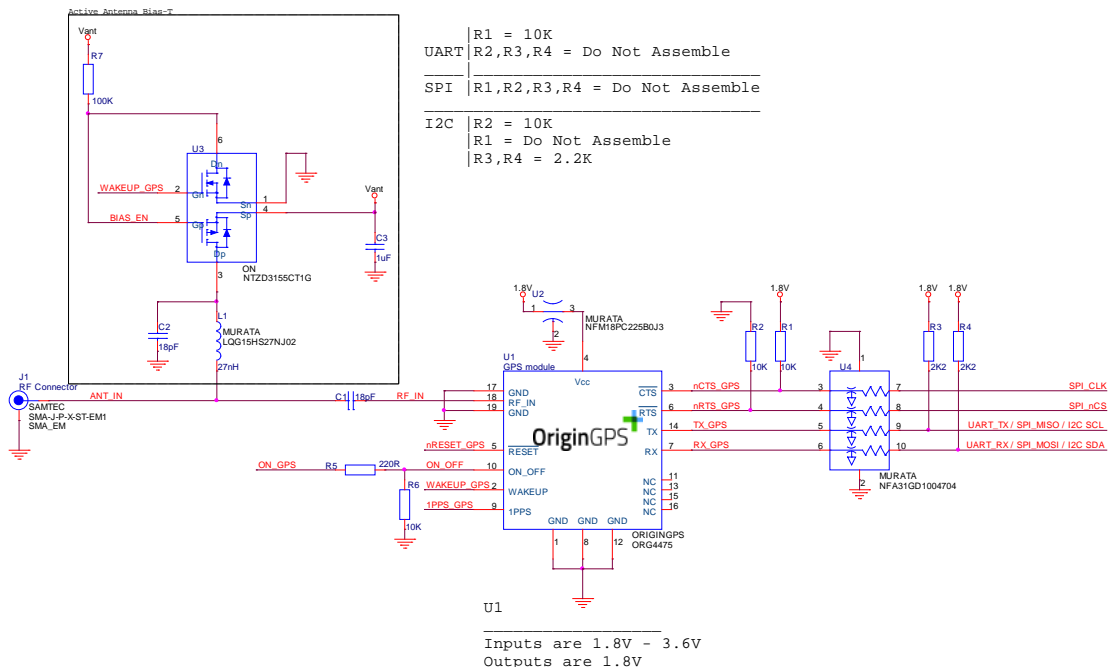


FIGURE 11 – SCHEMATIC DIAGRAM OF ACTIVE ANTENNA CONNECTION

18.4. ANTENNA SWITCH

Contact OriginGPS for Application Note covering dual-antenna (on-board and external) design combining RF switch with auto-sense, DC bias and short-circuit protection.

19. RECOMMENDED PCB LAYOUT

19.1. FOOTPRINT

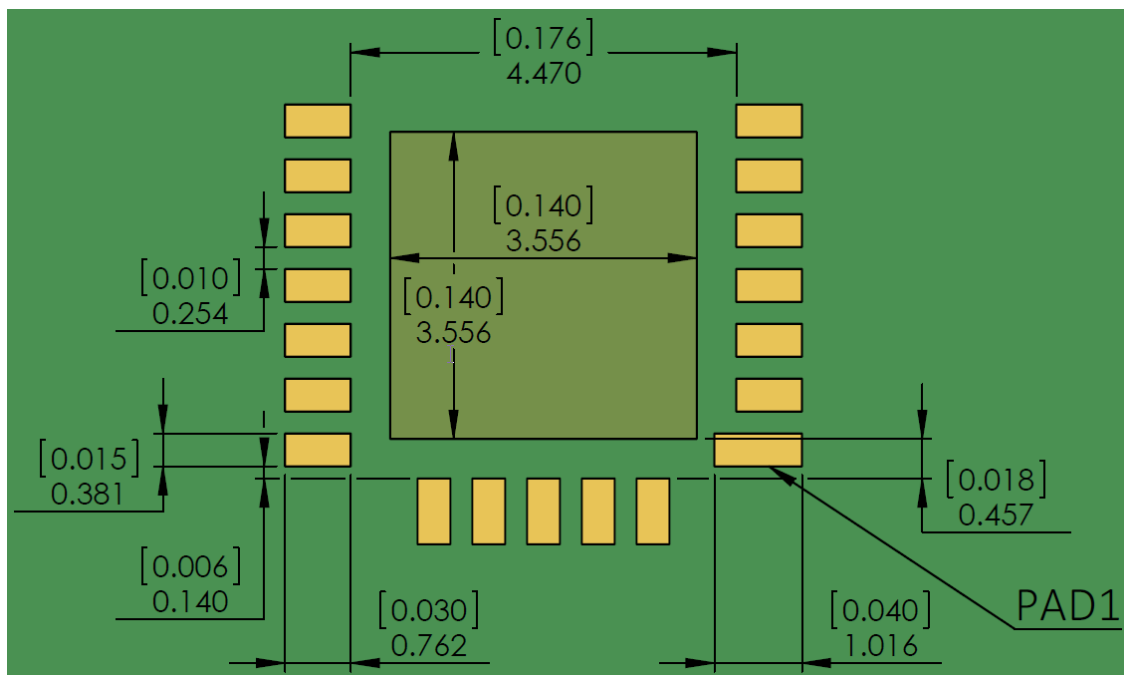


FIGURE 12 – FOOTPRINT

Ground paddle at the middle should be connected to main Ground plane by multiple vias.

Ground paddle at the middle must be solder masked.

Silk print of module's outline is highly recommended for SMT visual inspection.

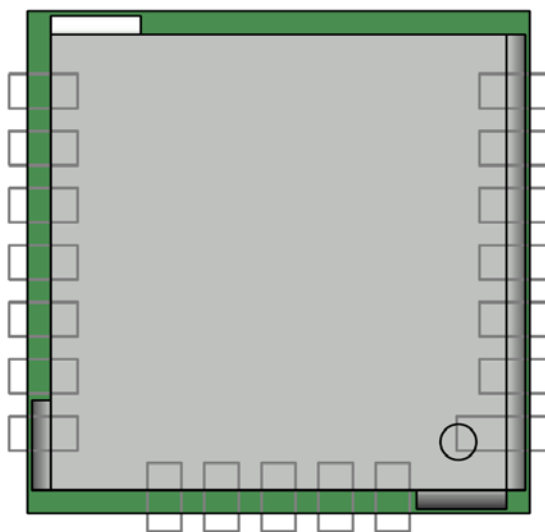


FIGURE 13 – MODULE HOSTED ON FOOTPRINT

19.2. HOST PCB

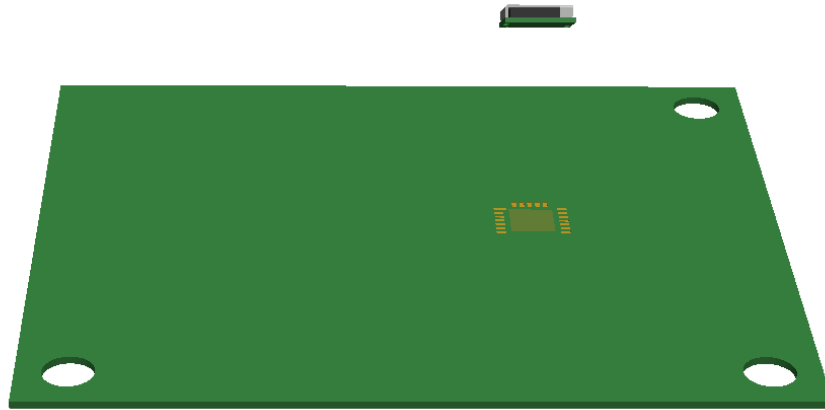


FIGURE 14 – HOST PCB

19.3. RF TRACE

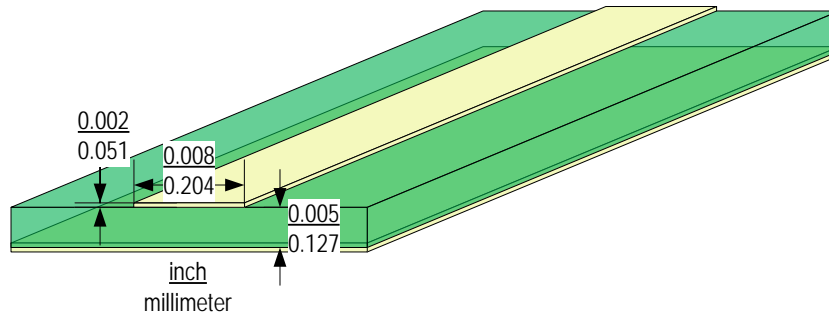


FIGURE 15 – TYPICAL MICROSTRIP PCB TRACE ON FR-4 SUBSTRATE

19.4. PCB STACK-UP

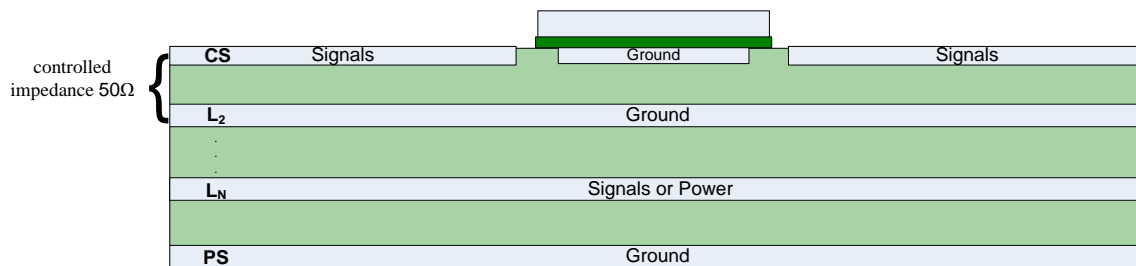


FIGURE 16 – TYPICAL PCB STACK-UP

19.5. PCB LAYOUT RESTRICTIONS

Switching and high-speed components, traces and vias must be kept away from ORG4475 module. Signal traces to/from module should have minimum length.

Recommended minimal distance from adjacent active components is 3mm.

Ground pads must be connected to host PCB Ground with shortest possible traces or vias.

In case of tight integration constrain or co-location with adjacent high speed components like CPU or memory, high frequency components like transmitters, clock resonators or oscillators, LCD panels or CMOS image sensors, contact OriginGPS for application specific recommendations.

20. DESIGN CONSIDERATIONS

ORG4475 operates with received signal levels down to -163dBm and can be affected by high absolute levels of RF signals, moderate levels of RF interference near the GPS bands and by low-levels of RF noise in the GPS band.

RF interference from nearby electronic circuits or radio transmitters can contain enough energy to desensitize ORG4475. These systems may also produce levels of energy outside of GPS band, high enough to leak through RF filters and degrade the operation of the radios in ORG4475.

This issue becomes more critical in small products, where there are industrial design constraints.

In that environment, transmitters for Wi-Fi, Bluetooth, RFID, cellular and other radios may have antennas physically close to the GPS antenna.

To prevent degraded performance of ORG4475, OriginGPS recommends performing EMI/jamming susceptibility tests for radiated and conducted noise on prototypes and assessing risks of other factors.

Antennas for GPS and GLONASS have a wider bandwidth than pure GPS antennas.

Some wideband antennas may not have a good axial ratio to block reflections of RHCP GPS and GLONASS signals. These antennas have lower rejection of multipath reflections and tend to degrade the overall performance of the receiver.

Designing with passive antenna require RF layout skills and can be challenging.

Contact OriginGPS for application specific recommendations and design review services.



21. OPERATION

When power is first applied, ORG4475 goes into a Hibernate state while integrated RTC starts and internal Finite State Machine (FSM) sequences through to “Ready-to-Start” state.

Host is not required to control external master nRESET since module’s internal reset circuitry handles detection of power application.

While in “Ready-to-Start” state, ORG4475 awaits a pulse to the ON_OFF input.

Since integrated RTC startup times are variable, host is required either to wait for a fixed interval or to monitor a short Low-High-Low pulse on WAKEUP output that indicates FSM “Ready-to-Start” state.

Another option is to repeat a pulse on the ON_OFF input every second until the module starts by either detecting a stable logic high level on WAKEUP output or neither generation of UART messages.

21.1. STARTING THE MODULE

A pulse on the ON_OFF input line when FSM is ready and in startup-ready state, Hibernate state, standby state, will command the module to start.

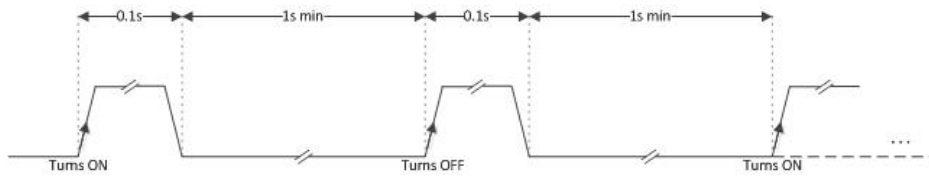


FIGURE 17 – ON_OFF TIMING

ON_OFF detector set requires a rising edge and high logic level that persists for at least 100 μ s. ON_OFF detector reset requires ON_OFF asserted to low logic level for at least 100 μ s.

Recommended ON_OFF Low-High-Low pulse length is 100ms.

ON_OFF pulses with less than 1s intervals are not recommended.

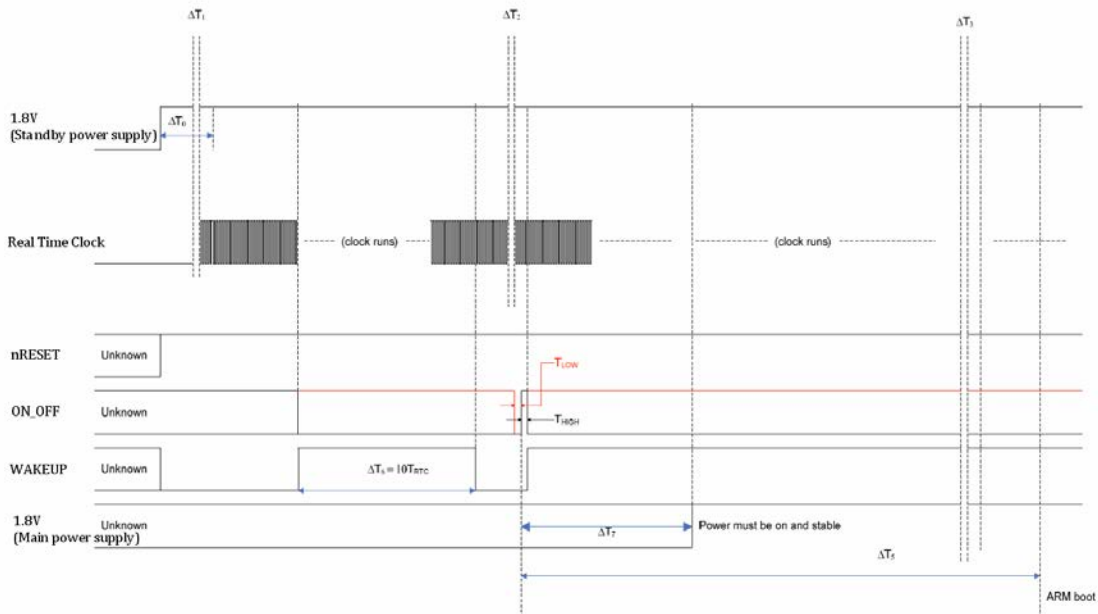


FIGURE 18 – START-UP TIMING

Note:

1. If power provided through dual supply, assign 1.8V LDO with low quiescent current for Hibernate state and 1.8V DC-DC with high efficiency for Full Power state.

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
f_{RTC}	RTC frequency	25°C	-20 ppm	32768	+20 ppm	Hz
t_{RTC}	RTC tick	25°C		30.5176		μ s
$\Delta T1$	RTC startup time			300		ms
$\Delta T0$	Power stabilization		$6 \cdot t_{RTC} + \Delta T1$	$7 \cdot t_{RTC} + \Delta T1$	$8 \cdot t_{RTC} + \Delta T1$	μ s
$\Delta T6$	WAKEUP pulse	RTC running		10		t_{RTC}
ΔT_{LOW}	ON_OFF low		3			t_{RTC}
ΔT_{HIGH}	ON_OFF high		3			t_{RTC}
$\Delta T3$	Startup sequencing	After ON_OFF		1024		t_{RTC}
-	ON_OFF to WAKEUP high	After ON_OFF		6		t_{RTC}
$\Delta T5$	ON_OFF to ARM start	After ON_OFF		2130		t_{RTC}
$\Delta T7$	Main power source start ¹	WAKEUP high	0	30	300	t_{RTC}

TABLE 12 – START-UP TIMING

21.2. AUTONOMOUS POWER ON

Connecting WAKEUP output (pad 2) to ON_OFF input (pad 10) enables self-start to Full Power state from Ready-To-Start state following boot process.

When host data interface is set UART, module will start autonomously transmitting NMEA messages after first power supply application. Further transfers between Full Power and Hibernate states require external logic circuitry combined with serial command.

21.3. VERIFYING THE MODULE HAS STARTED

WAKEUP output will go high indicating ORG4475 has started.

System activity indication depends upon selected serial interface.

The first message to come out of module is "OK_TO_SEND" - '\$PSRF150,1*3E'.

21.3.1. UART

When active, the module will output NMEA messages at the 4800bps.

21.3.2. I²C

In Multi-Master mode with no bus contention - the module will spontaneously send messages.

In Multi-Master mode with bus contention - the module will send messages after the I²C bus contention resolution process allows it to send.

21.3.3. SPI

Since ORG4475 is SPI slave device, there is no possible indication of system "ready" through SPI interface. Host must initiate SPI connection approximately 1s after WAKEUP output goes high.

21.4. SHUTTING DOWN THE MODULE

Transferring module from Full Power state to Hibernate state can be initiated in two ways:

- ✦ By a pulse on ON_OFF input.
- ✦ By NMEA (\$PSRF117) or OSP (MID205) serial message.

Orderly shutdown process may take anywhere from 10ms to 900ms to complete, depending upon operation in progress and messages pending, and hence is dependent upon serial interface speed and controls. Module will stay in Full Power state until TX FIFO buffer is emptied.

The last message during shutdown sequence is '\$PSRF150,0*3F'.



22. FIRMWARE

22.1. DEFAULT SETTINGS

Power On State	Hibernate	
Default Interface ¹	SPI	
SPI Data Format	NMEA	
UART Settings	4,800bps.	
UART Data Format	NMEA	
I ² C Settings	Multi-Master 400kbps	
I ² C Data Format	NMEA	
Satellite Constellation	GPS	
Default Output Messages	\$GPGGA @1 sec.	
	\$GPGSA @ 1 sec.	
	\$GPGSV @ 5 sec.	
	\$GPRMC @ 1 sec.	
Firmware Defaults	SBAS	OFF
	ABP™	OFF
	Static Navigation	OFF
	Track Smoothing	OFF
	Jammer Detector	ON
	Jammer Remover	OFF
	Fast Time Sync	OFF
	Pseudo DR Mode	ON
	Power Saving Mode	OFF
	3SV Solution Mode	ON
5Hz Update Rate	OFF	

TABLE 13 – DEFAULT FIRMWARE SETTINGS

Note:

1. Without external resistor straps on \overline{CTS} or \overline{RTS} .

22.2. FIRMWARE UPDATES

Firmware updates can be considered exclusively as patches on top of baseline ROM firmware. Those patch updates may be provided from time to time to address ROM firmware issues as a method of performance improvement. Typical patch file size is 24KB.

Host controller is initiating load and application of patch update by communicating module's Patch Manager software block allocating 16KB of memory space for patch and additional 8KB for cache. Patch updates are preserved until BBRAM is discarded.



23. HANDLING INFORMATION

23.1. MOISTURE SENSITIVITY

ORG4475 modules are MSL 3 designated devices according to IPC/JEDEC J-STD-033B standard.

Module in sample or bulk package should be baked prior to assembly at 125°C for 48 hours.

23.2. ASSEMBLY

The module supports automatic pick-and-place assembly and reflow soldering processes.

Reflow soldering of the module on the component side of the motherboard PCB according to standard IPC/JEDEC J-STD-020D for LGA SMD.

Suggested solder paste stencil is 5 mil to ensure sufficient solder volume.

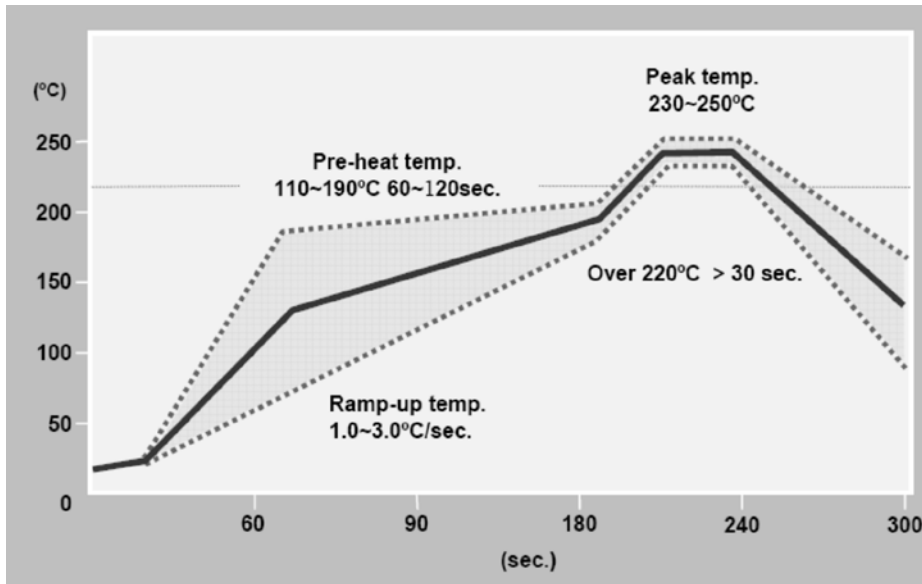


FIGURE 19 – RECOMMENDED SOLDERING PROFILE

Suggested peak reflow temperature is 250°C for 10 sec. for Pb-Free solder paste.

Absolute Maximum reflow temperature is 260°C for 10 sec.

23.3. REWORK

If localized heating is required to rework or repair the module, precautionary methods are required to avoid exposure to solder reflow temperatures that can result in permanent damage to the device.

23.4. ESD SENSITIVITY

This product is ESD sensitive device and must be handled with care.



23.5. SAFETY INFORMATION

Improper handling and use can cause permanent damage to the product.

Avoid cleaning process in ultrasonic degreaser, since ultrasonic vibrations may cause performance degradation or destruction of internal circuitry.

23.6. DISPOSAL INFORMATION

This product must not be treated as household waste.

For more detailed information about recycling electronic components contact your local waste management authority.



24. MECHANICAL SPECIFICATIONS

- + ORG4475 module has advanced ultra-miniature LGA SMD packaging sized 5.6mm x 5.6mm.
- + ORG4475 built on a PCB assembly enclosed with metallic RF shield box.
- + On bottom side there are 19 LGA SMT pads with Cu base and ENIG plating.
- + ORG4475 module supports automated pick and place assembly and reflow soldering processes.

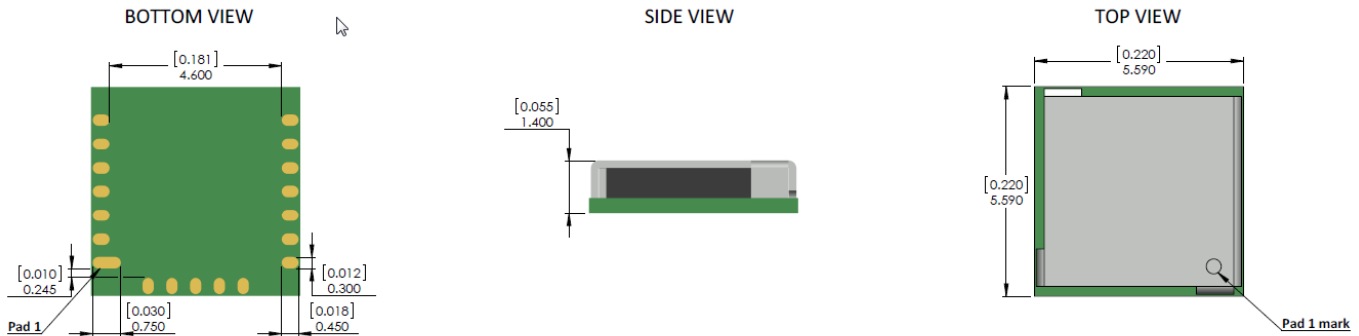


FIGURE 20 – MECHANICAL DRAWING

Dimensions	Length	Width	Height	Weight	
	mm	5.59 +0.10/ -0.05	5.59 +0.10/ -0.05	1.4 +0.1/ -0.0	gr
inch	0.220 +0.004/ -0.002	0.220 +0.004/ -0.002	0.055 +0.004/ -0.0	oz	0.004

TABLE 14 – MECHANICAL SUMMARY

25. COMPLIANCE

The following standards are applied on the production of ORG4475 modules:

- + IPC-6011/6012 Class2 for PCB manufacturing
- + IPC-A-600 Class2 for PCB inspection
- + IPC-A-610D Class2 for SMT acceptability

ORG4475 modules are manufactured in ISO 9001:2008 accredited facilities.

ORG4475 modules are manufactured in ISO 14001:2004 accredited facilities.

ORG4475 modules are manufactured in OHSAS 18001:2007 accredited facilities.

ORG4475 modules are designed, manufactured and handled in compliance with the Directive 2011/65/EU of the European Parliament and of the Council of June 2011 on the Restriction of the use of certain Hazardous Substances in electrical and electronic equipment, referred as RoHS II.

ORG4475 modules are manufactured and handled in compliance with the applicable substance bans as of Annex XVII of Regulation 1907/2006/EC on Registration, Evaluation, Authorization and Restriction of Chemicals including all amendments and candidate list issued by ECHA, referred as REACH.

ORG4475 modules comply with the following EMC standards:

- + EU CE EN55022:06+A1(07), Class B
- + US FCC 47CFR Part 15:09, Subpart B, Class B
- + JAPAN VCCI V-3/2006.04





26. PACKAGING AND DELIVERY

26.1. APPEARANCE

ORG4475 modules are delivered in reeled tapes for automatic pick and place assembly process.

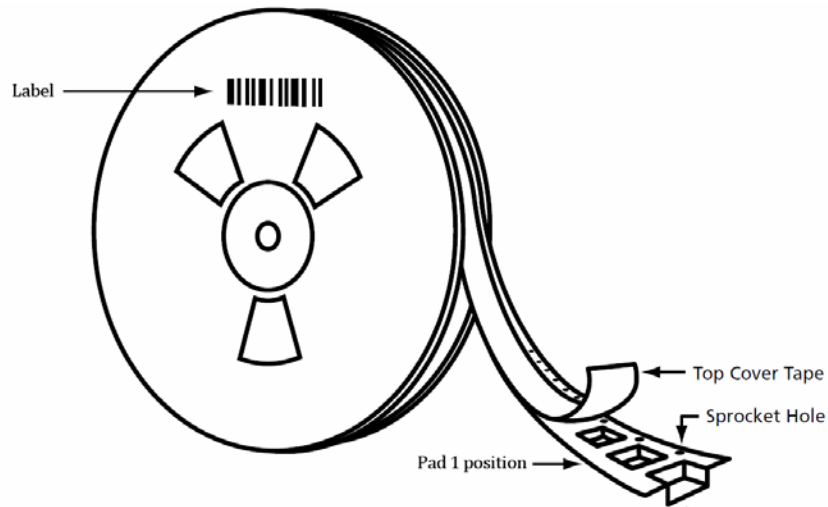


FIGURE 21 – MODULE POSITION

ORG4475 modules are packed in 2 different reel types.

SUFFIX	TR1	TR2
Quantity	500	2000

TABLE 15 – REEL QUANTITY

Reels are dry packed with humidity indicator card and desiccant bag according to IPC/JEDEC J-STD-033B standard for MSL 3 devices.

Reels are vacuum sealed inside anti-static moisture barrier bags.

Sealed reels are labeled with MSD sticker providing information about:

- + MSL
- + Shelf life
- + Reflow soldering peak temperature
- + Seal date

Sealed reels are packed inside cartons.

Reels, reel packs and cartons are labeled with sticker providing information about:

- + Description
- + Part number
- + Lot number
- + Customer PO number
- + Quantity
- + Date code



27. ORDERING INFORMATION

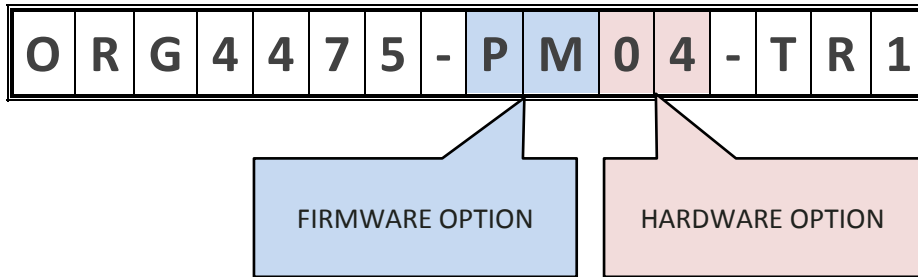


TABLE 18 – ORDERING OPTIONS

PART NUMBER	FIRMWARE VERSION	HARDWARE VARIANT	PACKAGING	SPQ
ORG4475-PM04-TR1	3	01	REELED TAPE	500
ORG4475-PM04-TR2	3	01	REELED TAPE	2000
ORG4475-PM04-UAR	3	01	EVALUATION KIT	1

TABLE 19 – ORDERABLE DEVICES