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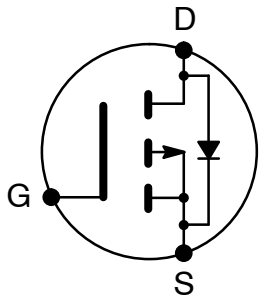
# NTE2391
# MOSFET
# P–Channel Enhancement Mode, High Speed Switch TO–220 Type Package

**Description:**

The NTE2391 is a P–Channel Enhancement Mode Power MOS Field Effect Transistor that utilizes advanced processing techniques to achieve extremely low on–resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

**Features:**

- Ultra Low On–Resistance
- Dynamic dv/dt Rating
- +175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated




**Absolute Maximum Ratings:**

Continuous Drain Current ($V_{GS}$ = –10V), $I_D$
- $T_C$ = +25°C . . . . . –40A
- $T_C$ = +100°C . . . . . –29A

Pulsed Drain Current (Note 1), $I_{DM}$ . . . . . –140A
Power Dissipation ($T_C$ = +25°C), $P_D$ . . . . . 200W
- Derate Above 25°C . . . . . 1.3W/°C

Gate–Source Voltage, $V_{GS}$ . . . . . ±20V
Single Pulse Avalanche Energy (Note 2), $E_{AS}$ . . . . . 780mJ
Avalanche Current (Note 1), $I_{AR}$ . . . . . –21A
Repetitive Avalanche Energy (Note 1), $E_{AR}$ . . . . . 20mJ
Peak Diode Recovery (Note 3), dv/dt . . . . . –5.0V/ns
Operating Junction Temperature Range, $T_J$ . . . . . –55° to +175°C
Storage Temperature Range, $T_{stg}$ . . . . . –55° to +175°C
Lead Temperature (During Soldering, 0.063 in. (1.6mm) from case, 10sec), $T_L$ . . . . . +300°C
Mounting Torque, 6–32 or M3 Screw . . . . . 10 lbf•in (1.1N•m)
Maximum Thermal Resistance, Junction–to–Case, $R_{thJC}$ . . . . . 0.75°C/W
Typical Thermal Resistance, Case–to–Sink, $R_{thCS}$ . . . . . 0.5°C/W
Maximum Thermal Resistance, Junction–to–Ambient, $R_{thJA}$ . . . . . 62°C/W

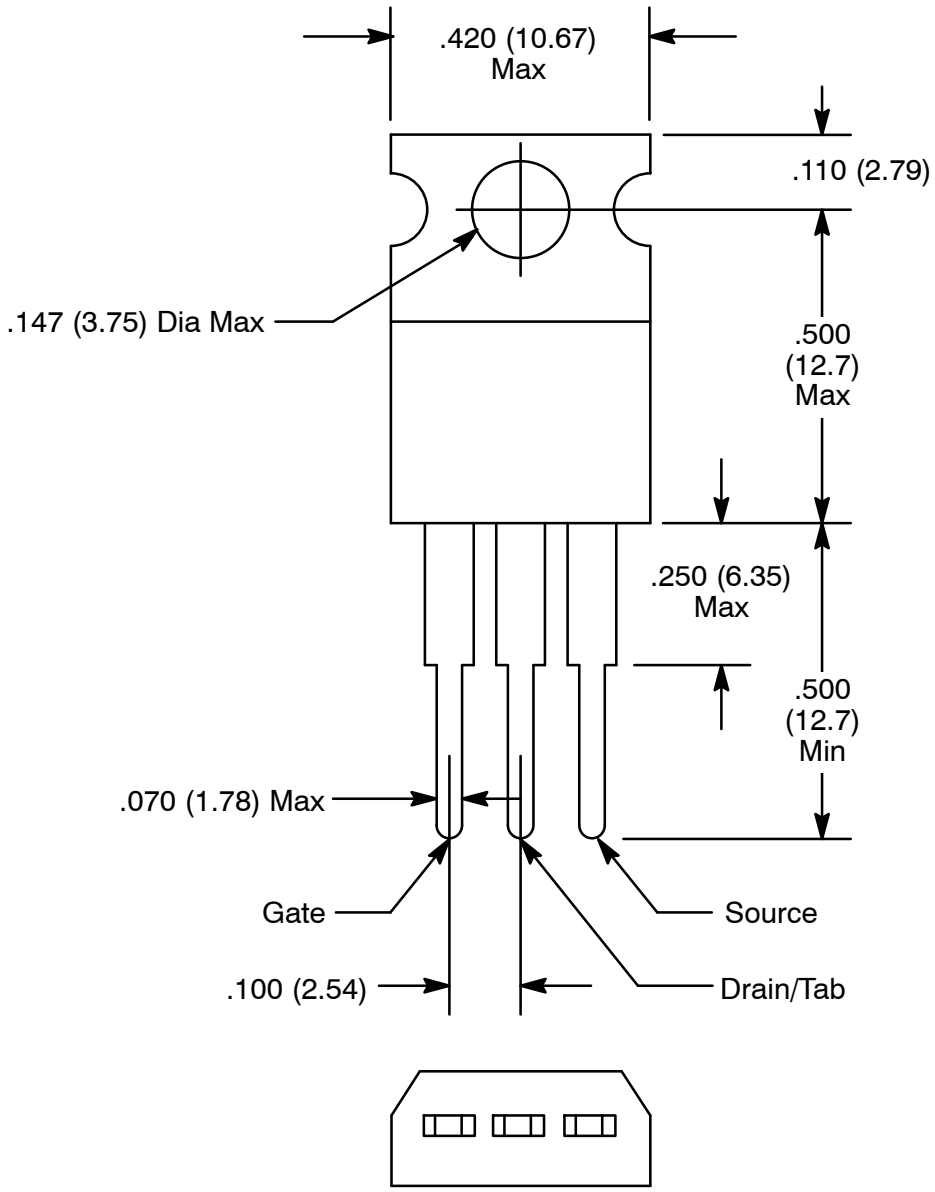
Note 1. Repetitive Rating: Pulse width limited by maximum junction temperature.
Note 2. $V_{DD}$ = –25V, starting $T_J$ = +25°C, L = 3.5mH, $R_G$ = 25Ω, $I_{AS}$ = –21A.
Note 3. $I_{SD}$ ≤ –21A, di/dt ≤ –480A/s, $V_{DD}$ ≤ $V_{(BR)DSS}$, $T_J$ +175°C.

RoHS

**Electrical Characteristics:** ($T_J$ = +25°C unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Drain−Source Breakdown Voltage | $V_{(BR)DSS}$ | $I_D$ = −250μA, $V_{GS}$ = 0 | −100 | – | – | V |
| Breakdown Voltage Temp. Coefficient | $\Delta V_{(BR)DSS}/\Delta T_J$ | Reference to +25°C, $I_D$ = −1mA | – | −0.11 | – | V/°C |
| Static Drain−Source On Resistance | $R_{DS(on)}$ | $V_{GS}$ = −10V, $I_D$ = −24A, Note 4 | – | – | 0.06 | Ω |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = −250μA | −2 | – | −4 | V |
| Forward Transconductance | $g_{fs}$ | $V_{DS}$ = −50V, $I_D$ = −21A | 10 | | – | S |
| Drain−Source Leakage Current | $I_{DSS}$ | $V_{GS}$ = 0, $V_{DS}$ = −100V | – | – | −25 | μA |
| | | $V_{GS}$ = 0, $V_{DS}$ = −80V, $T_C$ = +150°C | – | – | −250 | μA |
| Gate−Body Leakage Current | $I_{GSS}$ | $V_{DS}$ = 0, $V_{GS}$ = ±20V | – | – | ±100 | nA |
| Total Gate Charge | $Q_g$ | $V_{GS}$ = −10V, $I_D$ = −21A, $V_{DS}$ = −80V, Note 4 | – | – | 180 | nC |
| Gate−Source Charge | $Q_{gs}$ | | – | – | 25 | nC |
| Gate−Drain (“Miller”) Charge | $Q_{gd}$ | | – | – | 97 | nC |
| Turn−On Time | $t_{d(on)}$ | $V_{DD}$ = −50V, $I_D$ = −21A, $R_G$ = 2.5Ω, $R_D$ = 2.4Ω, Note 4 | – | 17 | – | ns |
| Rise Time | $t_r$ | | – | 86 | – | ns |
| Turn−Off Delay Time | $t_{d(off)}$ | | – | 79 | – | ns |
| Fall Time | $t_f$ | | – | 81 | – | ns |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = −25V, $V_{GS}$ = 0, f = 1MHz | – | 2700 | – | pf |
| Output Capacitance | $C_{oss}$ | | – | 790 | – | pf |
| Reverse Transfer Capacitance | $C_{rss}$ | | – | 450 | – | pf |
| Internal Drain Inductance | $L_D$ | Between lead, 6mm (0.25 in.) from package and center of die contact | – | 4.5 | – | nH |
| Internal Source Inductance | $L_S$ | | – | 7.5 | – | nH |
| **Source−Drain Diode Ratings and Characteristics** | | | | | | |
| Continuous Source Current (Body Diode) | $I_S$ | | – | – | −40 | A |
| Pulsed Source Current (Body Diode) | $I_{SM}$ | Note 1 | – | – | −140 | A |
| Diode Forward Voltage | $V_{SD}$ | $I_S$ = −21A, $V_{GS}$ = 0, $T_J$ = +25°C, Note 4 | – | – | −1.6 | V |
| Reverse Recovery Time | $t_{rr}$ | $I_F$ = −21A, di/dt = −100A/μs, $T_J$ = +25°C, Note 4 | – | 170 | 260 | ns |
| Reverse Recovered Charge | $Q_{rr}$ | | – | 1.2 | 1.8 | μC |
| Forward Turn−On Time | $t_{on}$ | Intrinsic turn−on time is negligible (turn−on is dominated by $L_S$ + $L_D$) | | | | |

Note 1. Repetitive Rating: Pulse width limited by maximum junction temperature.
Note 4. Pulse test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.


.420 (10.67)
Max
.110 (2.79)
.147 (3.75) Dia Max
.500
(12.7)
Max
.250 (6.35)
Max
.500
(12.7)
Min
.070 (1.78) Max
Gate
Source
.100 (2.54)
Drain/Tab