MCP1012

Primary-Side Start-up IC for Isolated Converters

Features:

- High-Voltage Start-up (Rated 500V/700V)
- Few External Components
- Internal Open-Loop, Peak Current-Mode (PCM) Current Regulator for Start-up
- Current Regulator Constant 21 µs Off Time
- Programmable Low-Frequency Oscillator (LFO) Period
- Cycle-by-Cycle Current Limiting
- Protection Against Continuous Conduction Mode (CCM) of Operation
- Able to Accept External PWM Commands from a Secondary Side Controller via Isolator (Optocoupler or Pulse Transformer)
- Undervoltage Lockout (UVLO) and Overvoltage Lockout (OVLO) Protections
- Sleep and Wake-up Commands
- Low Sleep Power: <15 mW
- Robust Gate Driver, Able to Drive 2.2 nF Load at 65 kHz
- Overtemperature Protection (Thermal Shutdown)
- Package: 7-Lead SOIC
- Environmentally Friendly, EU RoHS Compliant, Pb Free

Applications:

- 120-240 VAC AC-DC Applications
- High Input Voltage Applications, Up to 500 VDC
- DC-DC Conversion where Galvanic Isolation is Required
- Offline Switch Mode Power Supply (SMPS) Applications, such as:
    - Power-on Reset (POR) Voltage Source
    - Current Source for Battery Charging
    - Isolated Bulk Energy Storage for Power Distribution

Related Literature:

- *"MCP1012 1W Demonstration Board User's Guide"*
- *"MCP1630 Data Sheet"*
- *"MCP2221A Data Sheet"*
- *"UCS2113 Data Sheet"*

General Description

The MCP1012 is used as a primary-side start-up IC for starting an offline Switch Mode Power Supply converter working in conjunction with a secondary-side controller. The MCP1012 does not linearly regulate the power converter. The secondary-side controller (digital and/or analog) accurately linear regulates using sophisticated adaptive control schemes that enhance performance and efficiency.

The power converter is exemplified by a flyback converter.

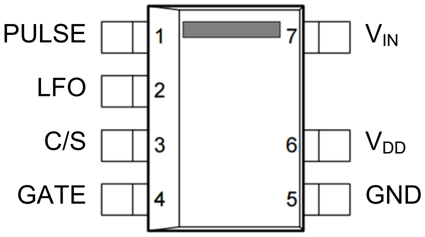
The primary functions of the MCP1012 are:

- Starting-up the flyback converter using an internal open-loop, Peak Current-Mode current regulator
- Accepting PWM commands via optocoupler or pulse transformer from a secondary-side controller
- Providing Undervoltage Lockout (UVLO) and Overvoltage Lockout (OVLO) protection
- Peak cycle-by-cycle current limiting when either under control of its internal current regulator or under control of the secondary-side controller
- Overtemperature protection

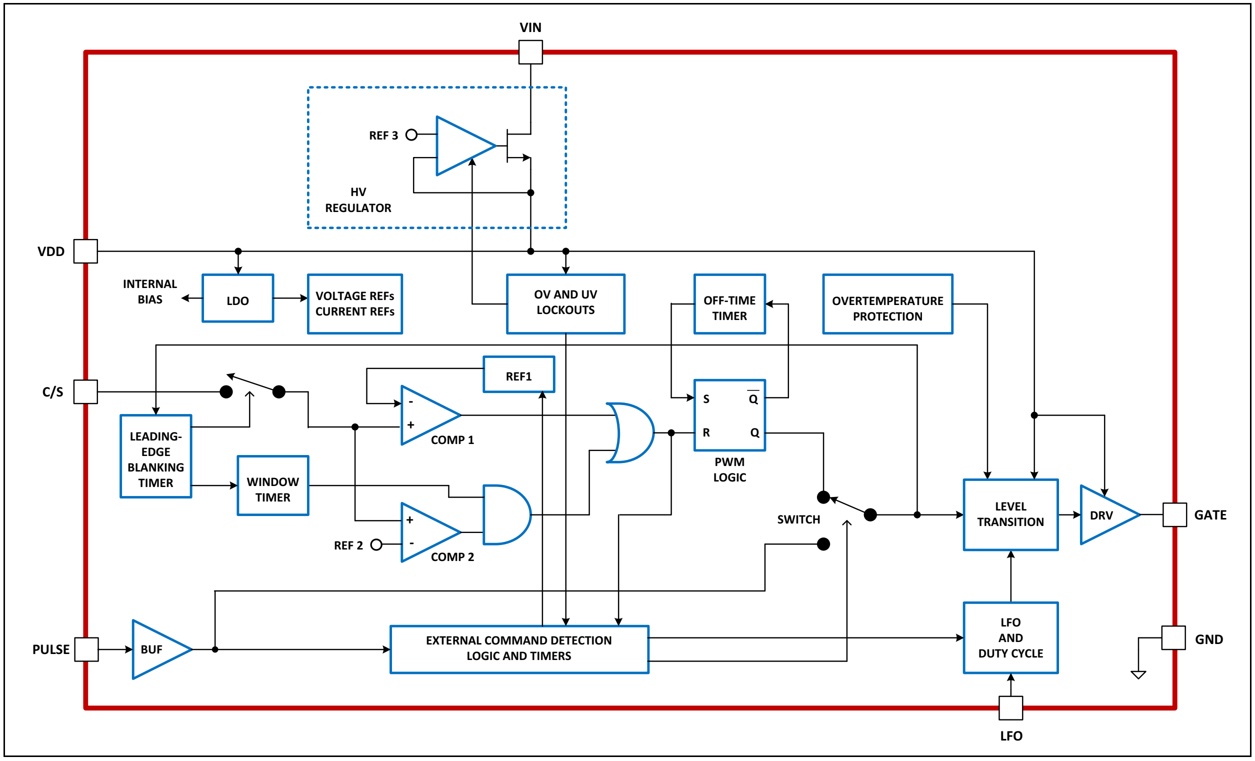
Package Type (Top View)

MCP1012

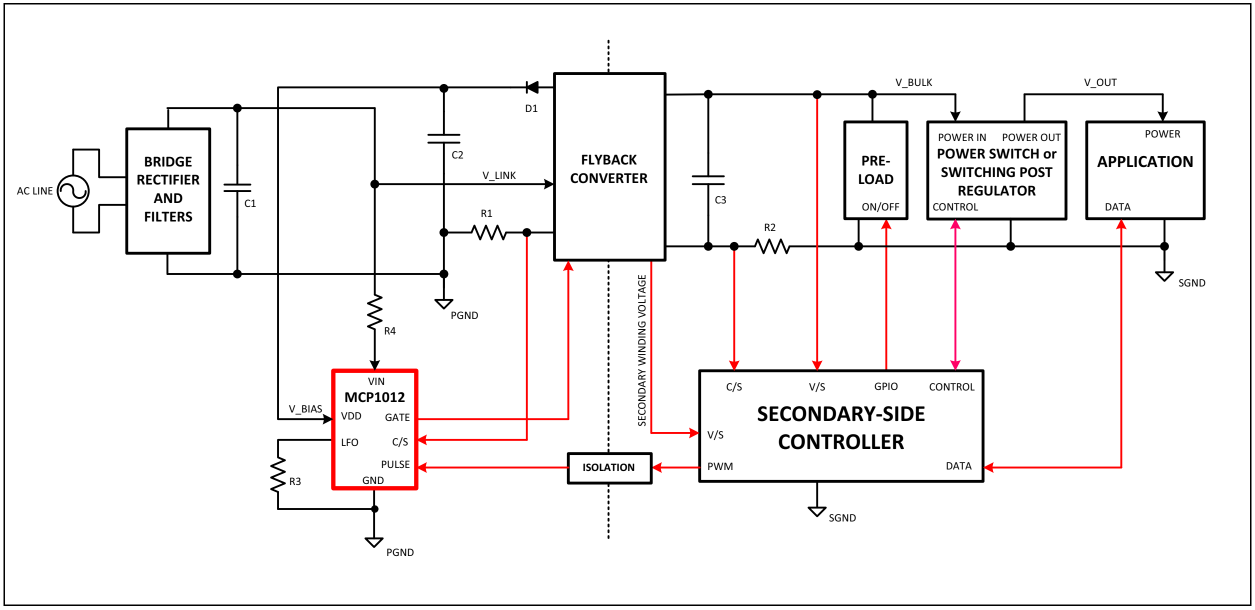
7-Lead SOIC



Functional Block Diagram



Typical Application Circuit



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1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings†

Input Voltage, V_{IN} (**Note 1**)	+700V
External Bias Voltage, V_{DD}	+30V
PULSE, GATE Pins	V_{GND} – 0.3V to V_{DD} + 0.3V
C/S, LFO Pins	V_{GND} – 0.3V to 5.0V + 0.3V
Operating Ambient Temperature	-40°C to +105°C
Storage Temperature	-65°C to +150°C
Maximum Junction Temperature	+125°C
ESD Protection On All Pins (HBM)	±2 kV for LV Pins, 700V for HV Pin

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: V_{IN} is rated for 500V maximum continuous operation. V_{IN} can withstand transients up to 700V with the inclusion of 10 kΩ of resistance in series with V_{IN}, as illustrated by R4 in the **Typical Application Circuit**.

DC CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated: V_{DD} = 15.0V, C_{VDD} = 0.1 µF X7R, C_{GATE} = 2.2 nF, T_A = +25°C. **Boldface** type applies for the full operating temperature range of -40°C to +105°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
High-Voltage Start-up Section						
Minimum Start-up Voltage on V_{IN} Pin	V_{IN}	—	16	—	V	(**Note 2**)
Start-up Current through HV Linear Regulator	$I_{START\text{-}HV}$	**3**	14.6	—	mA	V_{DD} = 2V, V_{IN} = 100V
V_{DD} Regulation Voltage	V_{DD}	**10.5**	11.1	**11.7**	V	V_{IN} = 100V
V_{DD} Regulator Turn-Off Threshold Voltage	$V_{DD\_T\text{-}OFF}$	**10.9**	11.5	**12.1**	V	V_{IN} = 100V
Leakage Current after Start-up	I_{LEAK}	—	1	**10**	µA	V_{IN} = 500V, V_{DD} = 15V (**Note 2**)
V_{DD} Section						
Undervoltage Turn-Off Threshold	$UVLO_{OFF}$	**9.5**	10.0	**10.5**	V	Test by ramping up voltage on V_{DD} (**Note 3**)
Undervoltage Turn-On Threshold	$UVLO_{ON}$	**8.9**	9.4	**9.9**	V	Test by ramping down voltage on V_{DD} (**Note 3**)
Overvoltage Turn-On Threshold	$OVLO_{ON}$	**17.0**	17.9	**18.8**	V	Test by ramping up voltage on V_{DD} (**Note 3**)
Overvoltage Turn-Off Threshold	$OVLO_{OFF}$	**15.4**	16.2	**17.0**	V	Test by ramping down voltage on V_{DD} (**Note 3**)
Start-up Current	$I_{START\text{-}VDD}$	—	320	**480**	µA	$V_{DD} = V_{UVLO\text{-}ON} - 1V$ (**Note 3**)
Operating Current without Gate Switching	I_{OP}	—	600	**900**	µA	V_{DD} = 15V (**Note 3**), R_{LFO} = 47.5 kΩ
Quiescent Current during OVLO	I_Q	—	500	**750**	µA	$V_{DD} = V_{OVLO\text{-}ON} + 1V$ (**Note 3**)
V_{DD} OVP2 Threshold Voltage	V_{OVP2}	24	27	29.9	V	
Shunt Current in OVP2 Mode	I_{DD_OVP2}	3	5	7	mA	$V_{DD} > V_{OVP2}$

Note 1: Specification is obtained by characterization and is not 100% tested.
2: Design guidance only.
3: V_{DD} using external voltage source.

DC CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated: V_{DD} = 15.0V, C_{VDD} = 0.1 µF X7R, C_{GATE} = 2.2 nF, T_A = +25°C. **Boldface** type applies for the full operating temperature range of -40°C to +105°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Low-Frequency Oscillator (LFO)						
Oscillator Frequency	f_{OSC}	**37**	50	**63**	Hz	R_{LFO} = 1 MΩ
		0.70	0.94	**1.18**	kHz	R_{LFO} = 47.5 kΩ
Current Sense Section						
C/S Pin Input Bias Current	$I_{C/S}$	—	—	**10**	µA	$V_{C/S}$ = 0.25V
Propagation Delay to Output	t_{C/S_DELAY}	—	140	**280**	ns	$V_{C/S}$ = 0.25V + 30 mV overdrive
Leading-Edge Blanking (LEB) Time	t_{LEB}	**145**	240	**335**	ns	
Threshold Voltage Right After Blanking	Ref2	**80**	100	**120**	mV	**Note 2**
Timing Windows for Sensing Ref2 Limit After Blanking	t_{SNS_Ref2}	**100**	166	**234**	ns	**Note 2**
COMP1 Reference during External Command	Ref1	**229**	252	**275**	mV	
COMP1 Reference during Internal Command	Ref1	**113**	125	**137**	mV	**Note 2**
Internal Current Regulator Section						
Regulator Off Time	t_{OFF}	**12.5**	21	**29**	µs	
Number of Consecutive Pulses in One Cycle	n_{PULSES}	—	16	—	Pulses	
Command Detection Section						
External PWM Operating Frequency	f_{PWM}	—	—	**100**	kHz	
Propagation Delay to Output	t_{PULSE_DELAY}	—	120	**280**	ns	
External PWM Cease Time Duration	t_{PWM_CEASE}	**145**	260	**375**	ns	
Frequency Range for Sleep Mode	f_{SLEEP}	**450**	500	—	kHz	
Valid Pulse High and Low Levels Duration for Sleep Mode	t_{SLEEP}	—	—	**1.1**	µs	
Pulse Input High Level	$PULSE_{HIGH}$	**3.5**	—	**V_{DD}**	V	
Pulse Input Low Level	$PULSE_{LOW}$	**0**	—	**1.5**	V	
Pulse Input Bias Current	I_{PULSE}	—	10	—	µA	**Note 1**
GATE Output Section						
Output Voltage Low Level	$V_{GATE\text{-}LOW}$	—	—	0.1	V	DC test
Output Voltage High Level	$V_{GATE\text{-}HIGH}$	14.9	—	—	V	DC test
Output Pull-up Resistance	$R_{PULL\text{-}UP}$	—	9.5	13	Ω	I_{OUT} = 50 mA
Output Pull-Down Resistance	$R_{PULL\text{-}DOWN}$	—	2.5	3.4	Ω	I_{OUT} = 50 mA
Rising Time	t_{RISE}	—	—	**250**	ns	
Falling Time	t_{FALL}	—	—	**160**	ns	
GATE Source Driving Capability	I_{SOURCE}	**500**	—	—	mA	V_{GATE} = 0 (**Note 2**)
GATE Sink Driving Capability	I_{SINK}	**1000**	—	—	mA	V_{GATE} = 15V (**Note 2**)
Internal Resistance GATE to GND	$R_{GATE\text{-}GND}$	140	230	320	kΩ	

Note 1: Specification is obtained by characterization and is not 100% tested.

2: Design guidance only.

3: V_{DD} using external voltage source.

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DC CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated: V_{DD} = 15.0V, C_{VDD} = 0.1 µF X7R, C_{GATE} = 2.2 nF, T_A = +25°C. **Boldface** type applies for the full operating temperature range of -40°C to +105°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Overtemperature Protection Section						
Protection Junction Temperature	T_{OTP}	—	146	—	°C	**Note 1**
Hysteresis	T_{HYS}	—	26	—	°C	**Note 1**

Note 1: Specification is obtained by characterization and is not 100% tested.

2: Design guidance only.

3: V_{DD} using external voltage source.

TEMPERATURE SPECIFICATIONS

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Operating Ambient Temperature Range	T_A	-40	—	+105	°C	Steady state
Junction Operating Temperature	T_J	-40	—	+125	°C	
Storage Temperature Range	T_S	-65	—	+150	°C	
Package Thermal Resistances						
Thermal Resistance, 7-Lead SOIC	θ_{JA}	—	141.5	—	°C/W	

NOTES:

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C.

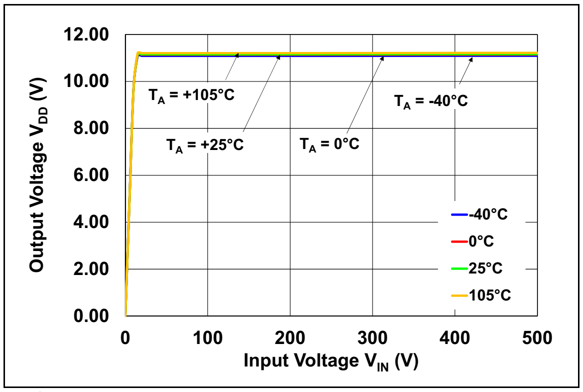

FIGURE 2-1: *V_{DD} Regulation vs. V_{IN} Input Voltage.*

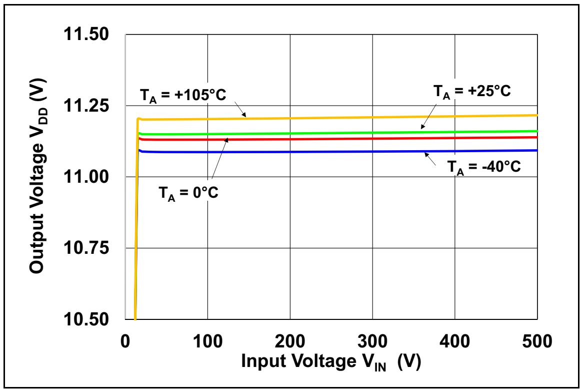

FIGURE 2-2: *V_{DD} Regulation vs. V_{IN} Input Voltage (Zoomed Image).*

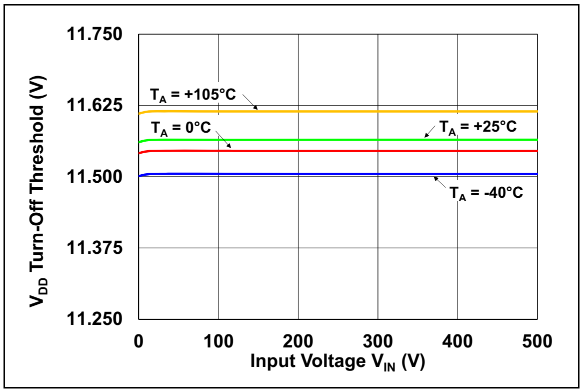

FIGURE 2-3: *V_{DD} Regulator Turn-Off Threshold vs. V_{IN} Voltage.*

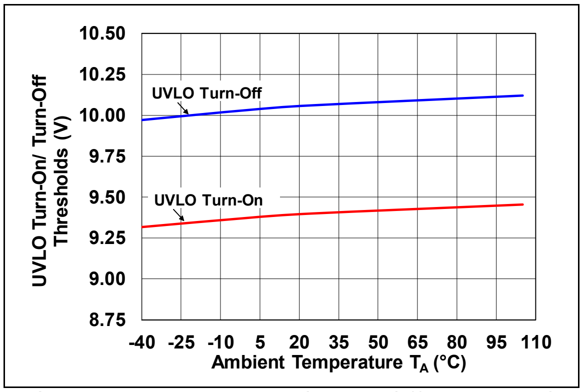

FIGURE 2-4: *UVLO Turn-Off and Turn-On Thresholds vs. Temperature.*

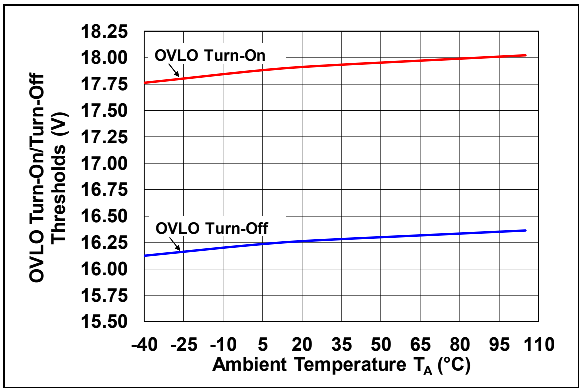

FIGURE 2-5: *OVLO Turn-On and Turn-Off Thresholds vs. Temperature.*

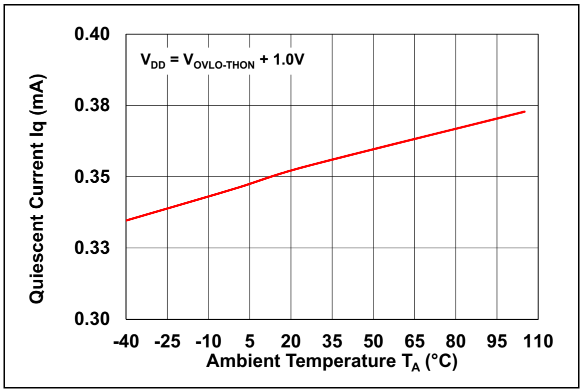

FIGURE 2-6: *Quiescent Current During OVLO vs. Temperature.*

Note: Unless otherwise indicated, T_A = +25°C.

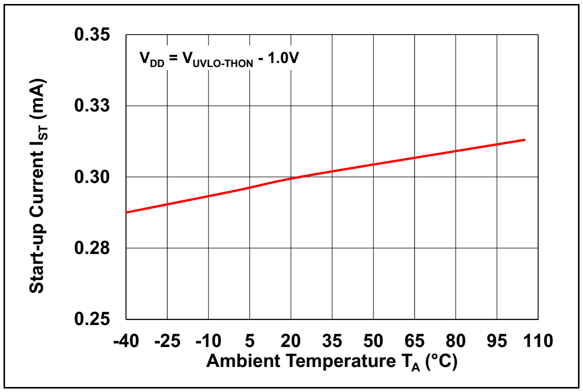

FIGURE 2-7: *Start-up Current During UVLO vs. Temperature.*

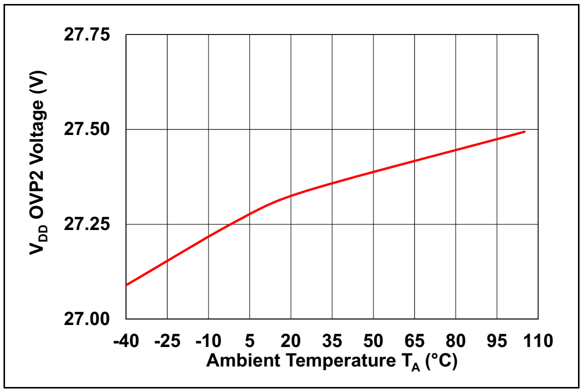

FIGURE 2-8: *V_{DD} OVP2 Voltage vs. Temperature.*

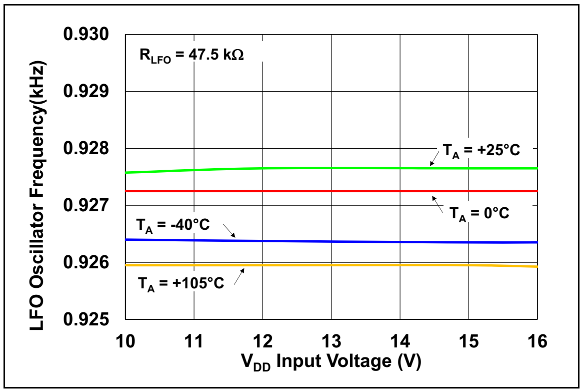

FIGURE 2-9: *LFO Frequency vs. V_{DD} Voltage.*

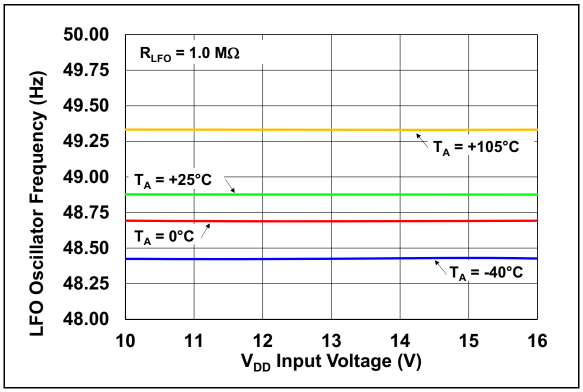

FIGURE 2-10: *LFO Frequency vs. V_{DD} Input Voltage.*

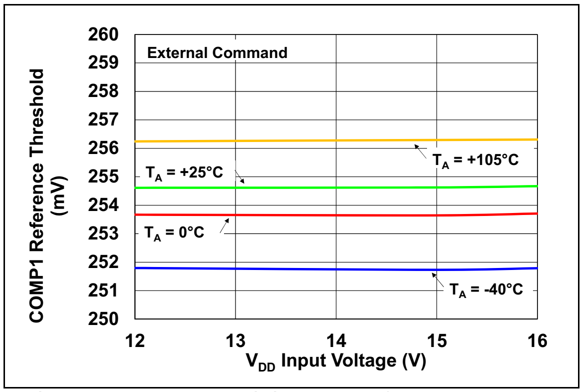

FIGURE 2-11: *COMP1 Reference During External Command vs. V_{DD} Input Voltage.*

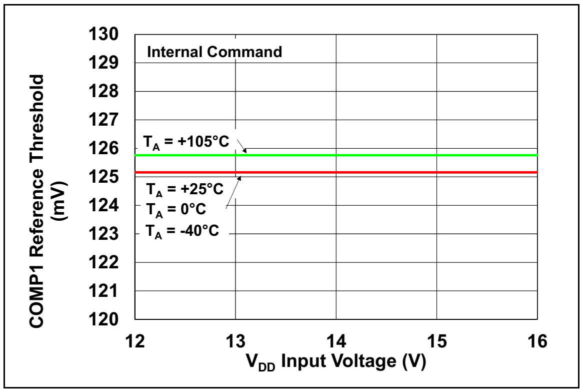

FIGURE 2-12: *COMP1 Reference During Internal Command vs. V_{DD} Input Voltage.*

Note: Unless otherwise indicated, T_A = +25°C.

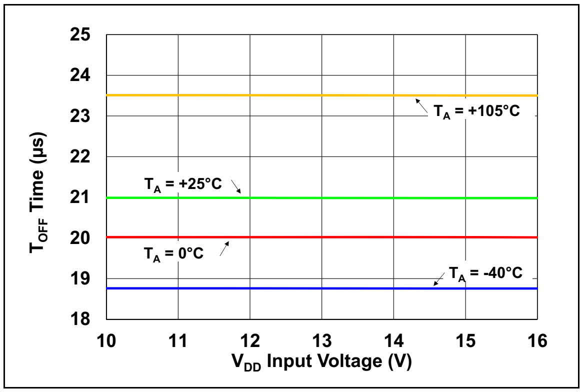

FIGURE 2-13: *Off Time vs. V_{DD} Input Voltage.*

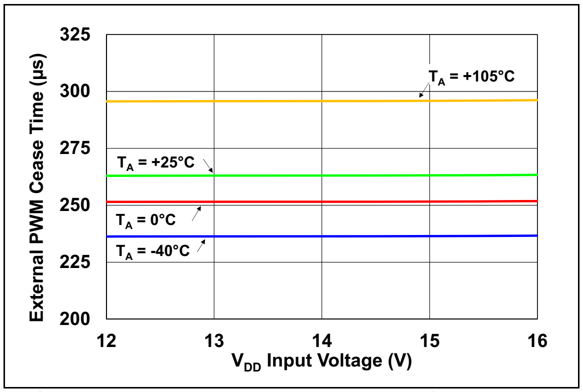

FIGURE 2-14: *External PWM Cease Time vs. V_{DD} Input Voltage.*

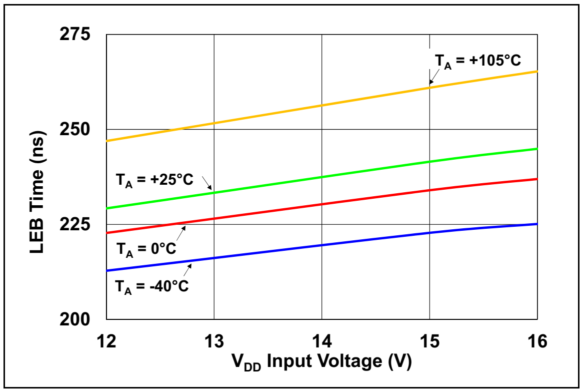

FIGURE 2-15: *LEB Time vs. V_{DD} Input Voltage.*

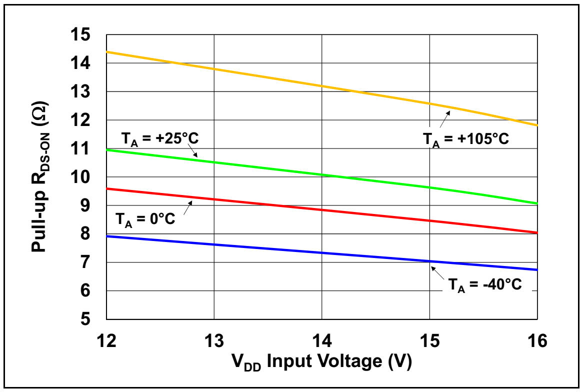

FIGURE 2-16: *Output High-Side Transistor R_{DS-ON} vs. V_{DD} Input Voltage.*

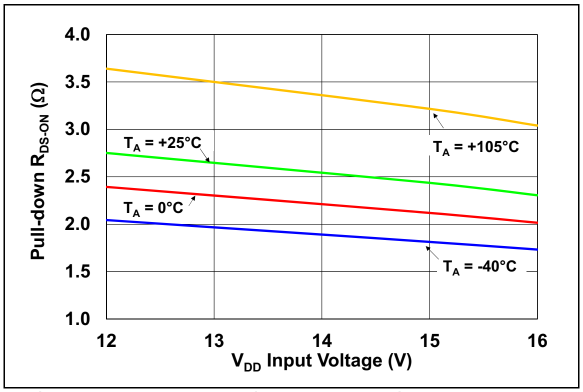

FIGURE 2-17: *Output Low-Side Transistor R_{DS-ON} vs. V_{DD} Input Voltage.*

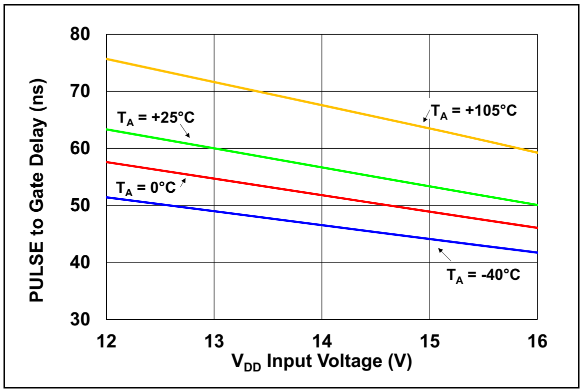

FIGURE 2-18: *PULSE to Gate Delay vs. V_{DD} Input Voltage.*

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Note: Unless otherwise indicated, T_A = +25°C.

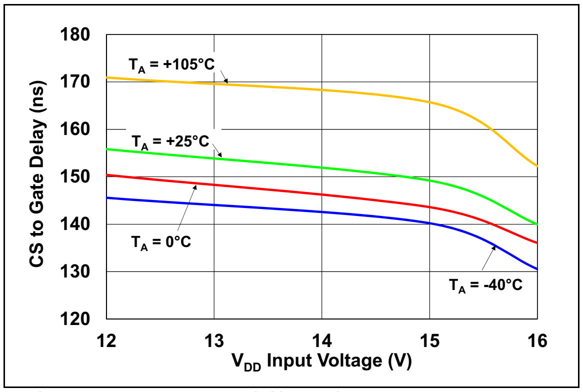

FIGURE 2-19: *C/S to Gate Delay vs. V_{DD} Input Voltage.*

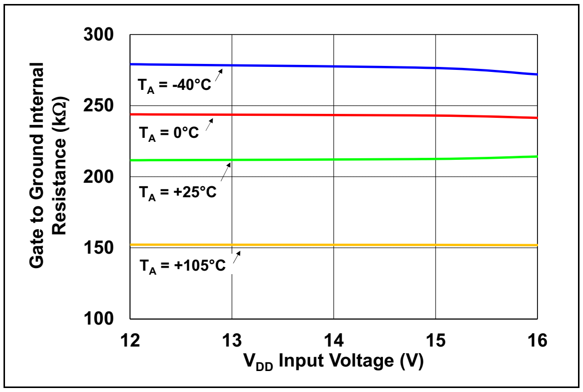

FIGURE 2-20: *Gate to Ground Internal Resistance vs. V_{DD} Input Voltage.*

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3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP1012 7-Lead SOIC	Symbol	Description
1	PULSE	External PWM command input pin.
2	LFO	Low-Frequency Oscillator pin. Resistor connected from this pin to GND sets the LFO's switching period.
3	C/S	Current Sense input pin.
4	GATE	MOSFET Gate Driver output pin.
5	GND	Circuit Ground pin.
6	V_{DD}	Output of the HV Linear Regulator and provides bias to the gate driver and to the IC's internal low-voltage circuitry. V_{DD} is also an input for an external bias source.
7	V_{IN}	High-Voltage input pin to bias the IC during start-up.

3.1 PULSE Pin

This pin accepts signals from the secondary-side controller via an optocoupler or pulse transformer. When the secondary-side controller is in linear control of the flyback converter, the signal to PULSE is a duty cycle varying Pulse-Width Modulation (PWM) wave whose frequency can be between 20 kHz and 65 kHz. While a signal is being detected at the PULSE pin, the GATE pin receives its gating commands via the PULSE pin and not from the IC's internal current regulator. If the signal to PULSE ceases for a time interval greater than 260 µs typical, then the IC will revert to the GATE receiving gating commands from the internal current regulator. The secondary-side controller can also send a short burst (five pulses) of a high-frequency (500 kHz typical) PWM waveform to the PULSE pin to shut down any gating of the gate driver, initiating the Sleep mode. Gating is resumed either by the secondary-side controller resuming sending signals to the PULSE pin, or from the voltage on the V_{DD} pin decaying below the lower limit of the UVLO.

3.2 LFO (Low-Frequency Oscillator) Pin

The power delivered to the secondary during start-up is determined by the switching frequency of the internal Low-Frequency Oscillator (LFO). The duty cycle of the LFO is determined by counts of the internal open-loop, Peak Current-Mode current regulator switching periods. The number of counts is 16. The duty cycle enables/disables the GATE while being commanded by the internal open-loop Peak Current-Mode current regulator. The LFO switching period is determined by the resistor value on the LFO pin.

3.3 C/S (Current Sense) Pin

This pin senses the voltage across an external current sense resistor. This voltage is analogous to the transformer's primary current. A Leading-Edge Blanking (LEB) timer is used to prevent the MOSFET turn-on current spike from prematurely ending the on-time. The C/S voltage is then compared by two comparators: COMP1 and COMP2. COMP1 limits the maximum voltage sensed at the C/S pin (maximum current limit set by REF1). COMP2 is active during the Window Timer time interval that follows the LEB interval. The voltage at the C/S pin will not be allowed to exceed the reference value (REF2) of COMP2 during the Window Timer interval.

3.4 GATE Pin

This pin is the output of the gate driver to an external N-channel power MOSFET.

3.5 GND (Ground) Pin

Ground return for all internal circuitry. GND pin is the ground for both the gate drive and for the IC's internal biases. The PCB layout design needs to consider this single-point GND pin concept.

3.6 V_{DD} Pin

The V_{DD} pin is the output of the HV linear regulator and provides bias to the gate driver and to the IC's internal low-voltage regulators. V_{DD} has an external capacitor to GND. V_{DD} is also the input from an external source of bias (namely, the primary-side bias from the converter). When the external bias is high enough, it can turn off the HV linear regulator. V_{DD} is monitored by Undervoltage Lockout (UVLO) and Overvoltage Lockout (OVLO) blocks.

3.7 V_{IN} Pin

High-voltage input to bias the IC during start-up. V_{IN} is the input to the IC's internal HV linear regulator that steps down the voltage. The output of this regulator is V_{DD}.

NOTES:

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4.0 DEVICE OVERVIEW

The MCP1012 is used as a primary-side start-up IC for starting an offline flyback converter working in conjunction with a secondary-side controller. The secondary-side controller can be a Microchip Digitally Enhanced Power Analog (DEPA) device, a PIC® MCU-based or ARM-based digital controller, or another device. The secondary-side controller's resources can be made available and interactive to the application, (load) since being located on the isolated side of the power supply.

4.1 Input Voltage (V_{IN})

An internal HV (High Voltage) linear regulator is placed between the $\mathbf{V_{IN}}$ pin and the $\mathbf{V_{DD}}$ pin. $\mathbf{V_{IN}}$ can be connected directly to the rectified and filtered AC line. The AC line can typically range between 85 VAC and 265 VAC, resulting in a rectified voltage (V_LINK) range of 120 VDC and 375 VDC. $\mathbf{V_{IN}}$ is rated for 500V maximum continuous operation. V_{IN} can withstand transients up to 700V with the inclusion of 10 kΩ of resistance in series with V_{IN}.

When MCP1012 is in a start-up mode, bias for the IC is drawn from V_LINK via the $\mathbf{V_{IN}}$ pin. The HV linear regulator regulates V_{DD} to 11.1V typical. As the flyback converter starts up, the primary-side bias is assured by an additional transformer winding. This bias must raise $\mathbf{V_{DD}}$ above 11.1V. This will turn off the internal HV linear regulator at a typical threshold of 11.5V and the current through it (from V_LINK via the $\mathbf{V_{IN}}$ pin) will fall to near zero. When the HV linear regulator turns off, this also allows the MCP1012 to accept external PWM commands from the secondary-side controller at its **PULSE** pin. The secondary-side controller should establish converter regulation so that the MCP1012 remains externally biased.

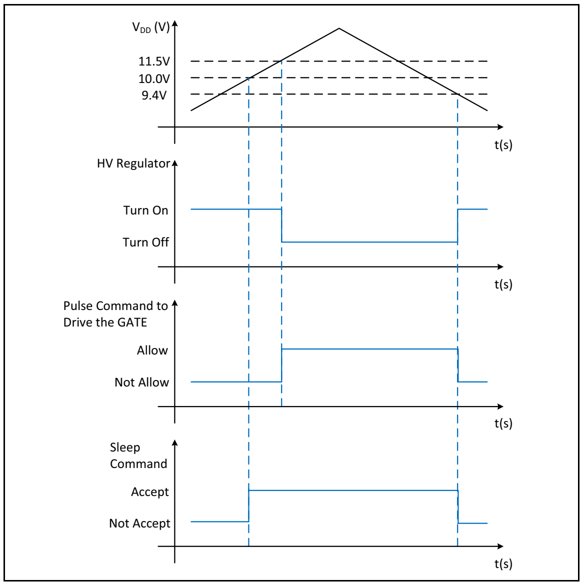

FIGURE 4-1: *UVLO and HV Linear Regulator Turn-Off Thresholds.*

4.2 V_{DD} – Output of the HV Linear Regulator/Input for External Bias

$\mathbf{V_{DD}}$ is the output of the IC's internal HV linear regulator, as well as an input for external bias provided by the flyback converter through the additional transformer winding. $\mathbf{V_{DD}}$ should be bypassed to **GND** by a capacitor of 0.1 µF or greater (this capacitor is the source of peak gate drive currents, Printed Wire Board (PWB) trace routing should take this into account). $\mathbf{V_{DD}}$ is regulated to 11.1V typical by the internal HV linear regulator when power to the IC is being delivered from V_LINK via the $\mathbf{V_{IN}}$ pin. When the flyback converter is in normal operation, it shall provide a bias to $\mathbf{V_{DD}}$ above a nominal 11.5V, which shuts down the internal HV linear regulator and allows the IC to accept external PWM commands on the PULSE pin, but below the OVLO (Overvoltage Lockout) protection threshold.

$\mathbf{V_{DD}}$ directly biases the IC's gate driver (as well as the IC's other low-voltage circuitry). In order to protect the gate of an external power MOSFET, $\mathbf{V_{DD}}$ is monitored by Undervoltage Lockout (UVLO) and Overvoltage Lockout (OVLO) blocks. UVLO has a typical hysteresis range of 9.4V to 10.0V. Once $\mathbf{V_{DD}}$ exceeds the UVLO threshold, the IC's internal current regulator will be allowed to drive the **GATE**. Once $\mathbf{V_{DD}}$ exceeds the HV linear regulator turn-off threshold (11.5V typical), the MCP1012 will allow an external PWM command via the **PULSE** pin to drive the **GATE**. If $\mathbf{V_{DD}}$ drops below 9.4V typical, gating the MOSFET shall be prevented. OVLO has a typical hysteresis range of 16.2V to 17.9V. If $\mathbf{V_{DD}}$ exceeds 17.9V typical, gating the MOSFET shall be stopped.

$\mathbf{V_{DD}}$ voltage may still rise to a 30V level because of voltage transient due to transformer winding leakage inductance. Therefore, in addition to OVLO, a current shunt has been added to $\mathbf{V_{DD}}$, forming the second overvoltage protection: OVP2**.** If the $\mathbf{V_{DD}}$ voltage is larger than 27V typical, then a 5 mA rated (typical) shunt can dissipate the leakage energy to limit the voltage transient.

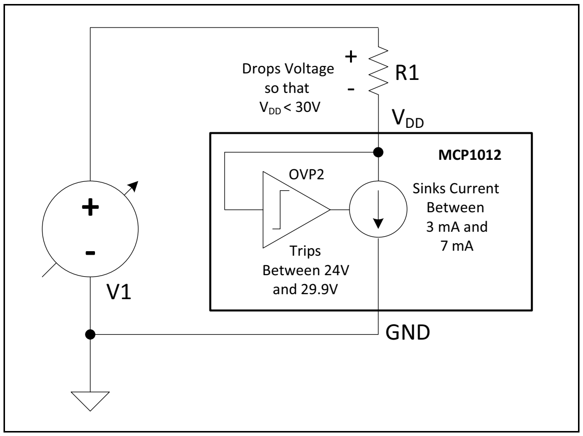

FIGURE 4-2: *V_{DD} Transient Protection Shunt.*

4.3 Ground Pin (GND)

The MCP1012 shares just one ground pin (**GND**) for the gate driver and all the low-power, signal-level circuitry. Therefore, utmost care must be taken in the PWB's design when routing the power returns and the signal returns.

4.4 Current Sense (C/S)

C/S senses a voltage across an external current sense resistor. This resistor is scaled so that the voltage developed across the resistor at maximum allowable peak transformer primary current is 252 mV, which is also the typical reference voltage, REF1, for comparator COMP1 when the MCP1012 is commanded by an external PWM signal at its **PULSE** pin (Normal Run mode).

The current sense signal is "blanked" for 240 ns (typically) at the initiation of the external MOSFET gating on-time. This is called Leading-Edge Blanking (LEB). LEB allows the MCP1012 device's internal current regulator to ignore the turn-on current spike through the current sense resistor. This prevents nuisance tripping causing a premature termination of the on-time.

At the end of the LEB time interval, another Window Timer time interval (typically 166 ns) starts when the COMP2 comparator can sense the signal at **C/S**. COMP2 compares this signal against REF2, whose value is 100 mV typical. If REF2 is exceeded during the Window Timer interval, then the gating on-time is terminated. The purpose of COMP2 is to prevent the flyback converter from entering too deep into a Continuous Conduction mode of operation, which prevents excessive currents from building up in the secondary winding of the transformer if there is a Fault on the secondary side.

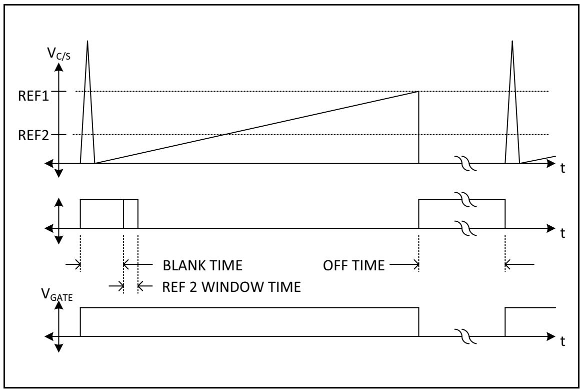

FIGURE 4-3: GATE On-Time being Terminated by C/S Signal Crossing REF1 of COMP1.

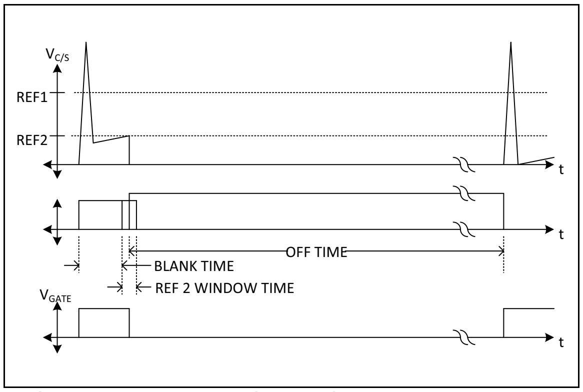

FIGURE 4-4: GATE On-Time being Terminated by C/S Signal Crossing REF2 of COMP2.

The outputs of COMP1 and COMP2 are ORed to an S-R latch. Either comparator can reset the S-R latch which terminates the on-time and begins the off-time. The off-time is internally fixed and has a typical duration of 21 µs. The end of the off-time sets the S-R latch and the on-time begins again. This arrangement forms an open-loop, Peak Current-Mode current regulator.

During start-up, it is this current regulator that limits the transformer's primary current, allowing the flyback converter's output capacitor to charge and activate the secondary-side controller. COMP1 provides maximum current limit protection and COMP2 protects against the flyback converter entering too deep into a Continuous Conduction Mode (CCM) of operation. REF1 for COMP1 is set to 125 mV (typically) when the internal current regulator commands GATE (Start-up mode).

Once the flyback converter has started up, the secondary-side controller will command the MCP1012's gate driver via the PULSE pin, and COMP1 and COMP2 will still provide current protection. If the secondary-side controller is in proper control of the converter, then the signal at C/S should neither trip COMP1 and COMP2, and the on and off-times will be determined by that external controller. If either COMP1 or COMP2 change state while the MCP1012 is being externally commanded, then either comparator will terminate the on-time and the next on-time will be initiated by the PWM signal from the external controller to the PULSE pin. While the MCP1012 is being externally commanded (Normal Run mode), REF1 for COMP1 is set to 252 mV typical.

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4.5 Low-Frequency Oscillator (LFO)

The MCP1012 is equipped with a Low-Frequency Oscillator (LFO). The LFO has a typical selectable frequency range of 50 Hz to 1000 Hz. The period of the LFO is determined by the resistor value on the LFO pin (as typically determined by the following formula).

EQUATION 4-1:

$$R_{LFO} = \frac{5 \cdot 10^7}{f} - 6011.2$$

Where:

R_{LFO} = The resistance value from the LFO pin to GND in ohms

f = Frequency in Hz

The on-time of the LFO’s duty cycle is determined by the number of counts of the internal open-loop, Peak Current-Mode current regulator switching period. The number of counts is 16. So in other words, during start-up, the **GATE** drives the MOSFET 16 times at the frequency of the internal current regulator for each switching period of the LFO.

The following is an example of how the LFO is used to determine the power delivered to the secondary during start-up:

1. Determine the desired start-up Power (P) in watts:
    a) The power selected and the amount of output capacitance to be charged determines the rate of rise of the flyback output voltage;
        i. Output rectifier losses and any secondary-side quiescent loading also determines the rate of rise of output voltage.
    b) Once the output capacitor is charged, the capacitor’s voltage can be clamped by a shunt. The shunt would dissipate the start-up power not used by the secondary-side controller until the secondary-side controller becomes active and assumes control of the MCP1012. Once the secondary-side controller is active, then the shunt can be turned off.
2. Choose the median voltage across the transformer primary (midpoint of the rectified AC input range).
3. Use the value of the primary magnetization inductance (L_{MAG}) of the flyback transformer.
4. Use the value of the primary current sense resistor:
    a) This value is determined to limit the maximum power of the converter when the reference for COMP1 is set for 252 mV.
5. During start-up, the reference for COMP1 is set to 125 mV. Knowing L_{MAG} and the input voltage to the flyback determine the time it takes for the primary current to ramp until the voltage across the current sense resistor is equal to 125 mV.
6. The internal current regulator has a fixed off-time of 21 µs typical. Add the time it takes for the voltage across the current sense to reach 125 mV to the 21 µs off-time to determine the switching period of the internal current regulator.
7. Determine the Energy (E) delivered to the secondary during each switch cycle. Determine the peak primary current when the voltage across the current sense resistor is 125 mV. The energy delivered (in joule) is equal to: 0.5 * L_{MAG} * I^2peak.
8. Multiply this energy by 16. This is the energy delivered during each LFO switching period.
9. Determine how many LFO periods per second are needed to deliver the desired start-up power. This determines the LFO switching frequency (f = P/E). Once the LFO frequency is determined, then the resistor on the LFO pin can be determined

The LFO allows 16 gate pulses at the frequency of the internal open-loop Peak Current-Mode current regulator, per LFO period, when the MCP1012 is in Start-up (internally commanded) mode. When **GATE** is controlled by an external PWM signal at the **PULSE** pin (Normal Run mode), then the LFO is disabled.

4.6 PULSE

The **PULSE** pin is the input for an external source of PWM commands from an external controller (typically located on the secondary side of the power supply). Signals to **PULSE** from the secondary-side controller can be transmitted via either an optocoupler or pulse transformer across the isolation barrier. Figure 4-5 shows a simplified **PULSE** input interface diagram.

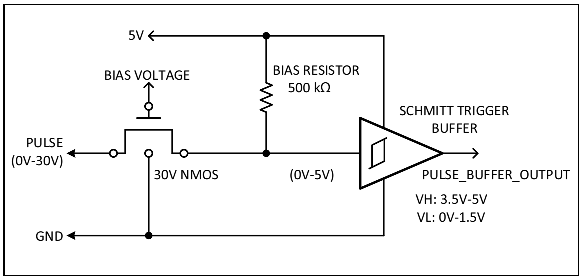

FIGURE 4-5: *Simplified PULSE Input Interface Diagram.*

Interface Description:

- External **PULSE** driver circuit can be biased to V_{DD}
- Pulse input passes through a 30V NMOS transistor
- Pulse voltage greater than 5V will be translated to 5V
- 500 kΩ bias resistor is tied to internal 5V (pull-up)
- Typical 10 µA input sourcing current (5V/500 kΩ)
- High-speed capability > 1 MHz
- Internal 5V Schmitt Trigger with logic spec low level = 0 – 1.5V and high level = 3.5 – 5V
- Hysteresis voltage ~300 mV

The LOW state of the external PWM signal at the **PULSE** pin is the command for **GATE** to be HIGH (**PULSE** is an active-LOW).

External gating commands at **PULSE** will only drive **GATE** when the HV linear regulator is off. External "Sleep/Wake" commands at **PULSE** are valid if the IC is active and V_{DD} is above the lower UVLO threshold.

The **PULSE** detection logic monitors the "R" input of the S-R latch (the ORing of COMP1 and COMP2, see the **Functional Block Diagram**). If "R" changes state due to either COMP1 or COMP2, then the logic will terminate the on-time of the **GATE** until the next on command of the external PWM signal.

Typically, the secondary-side controller will be transmitting a Pulse-Width Modulation (PWM) signal at frequencies between 20 kHz and 65 kHz. If this signal is present, then the MCP1012 device's gate driver will be driven by the signal at the **PULSE** pin and not by the signal from the IC's internal current regulator. This is the Normal Run mode. If the external PWM signal ceases for a period greater than 260 µs typical, then the gate driver will be driven by the internal current regulator (return to Start-up mode).

If the PWM ceases and the signal remains HIGH at the **PULSE** pin, then after 260 µs typical, the **GATE** will be commanded by the internal current regulator (the MCP1012 returns to Start-up mode).

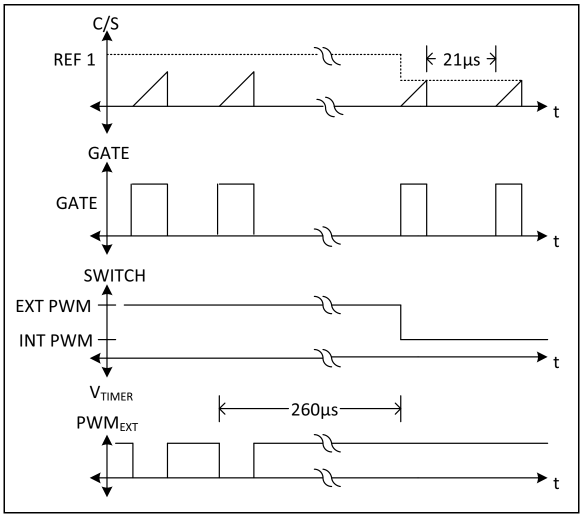

FIGURE 4-6: *External PWM Signal Ceases, Remains HIGH.*

If the PWM ceases and the signal remains LOW, then the **GATE** remains HIGH at first and the signal at **C/S** ramps until either COMP1 or COMP2 trips, and then the **GATE** goes LOW. After 260 µs typical, the **GATE** will be commanded by the internal current regulator (the MCP1012 returns to Start-up mode).

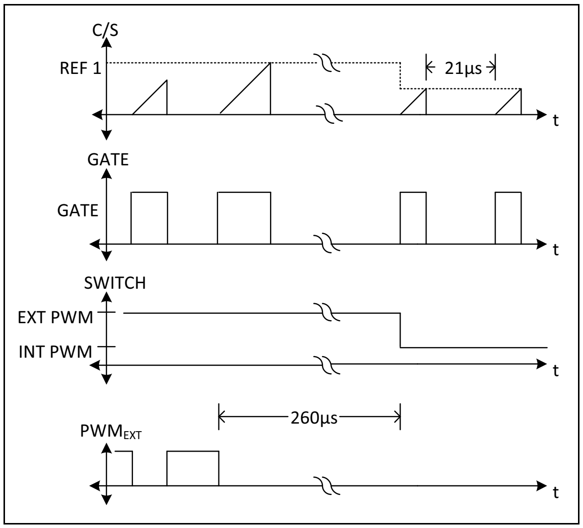

FIGURE 4-7: *External PWM Signal Ceases, Remains LOW.*

For the secondary-side controller to turn off the MCP1012's gating (enter a "Sleep mode"), the **PULSE** logic will detect a high-frequency signal burst at the **PULSE** pin. A burst pattern shall be five pulses (five falling edges at the **PULSE** pin), 50% cycle typical, at 500 kHz typical. This command from the secondary-side controller will not allow gating by the internal current regulator. In order to exit this "Sleep" state:

- The secondary side controller sends a signal:
  - Resuming a PWM signal (return to Normal Run mode), or
  - Sending a single pulse. After the 260 µs typical time interval (external PWM command ceases), the internal current regulator would be allowed to command the gate driver (return to Start-up mode).
- The V_{DD} voltage naturally decays below the lower UVLO threshold level:
  - Receiving the burst pattern (Sleep) command prevents the internal HV linear regulator from becoming active until V_{DD} drops below the lower UVLO threshold or a signal is received at **PULSE**.
  - The **PULSE** logic detects that the internal HV linear regulator has become active and that V_{DD} has exceeded the upper threshold of UVLO, allowing the internal current regulator to command the gate driver (return to Start-up mode).

The MCP1012 will accept the burst pattern command to stop gating if either V_{DD} is biased via the internal HV linear regulator or if V_{DD} is biased externally.

The design objective for Sleep mode is to minimize the MCP1012's power dissipations as much as possible.

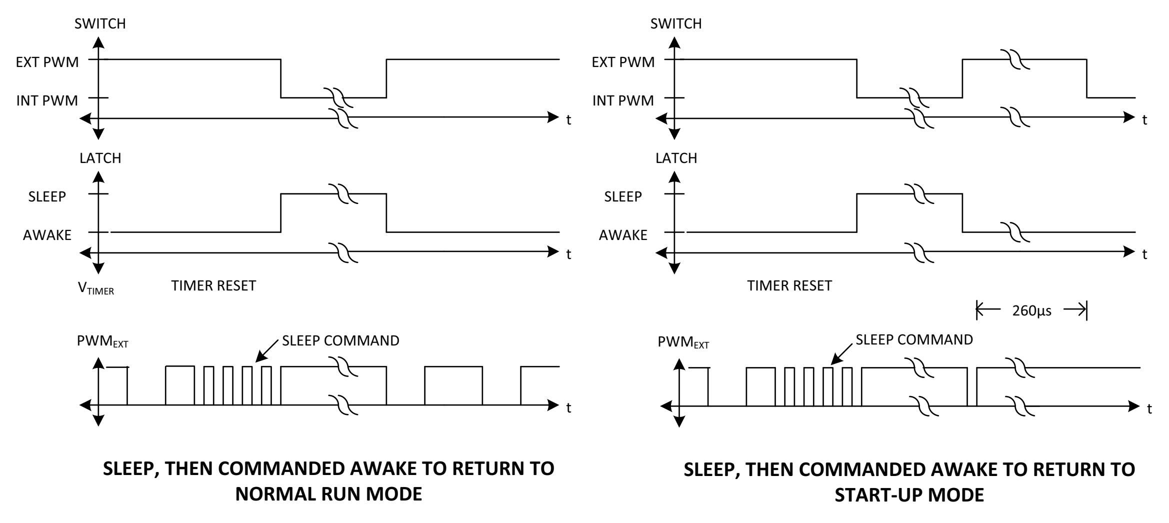

FIGURE 4-8: *Externally Commanded to Enter and Exit Sleep Mode.*

4.7 Application Circuits/Issues

The following is an example using the MCP1012 to start up the flyback converter illustrated in the **Typical Application Circuit** diagram.

- Power Supply Requirements:
  - Universal AC line input
  - 5V output
  - Output current limit, adjustable between 0.5A and 3A
  - Switching frequency of 65 kHz
  - Low-Power Standby mode
- Theory of Operation:
  - MCP1012 enters Start-up mode upon application of the AC line
  - Power delivery switch is open to isolate the load from the power supply output:
    - An example of a power delivery device would be the UCS2113
  - MCP1012 is programmed to deliver a fixed start-up power
  - Preload clamps the main output to a voltage just below the 5V regulation point:
    - Preload ensures all circuitry is properly biased
    - The secondary-side controller (µC) powers up
  - The secondary-side controller, through an isolator, regulates voltage across preload to 5V (Normal Run mode)
  - Power supply waits for commands from the application to apply power to the load:
    - Otherwise, the secondary-side controller can use the MCP1012's 'Sleep' command to enter a 'Standby mode' until the application commands power to be applied to the load
    - The secondary-side controller can communicate to the application via an I^2C/USB UART (an example of an I^2C/USB UART is the MCP2221A)
- Determining the LFO frequency to achieve the desired start-up power:
  - Choose 1W as the desired start-up power to the secondary:
    - This will be the power dissipated by the preload until the secondary-side controller assumes control
    - If the secondary-side controller fails to assume control, then the preload should be designed to dissipate the start-up power indefinitely
  - Assume an additional loss of 0.4W in the flyback converter's output rectifier:
    - 1.4W of power delivered by the transformer to the secondary
  - Assume that this 15W rated flyback converter's transformer has a primary magnetization inductance (L_{MAG}) of 1 mH
  - The typical fixed off-time of the MCP1012's internal current regulator is 21 µs typical
  - The current sense resistor value was chosen to be 0.25Ω:
    - When REF1 for COMP1 is set for 252 mV (in Normal Run mode), this allows a peak current of 1A; therefore, the maximum allowable power to be delivered to the secondary in Normal Run mode is: $0.5 * L_{MAG} * 1^2 * 65000 = 32.5W$
    - When REF1 for COMP1 is set for 125 mV (in Start-up mode), this allows a peak current of 0.5A
  - Determine the on-time of the internal current regulator:
    - Assume a median input voltage to the flyback converter of 248 VDC; the internal current regulator maintains a constant start-up power over the universal AC line range
    - The on-time is equal to: 0.5A * L_{MAG}/248 VDC or 2.016 µs; the off-time is a constant 21 µs
    - Therefore, the internal current regulator's switching period is: 2.016 µs + 21 µs = 23.016 µs typical or a switching frequency of 43.4 kHz
  - The energy per switch cycle of the internal current regulator is equal to $0.5 * L_{MAG} * 0.5^2$ or 0.000125 Joules
  - The energy per 16 switch cycles of the internal current regulator is equal to 16 * 0.000125 Joules or 0.002 Joules
  - The LFO frequency needed for 1.4W is equal to 1.4W/0.002 Joules or 700 Hz:
    - The LFO period is 1/700 = 1.429 ms
  - The resistor value needed for the LFO pin is equal to $5 * 10^7/700 – 6011.2$ or ~65.4 kΩ
  - The LFO 'on-time' is equal to 16*23.016 µs or 0.368 ms
  - The LFO 'duty cycle' is equal to 0.368 ms/1.429 ms or 25.8%

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4.8 Digital Optocoupler Isolation

Typically, the power supply's external controller is located on the load side of the power supply, and the MCP1012 is located on the AC line side of the power supply, where the two sides of the power supply are separated by a safety isolation barrier. Therefore, it is necessary to have a circuit that crosses the isolation barrier so that the external controller can send PWM commands to the PULSE pin of the MCP1012.

The MCP1012's PULSE pin has the same ratings as the MCP1012's V_{DD} pin. The purpose for this is that either an optocoupler circuit or a transformer pulse forming circuit would not require a series regulator and could be powered from the transformer's primary-side tertiary winding.

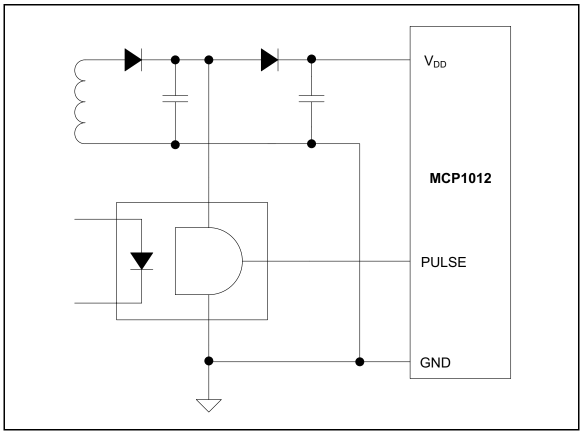


FIGURE 4-9: Digital Optocoupler Isolation.

An example of an optocoupler application circuit that could use the HCPL2202, whose receiver side has a 20V rating. The example is illustrated in Figure 4-9.

- A diode would isolate the HCPL2202 from directly loading the V_{DD} pin of the MCP1012:
  - The HCPL2202 is powered only by the bias winding
  - The V_{DD} of the MCP1012 will not tolerate much external loading
- No series regulator is needed for VCC:
  - V_{DD}'s OVLO prevents the voltage from exceeding 17.9V typical at the V_{DD} pin
  - The PULSE pin has a logic threshold HIGH for a voltage greater than 3.5V. The threshold is LOW for a voltage lower than 1.5V if a 5V series regulator is desired in order to use a different brand of digital optoisolator
- The MCP1012 only responds to commands on its PULSE pin when its V_{DD} is greater than11.5V typical:
  - Therefore, that means the bias winding is actively powering the MCP1012 and the HCPL2202

4.9 Pulse Transformer Isolation

Below is an example of a pulse transformer pulse-former circuit. The pulse transformer is a one-turn primary and a one-turn secondary traces in PCB artwork where two U Core halves meet through slots in the PWM where the traces pass through the core. One trace is on the top side artwork and the other trace is on the far side artwork for voltage isolation. PDRV is the driver output that sends the PWM signal from the external controller on the load side of the power supply to the PULSE pin of the MCP1012 on the AC line side of the power supply. The circuit forms the voltage waveform on the PULSE pin from the on and off current spikes through the transformer. The pulse-forming circuit is biased at the MCP1012's V_{DD} potential.

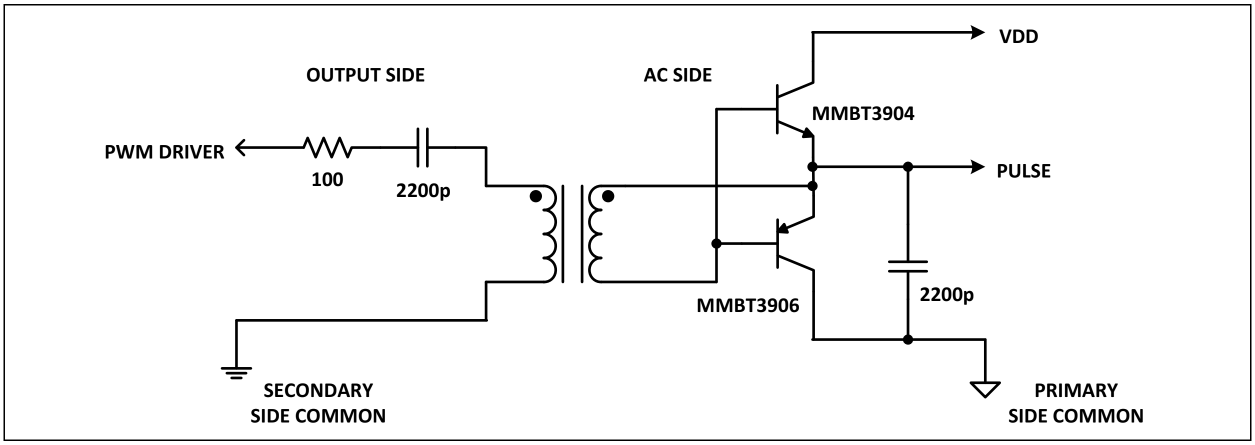


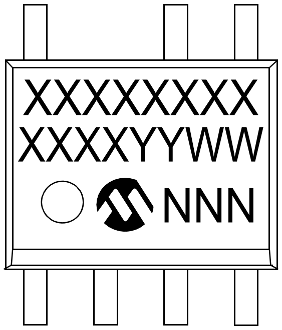
FIGURE 4-10: Planar PULSE Isolation Scheme.

NOTES:

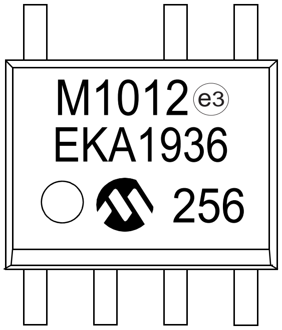
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

7-Lead SOIC



Example

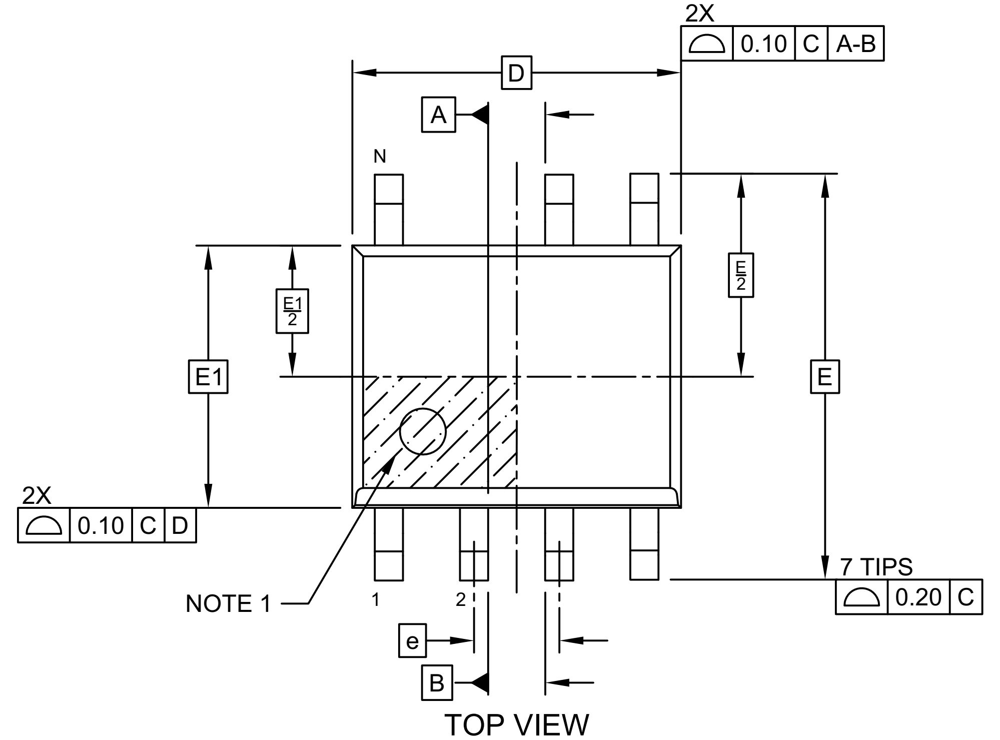


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

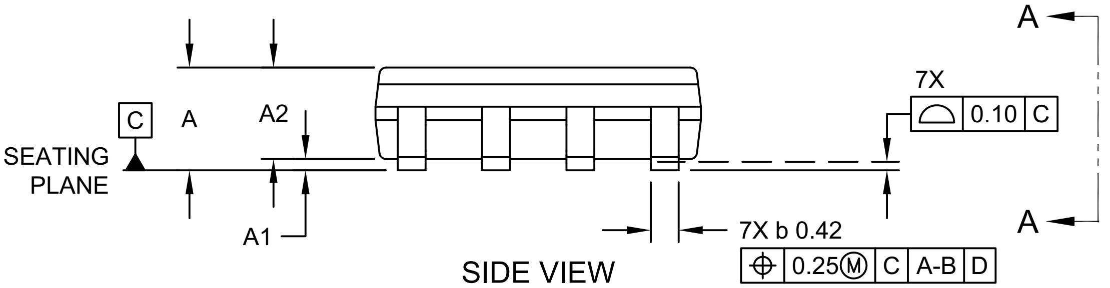
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

7-Lead Small Outline Integrated Circuit (EKA) - 3.90 mm (.150 In.) Body [SOIC]

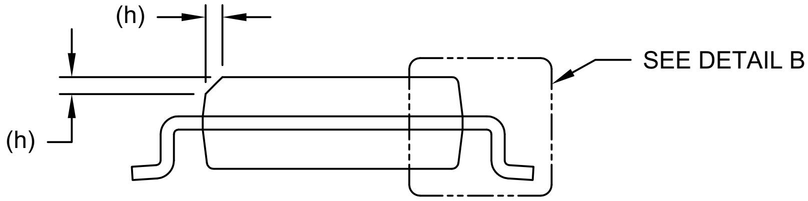
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



VIEW A–A

Microchip Technology Drawing C04-1278 Rev A Sheet 1 of 2

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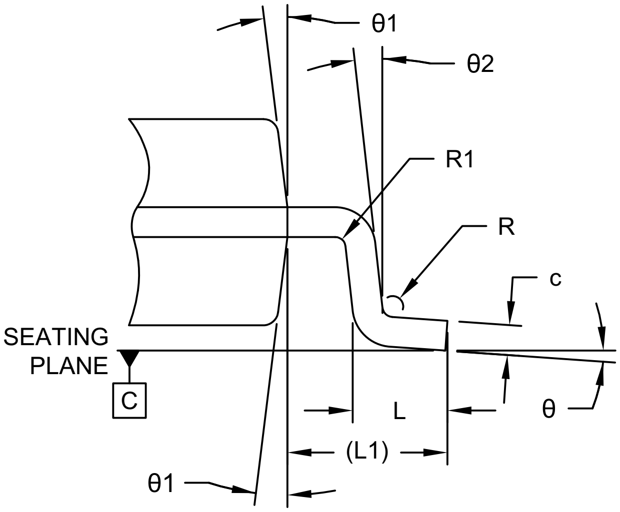
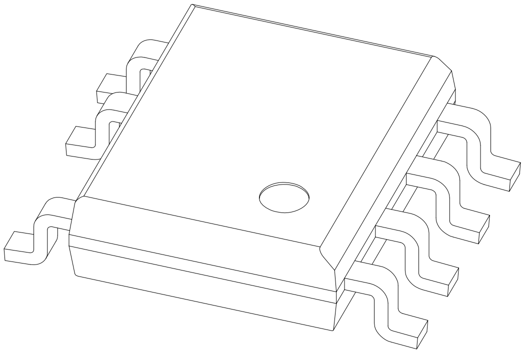
7-Lead Small Outline Integrated Circuit (EKA) - 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL B



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Terminals	N	7		
Pitch	e	1.27 BSC		
Overall Height	A	1.37	1.55	1.73
Standoff	A1	0.10	0.17	0.23
Molded Package Thickness	A2	1.27	1.39	1.50
Overall Length	D	4.90 BSC		
Overall Width	E	6.05 BSC		
Molded Package Width	E1	3.91 BSC		
Terminal Width	b	0.33	0.42	0.51
Terminal Thickness	c	0.10	0.20	0.25
Corner Chamfer	h	0.25 REF		
Terminal Length	L	0.508	-	0.762
Footprint	L1	1.40 REF		
Lead Bend Radius	R1	0.07	-	-
Lead Bend Radius	R2	0.07	-	-
Foot Angle	θ	0°	-	8°
Mold Draft Angle	θ1	5°	-	15°
Lead Angle	θ2	0°	-	-

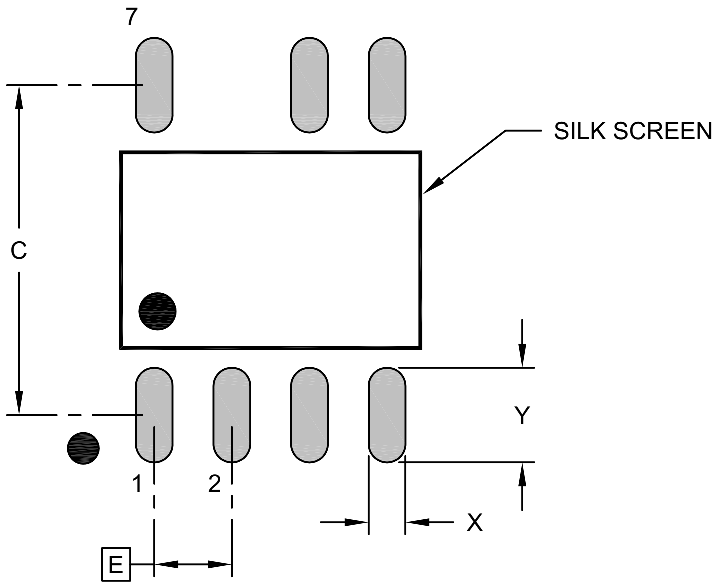
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1278 Rev A Sheet 2 of 2

7-Lead Small Outline Integrated Circuit (EKA) - 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (Xnn)	X			0.60
Contact Pad Length (Xnn)	Y			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3278 Rev A

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APPENDIX A: REVISION HISTORY

Revision B (April 2020)

The following is the list of modifications:

- Updated **Product Identification System**.
- Package available in Tape and Reel option

Revision A (February 2020)

- Original Release of this Document.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	**X(1)**	**-X**	**/XXX**
Device	**Media Type**	**Temperature Range**	**Package**

Device:	MCP1012	=	Primary-Side Start-up IC for Isolated Converters
Media Type:		=	Tape and Reel
Temperature Range:	V	=	-40°C to +105°C (Industrial)
Package:	EKA	=	Small Outline (SOIC)

Examples:

a)	MCP1012-V/EKA:	Primary-Side Start-up IC, Tape and Reel, -40°C to +105°C, 7-Lead SOIC

Note 1: Package available in Tape and Reel option.

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NOTES:

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