



LISA-U2 series

3.75G HSPA+ Cellular Modules

Data Sheet



Abstract

Technical data sheet describing the LISA-U2 series HSPA+ cellular modules. These modules are a complete and cost efficient 3.75G solution offering up to six-band high-speed HSPA+ and quad-band GSM/EGPRS voice and/or data transmission technology in a compact form factor.

Document Information

Title	LISA-U2 series	
Subtitle	3.75G HSPA+ Cellular Modules	
Document type	Data Sheet	
Document number	UBX-13001734	
Revision and date	R20	24-Jan-2019
Disclosure restriction		
Product Status	Corresponding content status	
Functional Sample	Draft	For functional testing. Revised and supplementary data will be published later.
In Development / Prototype	Objective Specification	Target values. Revised and supplementary data will be published later.
Engineering Sample	Advance Information	Data based on early testing. Revised and supplementary data will be published later.
Initial Production	Early Prod. Information	Data from product verification. Revised and supplementary data may be published later.
Mass Production / End of Life	Production Information	Final product specification.

u-blox or third parties may hold intellectual property rights in the products, names, logos and designs included in this document. Copying, reproduction, modification or disclosure to third parties of this document or any part thereof is only permitted with the express written permission of u-blox.

The information contained herein is provided "as is" and u-blox assumes no liability for its use. No warranty, either express or implied, is given, including but not limited to, with respect to the accuracy, correctness, reliability and fitness for a particular purpose of the information. This document may be revised by u-blox at any time without notice. For the most recent documents, visit www.u-blox.com.

Copyright © u-blox AG.

This document applies to the following products:

Name	Type number	Modem version	Application version	PCN reference	
LISA-U200	LISA-U200-01S-00	22.40		UBX-TN-12040	Obsolete
	LISA-U200-01S-01	22.40	A01.00		End of Life
	LISA-U200-01S-02	22.40	A01.02	UBX-17048820	End of Life
	LISA-U200-01S-03	22.40	A01.03	UBX-18055867	Initial Production
	LISA-U200-02S-01	22.90	A01.01	UBX-14005768	End of Life
	LISA-U200-02S-02	22.90	A01.03	UBX-17048820	End of Life
	LISA-U200-03S-00	23.41	A01.01	UBX-15020745	Obsolete
	LISA-U200-03S-01	23.41	A01.04	UBX-17048820	End of Life
	LISA-U200-03S-02	23.41	A01.05	UBX-18055867	Initial Production
	LISA-U200-52S-01	22.86	A01.01	UBX-14005768	Obsolete
	LISA-U200-52S-02	22.86	A01.03	UBX-17048820	End of Life
	LISA-U200-52S-03	22.86	A01.04	UBX-18055867	Initial Production
	LISA-U200-62S-01	22.90	A01.01	UBX-14005768	Obsolete
	LISA-U200-62S-02	22.90	A01.02	UBX-16017712	End of Life
	LISA-U200-62S-03	22.90	A01.03	UBX-17048820	End of Life
	LISA-U200-62S-04	22.90	A01.04	UBX-18055867	Initial Production
LISA-U200 FOTA	LISA-U200-83S-00	23.41	A01.01	UBX-15020745	End of Life
LISA-U201	LISA-U201-03S-00	23.41	A01.01	UBX-15020745	End of Life
	LISA-U201-03S-01	23.41	A01.04	UBX-17048820	Mass Production
LISA-U201 FOTA	LISA-U201-83S-00	23.41	A01.02	UBX-16006079	Obsolete
	LISA-U201-83S-01	23.41	A01.04	UBX-17048820	Mass Production
LISA-U230	LISA-U230-01S-01	22.40	A01.00	UBX-TN-12040	Obsolete
	LISA-U230-01S-02	22.40	A01.02	UBX-17048820	End of Life
	LISA-U230-01S-03	22.40	A01.03	UBX-18055867	Initial Production
LISA-U260	LISA-U260-01S-02	22.61	A01.02	UBX-14042086	Obsolete
	LISA-U260-01S-03	22.61	A01.05	UBX-17048820	End of Life
	LISA-U260-02S-02	22.90	A01.02	UBX-14042086	End of Life
	LISA-U260-02S-03	22.90	A01.04	UBX-17048820	End of Life
LISA-U270	LISA-U270-01S-02	22.61	A01.02	UBX-14042086	Obsolete
	LISA-U270-02S-02	22.90	A01.02	UBX-14042086	End of Life
	LISA-U270-02S-03	22.90	A01.04	UBX-17048820	End of Life
	LISA-U270-62S-04	22.93	A01.02	UBX-14042086	Obsolete
	LISA-U270-62S-05	22.93	A01.04	UBX-15029938	Obsolete
	LISA-U270-62S-06	22.93	A01.05	UBX-16009934	Obsolete
	LISA-U270-62S-07	22.93	A01.07	UBX-17048820	End of Life
	LISA-U270-63S-00	22.93	A01.06	UBX-16010383	Obsolete
	LISA-U270-63S-01	22.93	A01.07	UBX-17048820	End of Life
	LISA-U270-63S-02	22.93	A01.08	UBX-18055867	Initial Production
	LISA-U270-68S-00	22.93	A01.03	UBX-15019240	Obsolete
	LISA-U270-68S-01	22.93	A01.07	UBX-17048820	End of Life

Contents

Document Information	2
Contents	4
1 Functional description	6
1.1 Overview.....	6
1.2 Product features	6
1.3 Block diagram	7
1.4 Product description	8
1.5 AT command support	9
1.6 Supported features	10
2 Interfaces	13
2.1 Power management	13
2.1.1 Module supply (VCC).....	13
2.1.2 RTC supply (V_BCKP).....	13
2.1.3 Digital I/O interfaces supply (V_INT).....	13
2.2 RF antenna interface.....	13
2.3 System functions.....	13
2.3.1 Module power-on	13
2.3.2 Module power-off.....	13
2.3.3 Module reset	14
2.4 (U)SIM interface	14
2.5 Serial communication	14
2.5.1 Asynchronous serial interface (UART)	15
2.5.2 Universal Serial Bus (USB)	15
2.5.3 Serial Peripheral Interface (SPI).....	17
2.5.4 Multiplexer protocol	17
2.6 DDC (I ² C) bus interface	17
2.7 Audio.....	17
2.8 GPIO	18
3 Pin definition	19
3.1 Pin assignment.....	19
4 Electrical specifications	24
4.1 Absolute maximum rating.....	24
4.1.1 Maximum ESD.....	25
4.2 Operating conditions.....	25
4.2.1 Operating temperature range.....	25
4.2.2 Module thermal resistance.....	26
4.2.3 Supply/Power pins	26
4.2.4 Current consumption.....	27
4.2.5 RF characteristics	29
4.2.6 PWR_ON pin.....	30
4.2.7 RESET_N pin	30
4.2.8 (U)SIM pins.....	30

4.2.9	Generic Digital Interface pins	31
4.2.10	USB pins	43
4.2.11	DDC (I ² C) pins.....	43
4.3	Parameters for ATEX applications	44
5	Mechanical specifications	45
6	Reliability tests and approvals.....	46
6.1	Reliability tests	46
6.2	Approvals	46
7	Product handling & soldering.....	47
7.1	Packaging	47
7.1.1	Reels	47
7.1.2	Tapes.....	48
7.2	Moisture Sensitivity Levels.....	49
7.3	Reflow soldering	49
7.4	ESD precautions.....	49
8	Default settings	50
9	Labeling and ordering information	51
9.1	Product labeling.....	51
9.2	Explanation of codes	51
9.3	Ordering information.....	52
Appendix	53
Related documents	56
Revision history	57
Contact	58

1.3 Block diagram

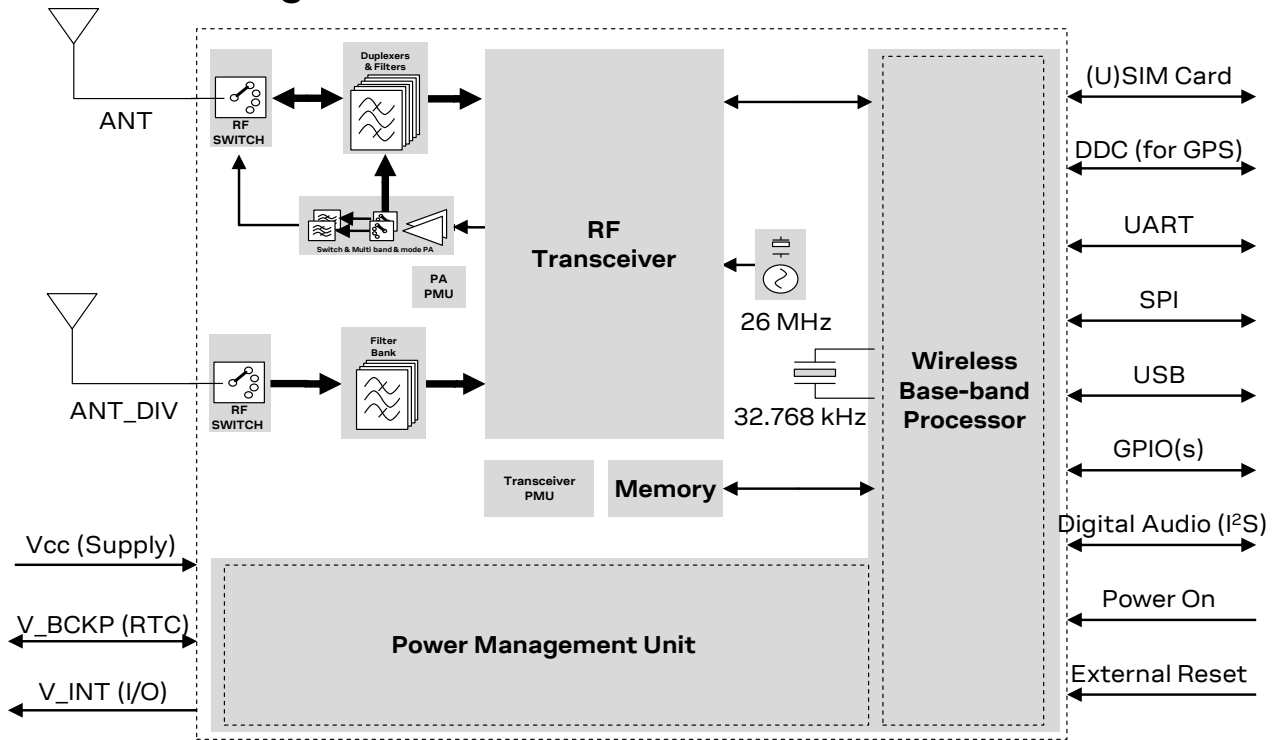


Figure 1: LISA-U2 series block diagram (for available options, see the product main features summary in [Table 1](#))

1.4 Product description

3G UMTS/HSDPA/HSUPA Characteristics	2G GSM/GPRS/EDGE Characteristics
Class A User Equipment ¹	Class B Mobile Station ²
UMTS Terrestrial Radio Access (UTRA) Frequency Division Duplex (FDD) 3GPP Release 7 Evolved High Speed Packet Access (HSPA+) Rx Diversity for LISA-U230	GSM EDGE Radio Access (GERA) 3GPP Release 7 Rx Diversity for LISA-U230
Six-band support for LISA-U200 and LISA-U230: <ul style="list-style-type: none"> Band I (2100 MHz), Band II (1900 MHz), Band IV (1700 MHz), Band V (850 MHz), Band VI (800 MHz), Band VIII (900 MHz) Five-band support for LISA-U201: <ul style="list-style-type: none"> Band I (2100 MHz), Band II (1900 MHz), Band V (850 MHz), Band VI (800 MHz), Band VIII (900 MHz) Dual-band support for LISA-U260: <ul style="list-style-type: none"> Band II (1900 MHz), Band V (850 MHz) Dual-band support for LISA-U270: <ul style="list-style-type: none"> Band I (2100 MHz), Band VIII (900 MHz) 	Quad-band support <ul style="list-style-type: none"> GSM 850 MHz, E-GSM 900 MHz, DCS 1800 MHz, PCS 1900 MHz
WCDMA/HSDPA/HSUPA Power Class <ul style="list-style-type: none"> Power Class 3 (24 dBm) for WCDMA/HSDPA/HSUPA mode 	GSM/GPRS Power Class <ul style="list-style-type: none"> Power Class 4 (33 dBm) for GSM/E-GSM bands Power Class 1 (30 dBm) for DCS/PCS bands EDGE Power Class <ul style="list-style-type: none"> Power Class E2 (27 dBm) for GSM/E-GSM bands Power Class E2 (26 dBm) for DCS/PCS bands
PS (Packet Switched) Data rate <ul style="list-style-type: none"> HSUPA category 6, up to 5.76 Mbit/s UL HSDPA category 8 up to 7.2 Mbit/s DL (except LISA-U230) HSDPA category 14 up to 21.1 Mbit/s DL (only LISA-U230) WCDMA PS data up to 384 kbit/s DL/UL 	PS (Packet Switched) data rate ³ <ul style="list-style-type: none"> GPRS multi-slot class 12 ⁴, coding scheme CS1-CS4, up to 85.6 kbit/s DL/UL EDGE multi-slot class 124, coding scheme MCS1-MCS9, up to 236.8 kbit/s DL/UL
CS (Circuit Switched) Data rate <ul style="list-style-type: none"> WCDMA CS data up to 64 kbit/s DL/UL 	CS (Circuit Switched) data rate <ul style="list-style-type: none"> GSM CS data up to 9.6 kbit/s DL/UL supported in transparent/non transparent mode

Table 2: LISA-U2 series UMTS/HSDPA/HSUPA and GSM/GPRS/EDGE characteristics

Operation modes I to III are supported on the GSM/GPRS network, with user-defined preferred service selectable from GSM to GPRS. Paging messages for GSM calls can be optionally monitored during GPRS data transfer in not-coordinating NOM II-III.

Direct Link mode is supported for TCP and UDP sockets.

¹ Devices can work simultaneously in Packet Switch and Circuit Switch modes: voice calls are possible while the data connection is active without any interruption in service.

² Device can be attached to both GPRS and GSM services (i.e. Packet Switch and Circuit Switch mode) using one service at a time. If for example during data transmission an incoming call occurs, the data connection is suspended to allow the voice communication. Once the voice call has terminated, the data service is resumed.

³ GPRS/EDGE multi-slot class determines the number of timeslots available for upload and download and thus the speed at which data can be transmitted and received, with higher classes typically allowing faster data transfer rates.


⁴ GPRS/EDGE multi-slot class 12 implies a maximum of 4 slots in DL (reception) and 4 slots in UL (transmission) with 5 slots in total.

Basic features	Supplementary services	Short Message Service (SMS)
Display of Called Number	Call Hold/Resume (CH)	SMS Classes 1, 2, 3
Indication of Call Progress Signals	Call Waiting (CW)	Mobile-Originating SMS (MO SMS)
Country/PLMN Indication	Multi-Party (MTPY)	Mobile-Terminating SMS (MT SMS)
International Access Function	Call Forwarding (CF)	SMS Cell Broadcast (SMS CB)
Service Indicator	Call Divert	Text and PDU mode supported
Dual Tone Multi Frequency (DTMF)	Explicit Call Transfer (ECT)	SMS during circuit-switched calls
Subscription Identity Management	Call Barring (CB)	SMS over PSD or CSD
Service Provider Indication	Advice of Charge Charging (AOCC)	SMS storage on SIM and memory module
Abbreviated Dialing	Calling Line Identification Presentation (CLIP)	
SIM Toolkit	Calling Line Identification Restriction (CLIR)	
SIM Access Profile	Connected Line Identification Presentation (COLP)	
	Connected Line Identification Restriction (COLR)	
	Unstructured Supplementary Services Data (USSD)	
	Network Identify and Time Zone (NITZ)	

Table 3: LISA-U2 series mobile station basic features, supplementary services and SMS services summary⁵

1.5 AT command support

LISA-U2 series modules support AT commands according to the 3GPP Technical Specifications TS 27.007 [1], 27.005 [2], 27.010 [3], and the u-blox AT commands extension.

 For the complete list of the supported AT commands and their syntax, see the u-blox AT Commands Manual [4].

RIL (Radio Interface Layer) software for Android is available for LISA-U2 series modules free of charge; see the Android RIL Production delivery application note [5] for more information.


⁵ All these functionalities are supported via AT commands (for more details, see the u-blox AT Commands Manual [4]).

1.6 Supported features

Table 4 lists the main features supported by LISA-U2 modules. For more details, see the LISA-U2 series System Integration Manual [6] and the u-blox AT commands manual [4].

Feature	Description
Network Indication	GPIO configured to indicate the network status: registered home network, registered roaming, voice or data call enabled, no service. The feature can be enabled through the +UGPIOC AT command.
Antenna Detection	Antenna presence detection capability is provided, evaluating the resistance from the ANT pin to GND by means of an internal antenna detection circuit. The antenna detection feature can be enabled through the +UANTR AT command.
Jamming detection	Detects some "artificial" interference that obscures the operator's carriers entitled to give access to the GSM/UMTS service and reports the start and stop of such conditions to the application processor (AP). The AP can react appropriately by e.g. switching off the radio transceiver to reduce power consumption and monitoring the environment at constant periods. The feature can be enabled and configured through the +UCD AT command.
Embedded TCP and UDP stack	Embedded TCP/IP and UDP/IP stack including direct link mode for TCP and UDP sockets. Sockets can be set in Direct Link mode to establish a transparent end-to-end communication with an already connected TCP or UDP socket via the serial interface.
FTP, FTPS	File Transfer Protocol as well as Secure File Transfer Protocol (SSL encryption of FTP control channel) functionalities are supported via AT commands.
HTTP, HTTPS	Hyper-Text Transfer Protocol as well as Secure Hypertext Transfer Protocol (SSL encryption) functionalities are supported via AT commands. HEAD, GET, POST, DELETE and PUT operations are available. Up to 4 client contexts can be used simultaneously.
Embedded TLS 1.2 ⁶	With the support of X.509 certificates, it provides server and mutual authentication, data encryption, data signature and enables TCP/IP applications, such as HTTP and FTP to communicate over a secured and trusted connection. The feature can be configured and enabled by +USECMNG and +USECPRF AT commands.
IPv4/IPv6 dual-stack ⁶	Capability to move between IPv4 and dual stack network infrastructures using external context. IPv4 and IPv6 addresses can be used.
GNSS via Modem	Full access to u-blox positioning chips and modules is available through a dedicated DDC (I ² C) interface. This means that from any host processor, a single serial port can control the cellular module and the positioning chip or module. For more details, see the GNSS Implementation Application Note [7].
Embedded AssistNow Software	Embedded AssistNow Online and AssistNow Offline clients to provide better GNSS performance and faster Time-to-First-Fix. An AT command can enable / disable the clients.
CellLocate [®]	Enables the estimation of device position based on the parameters of the mobile network cells visible to the specific device based on the CellLocate [®] database: <ul style="list-style-type: none"> • Normal scan: only the parameters of the visible home network cells are sent • Deep scan: the parameters of all surrounding cells of all mobile operators are sent CellLocate [®] is implemented using a set of AT commands that allow configuration and position request.
Hybrid Positioning	The module current position is provided using a u-blox positioning chip or module or the estimated position from CellLocate [®] depending on which positioning method provides the best and fastest solution according to the user configuration Hybrid positioning is implemented through a set of AT commands that allow configuration and position request.
Control Plan Aiding / LCS ⁶	Assisted GPS Location Services feature based on the Radio Resources Location Protocol (RRLP), according to 3GPP TS 44.031 [9] and Radio Resource Control (RRC), according to 3GPP TS 25.331 [18]. With the Assisted GPS feature, a location server provides the module with the GPS system information that otherwise needs to be downloaded from satellites. The feature allows faster position fixes, increases sensitivity and reduces module power consumption. The feature is invoked by the module through LCS Supplementary Services or by the Network during emergency calls.

⁶ Not supported by the "01", "x2", "63" and "68" product versions

Feature	Description
Firmware update Over AT commands (FOAT)	Firmware module upgrade over UART, USB and SPI interface using AT command. The firmware upgrade can be executed through the +UFWUPD AT command.
Firmware update Over The Air (FOTA) ⁷	Firmware module update over the 3G/2G air interface. The feature can be enabled and configured through the +UFWINSTALL AT command.
Rx Diversity ⁸	Improved link quality and reliability on all 2G and 3G operating bands except 2G DCS 1800.
Smart Temperature Supervisor	<p>Constant monitoring of the module board temperature:</p> <ul style="list-style-type: none"> Warning notification when the temperature approaches an upper or lower predefined threshold Shutdown notified and forced when the temperature value is outside the specified range (shutdown suspended in case of an emergency call in progress) <p>The feature can be enabled or disabled through the +USTS AT command.</p> <p> The sensor measures the board temperature, which can differ from ambient temperature.</p>
SIM Access Profile (SAP)	<p>Allows access and use of a remote (U)SIM card instead of the local SIM card directly connected to the module (U)SIM interface. The module acts as an SAP Client establishing a connection and performing data exchange to an SAP Server directly connected to the remote SIM.</p> <p>The modules provide a dedicated USB SAP channel and dedicated multiplexer SAP channel over UART and SPI for communication with the remote (U)SIM card.</p> <p>The feature can be configured and enabled by +USAPMODE and +USAPIND AT commands.</p>
BIP ⁶	Bearer Independent Protocol for Over-the-Air SIM provisioning. The data transfer to/from the SIM uses either an already active PDP context or a new PDP context established with the APN provided by the SIM card.
In-Band Modem ⁹	<p>In-Band modem solution for eCall and ERA-GLONASS emergency call applications over cellular networks implemented according to the 3GPP TS 26.267 specification [8].</p> <p>When activated, the in-vehicle eCall / ERA-GLONASS system (IVS) creates an emergency call carrying both voice and data (including vehicle position data) directly to the nearest Public Safety Answering Point (PSAP) to determine whether rescue services should be dispatched to the known position.</p>
DTMF decoder ⁹	<p>During a voice call, the Dual-Tone Multi-Frequency detector analyses the RX speech (coming from the remote party). The detected DTMF symbols can be output via the related URC.</p> <p>For more details, see the +UDTMFD AT command.</p>
Power saving	<p>The power saving configuration is disabled by default, but it can be configured using an AT command. When power saving is enabled, the module automatically enters the low power idle-mode whenever possible, reducing current consumption. During low power idle-mode, the module processor core runs with the RTC 32 kHz reference clock, which is generated by the internal 32 kHz oscillator</p> <p>The feature can be enabled through the +UPSV AT command.</p>
Automatic selection of authentication type ⁶	<p>Automatic selection of authentication type during PDP context activation. The module will sequentially try different authentication protocols (none/CHAP/PAP) until the authentication succeeds.</p> <p>The feature can be enabled through the +UPSD and +UAUTHREQ AT commands.</p>
Signal quality report for Packet Switched calls ⁶	The quality of the GPRS UL and/or DL connection is returned by the AT+CSQ command.
eMLPP ⁶	<p>Multi-Level Precedence and Pre-emption Service (eMLPP) permits to handle the call priority. The maximum priority associated to a user is set in the SIM: within this threshold, the user can assign different priorities to the calls; this results in a differentiated treatment of the calls by the network in case of abnormal events such as handovers to congested cells. The feature can be enabled by +CAEMLPP, +CPPS, +CAAP AT commands.</p>
Network Friendly Mode ⁶	<p>When the NFM is enabled, the module reacts to service request denials by using time-spaced, randomized or delayed retry schemes according to GSMA IoT Device Connection Efficiency Guidelines [19].</p> <p>The feature can be enabled through the +UNFM, +UNFMCONF and +URPM AT commands.</p>


⁷ Supported by “8x” product versions only

⁸ Not supported by LISA-U200, LISA-U201, LISA-U260 and LISA-U270

⁹ Not supported by “01” product version

Feature	Description
Ethernet (CDC-ECM) over USB interface ⁶	Ethernet (CDC-ECM) interface allowing networking from a HOST by means of the IP address received from the cellular network (bridge mode). The HOST configuration is performed via the DHCP protocol (a DHCP server is implemented). It operates as a non-exclusive alternative to PPP dial-up. The feature can be configured by +UUSBCONF and enabled by +UCEDATA AT commands.

Table 4: LISA-U2 series main supported features

-  u-blox is extremely mindful of user privacy. When a position is sent to the CellLocate[®] server, u-blox is unable to track the SIM used or the specific device.

2 Interfaces

2.1 Power management

2.1.1 Module supply (VCC)

Modules must be supplied through the **VCC** pin by a DC power supply. Voltages must be stable: during operation, the current drawn from **VCC** can vary by some order of magnitude, especially due to the surging consumption profile of the GSM system (described in the LISA-U2 series System Integration Manual [6]). It is important that the system power supply circuit is able to support the peak power.

2.1.2 RTC supply (V_BCKP)

V_BCKP is the Real Time Clock (RTC) supply. When the **VCC** voltage is within the valid operating range, the internal Power Management Unit (PMU) supplies the RTC and the same supply voltage is available on the **V_BCKP** pin. If the **VCC** voltage is under the minimum operating limit (e.g. during not powered mode), the **V_BCKP** pin can externally supply the RTC.

2.1.3 Digital I/O interfaces supply (V_INT)

LISA-U2 modules provide an internally generated supply rail output for digital interfaces (**V_INT**). This can be used in place of an external discrete regulator to supply pull-up resistors on the DDC interface. This optimizes the bill of materials for various applications, e.g. with u-blox GNSS receivers operating at 1.8 V.

2.2 RF antenna interface

The **ANT** pin has an impedance of 50 Ω and represents the main Tx/Rx antenna interface.

The **ANT_DIV** pin, provided only by LISA-U230 modules, has an impedance of 50 Ω and represents the Rx diversity antenna interface. The integrated diversity receiver provides improved link quality and reliability on all 2G and 3G operating bands except 2G DCS 1800.

2.3 System functions

2.3.1 Module power-on

LISA-U2 modules can be switched on in one of the following ways:

- Rising edge on the **VCC** pin to a valid voltage for module supply, i.e. applying module supply
- Low pulse on the **PWR_ON** pin, i.e. forcing the pin (normally high with external pull-up) to a low level for a valid time period (see section 4.2.6): **PWR_ON** pin requires an external pull-up resistor to set its value to logic high and may not be left floating
- Rising edge on the **RESET_N** pin, i.e. releasing the pin from the low level, normally high with internal pull-up
- RTC alarm, i.e. pre-programmed scheduled time by AT+CALA command

2.3.2 Module power-off

LISA-U2 modules can be switched off, with a complete storage of the current parameter settings and a network detach, in one of these ways:

- AT+CPWROFF command
- Low pulse on the **PWR_ON** pin for at least 1 s

An under-voltage shutdown occurs when the **VCC** supply drops below the extended operating range minimum limit, but in this case it is not possible to perform the storing of the current parameter settings in the module's non-volatile memory as well as the clean network detach.

An over-temperature or an under-temperature shutdown occurs when the temperature measured within the cellular module reaches the dangerous area, if the optional Smart Temperature Supervisor feature is enabled and configured by the dedicated AT command. For more details, see the LISA-U2 series System Integration Manual [6] and the u-blox AT commands manual [4], +USTS AT command.

2.3.3 Module reset

LISA-U2 modules can be properly reset (rebooted), with storage of current parameter settings and network detach, in this way:

- By the AT+CFUN command (see the u-blox AT Commands Manual [4]). This causes an “internal” or “software” reset of the baseband processor, excluding the integrated power management unit and the RTC internal block: the **V_INT** interfaces supply is enabled and each digital pin is set to its internal reset state (reported in Table 6), the **V_BCKP** supply and the RTC block are enabled. The current parameter settings are saved in the module's non-volatile memory and a clean network detach is performed.

An abrupt “external” or “hardware” reset occurs forcing a low level the **RESET_N** input pin, normally high with internal pull-up, for a valid time period (see section 4.2.7). This causes a reset of the entire module, including the integrated power management unit, except for the RTC internal block: the **V_INT** interfaces supply is switched off and all the digital pins are tri-stated, but the **V_BCKP** supply and the RTC block are enabled. The current parameter settings are not saved in the module's non-volatile memory and a clean network detach is not performed.

2.4 (U)SIM interface

A (U)SIM card interface is provided on the SMT pads of the LISA-U2 modules: the high-speed SIM/ME interface is implemented as well as automatic detection of the required SIM supporting voltage.

Both 1.8 V and 3 V SIM types are supported (1.8 V and 3 V ME). Activation and deactivation with automatic voltage switch from 1.8 V to 3 V is implemented, according to ISO-IEC 7816-3 specifications. The SIM driver supports the PPS (Protocol and Parameter Selection) procedure for baud-rate selection, according to the values offered by the SIM card.

2.5 Serial communication

LISA-U2 modules provide the following serial communication interfaces where AT command interface and Packet-Switched / Circuit-Switched Data communication are concurrently available:

- One asynchronous serial interface (UART)
- One Inter Processor Communication (IPC) interface: two handshake signals added to a SPI interface
- One high-speed USB 2.0 compliant interface

When used as AT command interface, all the serial communication interfaces listed above can be used for firmware upgrade using AT commands (for more details, see the u-blox AT Commands Manual [4] +UFWUPD), but only the following serial communication interfaces can be used for firmware upgrade using the u-blox Easy Flash tool:

- The UART interface, using the **RxD** and **TxD** lines only (the other UART lines are not needed)
- The USB interface, using all the provided lines (**VUSB_DET**, **USB_D+** and **USB_D-**)

2.5.1 Asynchronous serial interface (UART)

The UART interface is a 9-wire unbalanced asynchronous serial interface provided for all communications with LISA-U2 modules. The UART features are:

- Complete serial port with RS-232 functionality conforming to the ITU-T V.24 Recommendation [10], with CMOS compatible signal levels (0 V for low data bit or ON state and 1.8 V for high data bit or OFF state)
- Data lines (**RxD** as output, **TxD** as input), hardware flow control lines (**CTS** as output, **RTS** as input), modem status and control lines (**DTR** as input, **DSR** as output, **DCD** as output, **RI** as output) are provided
- Hardware flow control (default value), software flow control, or none flow control are supported
- Power saving indication available¹⁰ on the hardware flow control output (**CTS** line): the line is driven to the OFF state when the module is not prepared to accept data by the UART interface
- 1'200, 2'400, 4'800, 9'600, 19'200, 38'400, 57'600, 115'200, 230'400, 460'800 and 921'600 bit/s baud rates are supported for the AT interface
- Autobauding is enabled by default
- Frame format can be:
 - 8N2 (8 data bits, no parity, 2 stop bits)
 - 8N1 (8 data bits, no parity, 1 stop bit)
 - 8E1 (8 data bits, even parity, 1 stop bit)
 - 8O1 (8 data bits, odd parity, 1 stop bit)
 - 7E1 (7 data bits, even parity, 1 stop bit)
 - 7O1 (7 data bits, odd parity, 1 stop bit)
- Default frame configuration is 8N1

The UART serial interface can be conveniently configured through AT commands. For more details, refer to the u-blox AT Commands Manual [4] (+IPR, +ICF, +IFC, &K, \Q, +UPSV AT command) and the LISA-U2 series System Integration Manual [6].

2.5.1.1 Autobauding feature

Only one-shot autobauding is supported. This means that the baud rate detection is performed once, at module start-up.

After detection, the module works at the fixed baud rate (the detected one) and the baud rate can only be changed via the appropriate AT command (for more details, refer to the u-blox AT Commands Manual [4], +IPR).

- The module detects the followings baud rates (bit/s): 1'200, 2'400, 4'800, 9'600, 19'200, 38'400, 57'600, 115'200, 230'400
- The only detectable frame configurations are: 7E1, 7O1, 8N1, 8E1, 8O1

2.5.2 Universal Serial Bus (USB)

LISA-U2 series modules include a high-speed USB 2.0 compliant interface with a maximum 480 Mbit/s data rate. The module itself acts as a USB device and can be connected to any USB host.


The USB is the suitable interface for transferring high speed data between LISA-U2 series and a host processor, available for AT commands, data communication, FW upgrade by means of the FOAT feature, FW upgrade by means of the u-blox EasyFlash tool and for diagnostic purposes.

The **USB_D+** / **USB_D-** lines carry the USB serial data and signaling. The USB interface is automatically enabled by an external valid USB VBUS supply voltage (5.0 V typical) applied on the **VUSB_DET** pin.

¹⁰ If enabled

LISA-U2 series modules can provide the following functions over the USB interface:

- CDC-ACM for AT commands and data communication
- CDC-ACM for GNSS tunneling
- CDC-ACM for diagnostics
- CDC-ACM for SAP (SIM Access Profile)
- CDC-ECM for Ethernet-over-USB

 The CDC-ECM for Ethernet-over-USB function is not supported by the "01", "x2", "63" and "68" product versions.


The default configuration of the USB interface provides 7 USB CDC-ACM modem COM ports:

- USB1: AT and data
- USB2: AT and data
- USB3: AT and data
- USB4: GNSS tunneling
- USB5: Primary Log (diagnostic purposes)
- USB6: Secondary Log (diagnostic purposes)
- USB7: SAP (SIM Access Profile)

The user can concurrently use the AT command interface on one CDC and use Packet-Switched / Circuit-Switched Data communication on another CDC.

The USB interface can be configured by the AT+UUSBCONF command to provide a different set of functions, including 1 CDC-ECM for Ethernet-over-USB and 4 CDC-ACM modem COM ports enumerated as follows:

- USB1: AT and data
- USB2: GNSS tunneling
- USB3: Primary Log (diagnostic purposes)
- USB4: SAP (SIM Access Profile)

 The default profile of the USB interface cannot be changed on the "01", "x2", "63" and "68" product versions.

For more details regarding the USB configurations and capabilities, see the LISA-U2 series System Integration Manual [\[6\]](#) and the u-blox AT Commands Manual [\[4\]](#) (+UUSBCONF AT command).

USB drivers are available for the following operating system platforms:

- Windows XP
- Windows Vista
- Windows 7
- Windows 8
- Windows 8.1
- Windows 10
- Windows CE 5.0
- Windows Embedded CE 6.0
- Windows Embedded Compact 7
- Windows Embedded Automotive 7
- Windows Mobile 5
- Windows Mobile 6
- Windows Mobile 6.1
- Windows Mobile 6.5

LISA-U2 modules are compatible with the standard Linux/Android USB kernel drivers.

2.5.3 Serial Peripheral Interface (SPI)

The LISA-U2 modules provide a 5-wire Inter Processor Communication (IPC) interface that includes two handshake signals (**SPI_MRDY** and **SPI_SRDY**) added to a standard 3-wire SPI-compatible serial interface (**SPI_MOSI**, **SPI_MISO**, **SPI_SCLK**). The LISA-U2 modules run natively as an SPI slave.

The SPI / IPC interface can be used for high speed data transfer (UMTS/HSPA) between LISA-U2 modules and the host processor. The high speed communication (up to 26 Mbit/s) between the two processors is possible only if both sides follow the same Inter Processor Communication (IPC) specifications.

See the LISA-U2 series System Integration Manual [6] and the SPI Interface Application Note [14] for a detailed description of the implementation of the SPI / IPC protocol.

2.5.4 Multiplexer protocol

The LISA-U2 module has a software layer with MUX functionality, 3GPP TS 27.010 Multiplexer Protocol [3], available either on the UART or on the SPI physical link.

- The multiplexer protocol is not supported by the USB interface.

This is a data link protocol (layer 2 of OSI model) which uses HDLC-like framing and operates between the module (DCE) and the application processor (DTE) and allows simultaneous sessions over the used physical link (UART or SPI): the user can concurrently use AT command interface on one MUX channel and Packet-Switched / Circuit-Switched Data communication on another MUX channel.

The multiplexer protocol can be used on one serial interface (UART or SPI) at a time. Each session consists of a stream of bytes transferring various kinds of data such as SMS, CBS, PSD, GNSS, AT commands in general.

LISA-U2 modules provide the following virtual channels:

- Channel 0: control channel
- Channel 1 – 5: AT commands / data connection
- Channel 6: GNSS tunneling
- Channel 7: SAP (SIM Access Profile)

For more details, see the Mux Implementation Application Note [11].

2.6 DDC (I²C) bus interface

LISA-U2 series modules include an I²C compatible DDC interface that is available to communicate with a u-blox GNSS receiver and at the same time with an external I²C device as an audio codec: the LISA-U2 module acts as an I²C master which can communicate with two I²C slaves in accordance with the I²C bus specifications [13].

2.7 Audio

LISA-U2 modules have two 4-wire I²S digital audio interfaces:

- First 4-wire I²S digital audio interface (**I2S_CLK**, **I2S_RXD**, **I2S_TXD** and **I2S_WA**)
- Second 4-wire I²S digital audio interface (**I2S1_CLK**, **I2S1_RXD**, **I2S1_TXD** and **I2S1_WA**)

These audio paths are selected by parameters <main_uplink> and <main_downlink> in the AT+USPM command (for more details, see the u-blox AT Commands Manual [4]).

LISA-U2 modules provide a digital clock output (**CODEC_CLK**) for an external audio codec.

For further details about the hardware integration of the audio interface in an application design, see the LISA-U2 series System Integration Manual [6].

For further details about the possible settings of the audio interface, as well as the allowed input/output audio path combinations and as the default values related to the uplink/downlink path, see the u-blox AT Commands Manual [4], +USPM AT command.

2.8 GPIO

LISA-U2 modules provide up to 14 GPIO pins (**GPIO1-GPIO14**) which can be configured for general purpose input/output, or to provide the custom functions listed in Table 5 using u-blox AT commands (for further details, see the LISA-U2 series System Integration Manual [6] and the u-blox AT Commands Manual [4], +UGPIOC, +UGPIOR, +UGPIOW, +UGPS, +UGPRF, +USPM, +UDCONF=50).

Function	Description	Module	Default GPIO	Configurable GPIOs
GSM Tx-burst indication	GSM transmit slot indication	All	--	GPIO1
GNSS supply enable	Enable/disable the supply of u-blox GNSS receiver connected to cellular module	All	GPIO2	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5
GNSS data ready	Sense when u-blox GNSS receiver connected to cellular module is ready for sending data by the DDC (I ² C)	All	GPIO3	GPIO3
GNSS RTC sharing	RTC (Real Time Clock) synchronization signal to u-blox GNSS receiver connected to cellular module	All	GPIO4	GPIO4
SIM card detection	SIM card presence	All	GPIO5	GPIO5
SIM card hot insertion/removal	SIM card hot insertion/removal	All	--	GPIO5
Network status indication	Network status: registered 2G / 3G home network, registered 2G / 3G roaming, 2G / 3G data transmission, no service	All	--	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5
Module status indication	Module status: power off mode, i.e. module switched off, versus idle, active or connected mode, i.e. module switched on	All	--	GPIO1, GPIO13
Module operating mode indication	Module operating mode: idle mode versus active or connected mode	All	--	GPIO5, GPIO14
I ² S digital audio interface	Second I ² S digital audio interface (I2S1_RXD, I2S1_TXD, I2S1_CLK, I2S1_WA respectively)	All	GPIO6, GPIO7, GPIO8, GPIO9	GPIO6, GPIO7, GPIO8, GPIO9
SPI serial interface	SPI / IPC serial interface (SPI_SCLK, SPI_MOSI, SPI_MISO, SPI_SRDY and SPI_MRDI respectively)	All	GPIO10, GPIO11, GPIO12, GPIO13, GPIO14	GPIO10, GPIO11, GPIO12, GPIO13, GPIO14
General purpose input	Input to sense high or low digital level	All	--	All
General purpose output	Output to set the high or the low digital level	All	--	All
Pad disabled	Tri-state with an internal active pull-down enabled	All	GPIO1	All

Table 5: GPIO custom functions configuration

3 Pin definition

3.1 Pin assignment

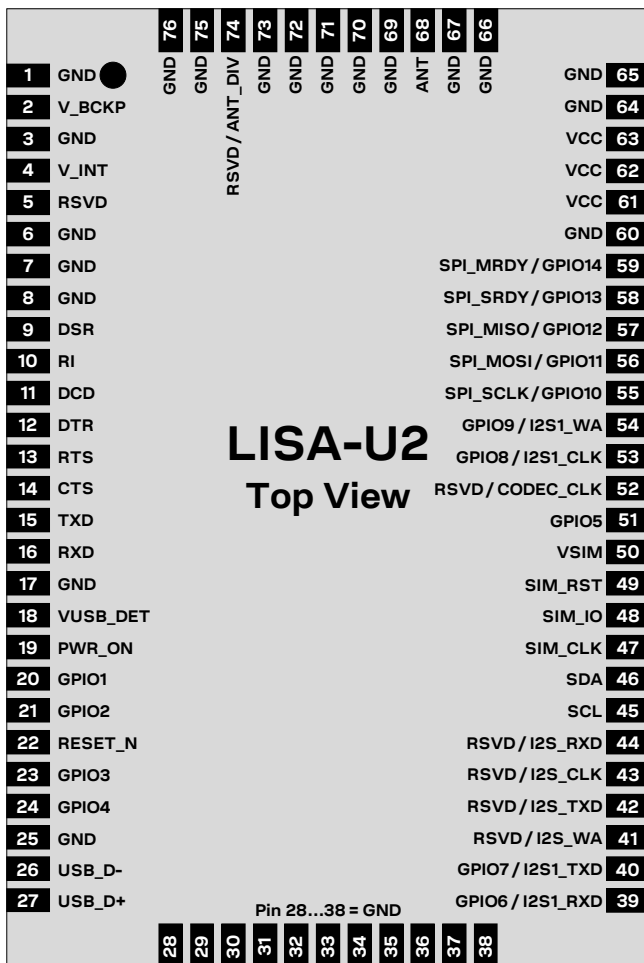


Figure 2: LISA-U2 series pin assignment

No	Module	Name	Power domain	I/O	Description	Remarks
1	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
2	All	V_BCKP	-	I/O	Real Time Clock supply input/output	V_BCKP = 1.8 V (typical) generated by the module to supply the Real Time Clock when VCC supply voltage is within valid operating range. A backup battery can be connected to this pin to supply the Real Time Clock when VCC supply voltage is not within valid operating range. See section 4.2.3 for detailed electrical specs.
3	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
4	All	V_INT	-	O	Digital I/O Interfaces supply output	V_INT = 1.8V (typical) generated by the module when it is switched on and the RESET_N (external reset input pin) is not forced to the low level. See section 4.2.3 for detailed electrical specs.
5	All	RSVD	-	N/A	RESERVED pin	This pin has special function: it must be connected to GND to allow module to work properly.

No	Module	Name	Power domain	I/O	Description	Remarks
6	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
7	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
8	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
9	All	DSR	GDI	O	UART data set ready	Circuit 107 (DSR) in ITU-T V.24. Output driver class D. PU/PD class a. Value at internal reset: T/PU. See section 4.2.9 for detailed electrical specs.
10	All	RI	GDI	O	UART ring indicator	Circuit 125 (RI) in ITU-T V.24. Output driver class C ₀ . PU/PD class c. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
11	All	DCD	GDI	O	UART data carrier detect	Circuit 109 (DCD) in ITU-T V.24. Output driver class C ₀ . PU/PD class c. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
12	All	DTR	GDI	I	UART data terminal ready	Circuit 108/2 (DTR) in ITU-T V.24. Internal active pull-up to V _{INT} enabled. PU/PD class c. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
13	All	RTS	GDI	I	UART ready to send	Circuit 105 (RTS) in ITU-T V.24. Internal active pull-up to V _{INT} enabled. PU/PD class a. Value at internal reset: T/PU. See section 4.2.9 for detailed electrical specs.
14	All	CTS	GDI	O	UART clear to send	Circuit 106 (CTS) in ITU-T V.24. Output driver class A. PU/PD class a. Value at internal reset: T/PU. See section 4.2.9 for detailed electrical specs.
15	All	TXD	GDI	I	UART transmitted data	Circuit 103 (TxD) in ITU-T V.24. Internal active pull-up to V _{INT} enabled. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
16	All	RXD	GDI	O	UART received data	Circuit 104 (Rx) in ITU-T V.24. Output driver class A. PU/PD class a. Value at internal reset: T/PU. See section 4.2.9 for detailed electrical specs.
17	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
18	All	VUSB_DETECT	USB	I	USB detect input	Input for VBUS (5 V typical) USB supply sense. See section 4.2.10 for detailed electrical specs.
19	All	PWR_ON	POS	I	Power-on input	The PWR_ON pin has high input impedance: don't leave it floating in noisy environment (an external pull-up resistor is required) See section 4.2.6 for detailed electrical specs.
20	All	GPIO1	GDI	I/O	GPIO	Output driver class A. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
21	All	GPIO2	GDI	I/O	GPIO	Output driver class E. PU/PD class b. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
22	All	RESET_N	ERS	I	External reset input	Internal 10 kΩ pull-up resistor to V _{BCKP} . See section 4.2.7 for detailed electrical specs.
23	All	GPIO3	GDI	I/O	GPIO	Output driver class A. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
24	All	GPIO4	GDI	I/O	GPIO	Output driver class A. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.

No	Module	Name	Power domain	I/O	Description	Remarks
25	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
26	All	USB_D-	USB	I/O	USB Data Line D-	90 Ω nominal differential impedance Pull-up or pull-down resistors and external series resistors as required by the USB 2.0 high-speed specification [12] are part of the USB pin driver and need not be provided externally. Value at internal reset: T. See section 4.2.10 for detailed electrical specs.
27	All	USB_D+	USB	I/O	USB Data Line D+	90 Ω nominal differential impedance Pull-up or pull-down resistors and external series resistors as required by the USB 2.0 high-speed specification [12] are part of the USB pin driver and need not be provided externally. Value at internal reset: T. See section 4.2.10 for detailed electrical specs.
28	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
29	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
30	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
31	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
32	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
33	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
34	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
35	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
36	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
37	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
38	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
39	All	I2S1_RXD / GPIO6	GDI	I / I/O	2 nd I ² S receive data / GPIO	Can be configured as receive data input of the second digital audio interface (with internal active pull-down to GND enabled), or as GPIO. Output driver class E. PU/PD class b. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
40	All	I2S1_TXD / GPIO7	GDI	O / I/O	2 nd I ² S transmit data / GPIO	Can be configured as transmit data output of the second digital audio interface, or as GPIO. Output driver class E. PU/PD class b. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
41	All	I2S_WA	GDI	I/O	1 st I ² S word alignment	Input with internal active pull-down to GND enabled in slave mode, Output in master mode. Output driver class C. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
42	All	I2S_TXD	GDI	O	1 st I ² S transmit data	Output driver class C. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
43	All	I2S_CLK	GDI	I/O	1 st I ² S clock	Input with internal active pull-down to GND enabled in slave mode, Output in master mode. Output driver class C. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
44	All	I2S_RXD	GDI	I	1 st I ² S receive data	Internal active pull-down to GND enabled. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.

No	Module	Name	Power domain	I/O	Description	Remarks
45	All	SCL	DDC	O	I ² C bus clock line	Fixed open drain. No internal pull-up. Value at internal reset: T. See section 4.2.11 for detailed electrical specs.
46	All	SDA	DDC	I/O	I ² C bus data line	Fixed open drain. No internal pull-up. Value at internal reset: T. See section 4.2.11 for detailed electrical specs.
47	All	SIM_CLK	SIM	O	SIM clock	Value at internal reset: L. See section 4.2.8 for detailed electrical specs.
48	All	SIM_IO	SIM	I/O	SIM data	Internal 4.7 kΩ pull-up resistor to VSIM. Value at internal reset: L/PD. See section 4.2.8 for detailed electrical specs.
49	All	SIM_RST	SIM	O	SIM reset	Value at internal reset: L. See section 4.2.8 for detailed electrical specs.
50	All	VSIM	-	O	SIM supply output	VSIM = 1.80 V typical or 2.90 V typical generated by the module according to the SIM card type. See section 4.2.3 for detailed electrical specs.
51	All	GPIO5	GDI	I/O	GPIO	Output driver class A. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
52	All	CODEC_C LK	GDI	O	Clock output	Output driver class B. PU/PD class b. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
53	All	I2S1_CLK / GPIO8	GDI	I/O / I/O	2 nd I ² S clock / GPIO	Can be configured as clock (Input with internal active pull-down to GND enabled in slave mode, Output in master mode) of the second digital audio interface, or as GPIO. Output driver class E. PU/PD class b. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
54	All	I2S1_WA / GPIO9	GDI	I/O / I/O	2 nd I ² S word alignment / GPIO	Can be configured as word alignment (Input with internal active pull-down to GND enabled in slave mode, Output in master mode) of the second digital audio interface, or as GPIO. Output driver class E. PU/PD class b. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
55	All	SPI_SCLK / GPIO10	GDI	I / I/O	SPI Serial Clock Input / GPIO	Can be set as SPI Serial Clock Input, or as GPIO When configured as SPI Serial Clock: <ul style="list-style-type: none"> • Idle low (CPOL=0) • Internal active pull-down to GND enabled. Output driver class A. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
56	All	SPI_MOSI / GPIO11	GDI	I / I/O	SPI Data Line Input / GPIO	Can be set as SPI Data Line Input, or as GPIO When configured as SPI Data Line Input: <ul style="list-style-type: none"> • Shift data on rising clock edge (CPHA=1) • Latch data on falling clock edge (CPHA=1) • Idle high. • Internal active pull-up to V_INT enabled. Output driver class A. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.

No	Module	Name	Power domain	I/O	Description	Remarks
57	All	SPI_MISO / GPIO12	GDI	O / I/O	SPI Data Line Output / GPIO	Can be set as SPI Data Line Output, or as GPIO When configured as SPI Data Line Output: <ul style="list-style-type: none"> • Shift data on rising clock edge (CPHA=1) • Latch data on falling clock edge (CPHA=1) • Idle high Output driver class A. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
58	All	SPI_SRDY / GPIO13	GDI	O / I/O	SPI Slave Ready Output / GPIO	Can be set as SPI Slave Ready Output, or as GPIO When configured as SPI Slave Ready Output: <ul style="list-style-type: none"> • Idle low Output driver class A. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
59	All	SPI_MRDY , GPIO14	GDI	I / I/O	SPI Master Ready Input / GPIO	Can be set as SPI Master Ready Input, or as GPIO When configured as SPI Master Ready Input: <ul style="list-style-type: none"> • Idle low • Internal active pull-down to GND enabled Output driver class A. PU/PD class a. Value at internal reset: T/PD. See section 4.2.9 for detailed electrical specs.
60	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
61	All	VCC	-	I	Module supply input	All VCC pins must be connected to external supply
62	All	VCC	-	I	Module supply input	All VCC pins must be connected to external supply
63	All	VCC	-	I	Module supply input	All VCC pins must be connected to external supply
64	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
65	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
66	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
67	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
68	All	ANT	-	I/O	RF input/output for main Tx/Rx antenna	50 Ω nominal impedance
69	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
70	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
71	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
72	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
73	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
74	All except LISA-U230	RSVD	-	N/A	RESERVED pin	Leave unconnected.
	LISA-U230	ANT_DIV	-	I	RF input for Rx diversity antenna	50 Ω nominal impedance
75	All	GND	-	N/A	Ground	All GND pins must be connected to ground.
76	All	GND	-	N/A	Ground	All GND pins must be connected to ground.





Table 6: LISA-U2 series module pin-out


For more information about pinouts, see the LISA-U2 series System Integration Manual [6].




For an explanation of the abbreviations and terms used, see Appendix A.

4 Electrical specifications


-  Stressing the device above one or more of the ratings listed in the Absolute Maximum Rating section may cause permanent damage. These are stress ratings only. Operating the module at these or at any conditions other than those specified in the Operating Conditions sections (section 4.2) of the specification should be avoided. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.
-  Operating conditions ranges define those limits within which the functionality of the device is guaranteed.
-  Electrical characteristics are defined according to verification on a representative number of samples or according to simulation.
-  Where application information is given, it is advisory only and does not form part of the specification.

4.1 Absolute maximum rating

-  Limiting values given below are in accordance with the Absolute Maximum Rating System (IEC 134).

Symbol	Description	Condition	Min.	Max.	Unit
VCC	Module supply voltage	Input DC voltage at VCC pin	-0.30	5.50	V
VUSB_DET	USB detection pin	Input DC voltage at VUSB_DET	-0.30	5.35	V
USB	USB D+/D- pins	Input DC voltage at USB_D+ and USB_D-	-1.00	5.35	V
V_BCKP	RTC supply voltage	Input DC voltage at V_BCKP pin	-0.15	2.00	V
GDI	Generic digital interfaces	Input DC voltage at Generic digital interfaces pins	-0.30	3.60	V
DDC	DDC interface	Input DC voltage at DDC interface pins	-0.30	3.60	V
SIM	SIM interface	Input DC voltage at SIM interface pin	-0.30	3.60	V
ERS	External reset signal	Input DC voltage at External reset signal pin	-0.15	2.10	V
POS	Power-on input	Input DC voltage at Power-on signal pin	-0.30	5.50	V
V_ANT	Antenna voltage	Input DC voltage at ANT pin	-0.15	3.00	V
P_ANT	Antenna power	Input in-band RF power at ANT pin		-8	dBm
Rho_ANT	Antenna ruggedness	Output RF load mismatch ruggedness at ANT pin		10:1	VSWR
Tstg	Storage temperature		-40	+90	°C

Table 7: Absolute maximum ratings

-  The product is not protected against overvoltage or reversed voltages. If necessary, voltage spikes exceeding the power supply voltage specification, given in the table above, must be limited to values within the specified boundaries by using appropriate protection devices.

4.1.1 Maximum ESD

Parameter	Module	Min.	Typ.	Max.	Unit	Remarks
ESD sensitivity for all pins except ANT and ANT_DIV pins	All			1000	V	Human Body Model as per JESD22-A114F
ESD sensitivity for ANT pin	All			1000	V	Human Body Model as per JESD22-A114F
ESD sensitivity for ANT_DIV pin	LISA-U230			1000	V	Human Body Model as per JESD22-A114F
ESD immunity for ANT pin	All			1000	V	Contact Discharge as per IEC 61000-4-2
				1000	V	Air Discharge as per IEC 61000-4-2
ESD immunity for ANT_DIV pin	LISA-U230			4000	V	Contact Discharge as per IEC 61000-4-2
				8000	V	Air Discharge as per IEC 61000-4-2

Table 8: Maximum ESD ratings

- LISA-U2 modules are Electrostatic Sensitive Devices (ESD) and require special precautions when handling.

4.2 Operating conditions

- Unless otherwise indicated, all operating condition specifications are at an ambient temperature of +25 °C.
- Operation beyond the operating conditions is not recommended and extended exposure beyond them may affect device reliability.

4.2.1 Operating temperature range

Symbol	Parameter	Min.	Typ.	Max.	Units	Remarks
Topr	Operating temperature range	-40		+85	°C	
		-20		+65	°C	Normal operating temperature range See section 4.2.1.1
		-40		-20	°C	Extended operating temperature range 1 See section 4.2.1.2
		+65		+85	°C	Extended operating temperature range 2 See section 4.2.1.3

Table 9: Environmental conditions

4.2.1.1 Normal operating temperature range

The cellular module is fully functional and meets the 3GPP specification across the specified temperature range.

4.2.1.2 Extended operating temperature range 1

The cellular module is fully functional across the specified temperature range. Occasional deviations from the 3GPP specification may occur.

4.2.1.3 Extended operating temperature range 2

The cellular module is functional across the specified temperature range. Occasional deviations from the 3GPP specification may occur. Thermal protection including automatic shutdown is implemented for protection against overheating. Thermal protection is disabled for emergency calls. For more details, see the u-blox AT Commands Manual [\[4\]](#), +USTS AT command).

4.2.2 Module thermal resistance

Symbol	Parameter	Min.	Typ.	Max.	Units	Remarks
R _{th,M-A}	Module-to-Ambient thermal resistance	7		12	°C/W	Thermal resistance from the module internal temperature sensor to the ambient, with the module mounted on a 90 mm x 70 mm x 1.46 mm 4-layer PCB with a high coverage of copper in still air conditions
R _{th,M-C}	Module-to-Case thermal resistance	1.5		3.5	°C/W	Thermal resistance from the module internal temperature sensor to the module case, evaluated as the thermal resistance from the module internal temperature sensor to the ambient, with the module mounted on a 90 mm x 70 mm x 1.46 mm 4-layer PCB with a high coverage of copper, with a robust aluminum heat sink on the back of the application board, with forced air ventilation

Table 10: Module thermal resistance

4.2.3 Supply/Power pins

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Module supply normal operating input voltage ¹¹	3.30	3.80	4.40	V
	Module supply extended operating input voltage ¹²	3.10		4.50	V
V_BCKP	RTC supply input voltage	1.00	1.80	1.90	V
I_BCKP	RTC supply average current consumption, at V_BCKP = 1.8 V		2.00		μA

Table 11: Input characteristics of the supply/power pins

Symbol	Parameter	Min.	Typ.	Max.	Unit
VSIM	SIM supply output voltage	1.76	1.80	1.83	V
		2.84	2.90	2.94	V
V_BCKP	RTC supply output voltage	1.71	1.80	1.89	V
I_BCKP	RTC supply output current capability			3	mA
V_INT	Digital I/O Interfaces supply output voltage	1.73	1.80	1.87	V
V_INT_RIPPLE	Digital I/O Interfaces supply output peak-to-peak voltage ripple during active or connected mode			15	mV
	Digital I/O Interfaces supply output peak-to-peak voltage ripple during low power idle mode with power saving enabled by AT+UPSV command			70	mV
I_INT	Digital I/O Interfaces supply output current capability			70	mA

Table 12: Output characteristics of the supply/power pins

¹¹ Input voltage at **VCC** must be above the normal operating range minimum limit to switch on the module.

¹² Occasional deviations from the 3GPP specifications may occur. Ensure that input voltage at **VCC** never drops below the extended operating range minimum limit during module operation: the wireless module may switch off when the **VCC** voltage value drops below the extended operating range minimum limit.

4.2.4 Current consumption

Table 13 details the LISA-U2 modules average current consumption through the **VCC** pins in the listed conditions¹³.

Mode	Condition	Band	Min	Typ	Max	Unit
Power Off Mode	Averaged current, module switched off			55	60	μA
Idle-Mode (Power Saving enabled by AT+UPSV, module in low power idle-mode, equivalent to +CFUN=0 or +COPS=2)	Averaged current over a 100-ms period, USB interface disconnected			0.6		mA
	Averaged current over a 100-ms period, USB interface connected and suspended			1.0		mA
2G Cyclic Idle/Active-Mode (Power Saving enabled by AT+UPSV, Module registered with network)	Averaged current over a 10-minute period, DRX = 9 ¹⁴ , AT+UPSV=2 or 3, USB disconnected	All		0.9	1.0	mA
	Averaged current over a 10-minute period, DRX = 5 ¹⁵ , AT+UPSV=1, USB disconnected	All		1.3	1.5	mA
	Averaged current over a 10-minute period, DRX = 5, AT+UPSV=1, USB suspended ¹⁵	All		1.7	2.0	mA
2G Active-Mode (Power Saving disabled by AT+UPSV=0, Module registered with network)	Averaged current over a 10-minute period, DRX = 5, USB disconnected	All		13.0		mA
	Averaged current over a 10-minute period, DRX = 5, USB connected and not suspended	All		36.8		mA
GSM Connected Mode (Tx / Rx call enabled)	Peak current ¹⁶ during a 1-slot Tx burst Maximum Tx power	GSM 850, EGSM 900		1.8	2.5	A
	Averaged current over a 10-second period, 1 Tx + 1 Rx slot, Maximum Tx power	GSM 850, EGSM 900		230	260	mA
	Averaged current over a 10-second period, 1 Tx + 1 Rx slot, Maximum Tx power	DCS 1800, PCS 1900		170	220	mA
GPRS Connected Mode (Tx / Rx call enabled)	Averaged current over a 10-second period, 4 Tx + 1 Rx slots, Maximum Tx power ¹⁷	GSM 850, EGSM 900		550	600	mA
	Averaged current over a 10-second period, 4 Tx + 1 Rx slots, Maximum Tx power ¹⁷	DCS 1800, PCS 1900		400	450	mA
EDGE Connected Mode (Tx / Rx call enabled)	Averaged current over a 10-second period, 4 Tx + 1 Rx slots, Maximum Tx power ¹⁷	GSM 850, EGSM 900		460	510	mA
	Averaged current over a 10-second period, 4 Tx + 1 Rx slots, Maximum Tx power ¹⁷	DCS 1800, PCS 1900		450	500	mA

¹³ It is assumed that no significant load is connected to any digital and analog pin except for antenna.

¹⁴ Module is registered with the network, with a paging period of 2.12 s (2G network DRX setting = 9), with no neighbour cell.

¹⁵ Module is registered with the network, with a paging period of 1.18 s (2G network DRX setting = 5), with 16 neighbour cells.

¹⁶ It is recommended to use this figure to dimension maximum current capability of power supply.

¹⁷ Condition for GPRS and EDGE multi-slot output power: Multi-Slot Power Reduction profile 2 (+UDCONF=40 AT command default value).

Mode	Condition	Band	Min	Typ	Max	Unit
3G Cyclic Idle/Active-Mode (Power Saving enabled by AT+UPSV, Module registered with network)	Averaged current over a 10-minute period, DRX = 9 ¹⁸ , AT+UPSV=2 or 3, USB disconnected	All		1.0	1.2	mA
	Averaged current over a 10-minute period, DRX = 7 ¹⁹ , AT+UPSV=1, USB disconnected	All		1.4	1.5	mA
	Averaged current over a 10-minute period, DRX = 7 ¹⁹ , AT+UPSV=1, USB suspended	All		1.8	2.0	mA
3G Active-Mode (Power Saving disabled by AT+UPSV=0, Module registered with network)	Averaged current over a 10-minute period, DRX = 7, USB disconnected ¹⁹	All		12.5		mA
	Averaged current over a 10-minute period, DRX = 7, USB connected and not suspended ¹⁹	All		35.4		mA
UMTS Connected Mode (Tx / Rx call enabled)	Averaged current over a 10-second period, 12.2 kbit/s UL, 12.2 kbit/s DL Tx power = -50 dBm	Band I		115		mA
		Band II		115		mA
		Band IV		110		mA
		Band V, VI		118		mA
		Band VIII		117		mA
	Averaged current over a 10-second period, 12.2 kbit/s UL, 12.2 kbit/s DL Tx power = 0 dBm	Band I		125		mA
		Band II		121		mA
		Band IV		120		mA
		Band V, VI		119		mA
		Band VIII		120		mA
	Averaged current over a 10-second period, 12.2 kbit/s UL, 12.2 kbit/s DL Tx power = 12 dBm	Band I		180		mA
		Band II		178		mA
		Band IV		165		mA
		Band V, VI		167		mA
		Band VIII		168		mA
	Averaged current over a 10-second period, 12.2 kbit/s UL, 12.2 kbit/s DL Tx power = 18 dBm	Band I		255		mA
		Band II		267		mA
		Band IV		242		mA
		Band V, VI		220		mA
		Band VIII		234		mA
Averaged current over a 10-second period, 12.2 kbit/s UL, 12.2 kbit/s DL Maximum Tx power	Band I		475	600	mA	
	Band II		510	640	mA	
	Band IV		450	600	mA	
	Band V, VI		385	490	mA	
	Band VIII		425	490	mA	
HSDPA Connected Mode (Tx / Rx call enabled)	Averaged current over a 10-second period, Maximum DL data rate (HSDPA) Maximum Tx power	Band I		590	650	mA
		Band II		590	690	mA
		Band IV		580	650	mA
		Band V, VI		460	550	mA
		Band VIII		490	550	mA
HSUPA or HSPA Connected Mode (Tx / Rx call enabled)	Averaged current over a 10-second period, Maximum UL data rate (HSUPA) or Maximum both UL/DL data rate (HSPA) Maximum Tx power	Band I		540	620	mA
		Band II		540	660	mA
		Band IV		530	650	mA
		Band V, VI		395	500	mA
		Band VIII		425	500	mA

Table 13: VCC current consumption
¹⁸ Module is registered with the network, with a paging period of 5.12 s (3G network DRX setting = 9).

¹⁹ Module is registered with the network, with a paging period of 1.28 s (3G network DRX setting = 7).

4.2.5 RF characteristics

The 3G and 2G bands supported by each LISA-U2 series module are defined in [Table 2](#), while the following [Table 14](#) lists the Tx and Rx frequencies for each band, according to 3GPP TS 34.121-1 [15] and 3GPP TS 51.010-1 [16].

Parameter		Min.	Max.	Unit	Remarks
Frequency range GSM 850	Uplink	824	849	MHz	Module transmit
	Downlink	869	894	MHz	Module receive
Frequency range E-GSM 900	Uplink	880	915	MHz	Module transmit
	Downlink	925	960	MHz	Module receive
Frequency range DCS 1800	Uplink	1710	1785	MHz	Module transmit
	Downlink	1805	1880	MHz	Module receive
Frequency range PCS 1900	Uplink	1850	1910	MHz	Module transmit
	Downlink	1930	1990	MHz	Module receive
Frequency range UMTS 800 (band VI)	Uplink	830	840	MHz	Module transmit
	Downlink	875	885	MHz	Module receive
Frequency range UMTS 850 (band V)	Uplink	824	849	MHz	Module transmit
	Downlink	869	894	MHz	Module receive
Frequency range UMTS 900 (band VIII)	Uplink	880	915	MHz	Module transmit
	Downlink	925	960	MHz	Module receive
Frequency range UMTS 1700 (band IV)	Uplink	1710	1755	MHz	Module transmit
	Downlink	2110	2155	MHz	Module receive
Frequency range UMTS 1900 (band II)	Uplink	1850	1910	MHz	Module transmit
	Downlink	1930	1990	MHz	Module receive
Frequency range UMTS 2100 (band I)	Uplink	1920	1980	MHz	Module transmit
	Downlink	2110	2170	MHz	Module receive

Table 14: Operating RF frequency bands

LISA-U2 series modules include a UE Power Class 3 3G transmitter, an EDGE Power Class E2 transmitter, a GMSK Power Class 4 transmitter for GSM/E-GSM bands and a GMSK Power Class 1 transmitter for DCS/PCS bands (see [Table 2](#)). Output power and characteristics are compliant with 3GPP TS 34.121-1 [15], 3GPP TS 51.010-1 [16].

LISA-U2 series modules 3G and 2G receiver characteristics are compliant with 3GPP TS 34.121-1 [15] and 3GPP TS 51.010-1 [16], with conducted receiver sensitivity performance specified in [Table 15](#).

Parameter	Min.	Typ.	Max.	Unit	Remarks
Receiver input sensitivity GSM 850 / E-GSM 900	-102.0	-110.0		dBm	Downlink RF level @ BER Class II < 2.4%
Receiver input sensitivity DCS 1800 / PCS 1900	-102.0	-109.0		dBm	Downlink RF level @ BER Class II < 2.4%
Receiver input sensitivity UMTS 800 (band VI)	-106.7	-111.0		dBm	Downlink RF level for RMC @ BER < 0.1%
Receiver input sensitivity UMTS 850 (band V)	-104.7	-112.0		dBm	Downlink RF level for RMC @ BER < 0.1%
Receiver input sensitivity UMTS 900 (band VIII)	-103.7	-111.0		dBm	Downlink RF level for RMC @ BER < 0.1%
Receiver input sensitivity UMTS 1700 (band IV)	-106.7	-111.0		dBm	Downlink RF level for RMC @ BER < 0.1%
Receiver input sensitivity UMTS 1900 (band II)	-104.7	-111.0		dBm	Downlink RF level for RMC @ BER < 0.1%
Receiver input sensitivity UMTS 2100 (band I)	-106.7	-111.0		dBm	Downlink RF level for RMC @ BER < 0.1%

Condition: 50 Ω source

Table 15: Receiver sensitivity performance

4.2.6 PWR_ON pin

Pin Name	Parameter	Min.	Typ.	Max.	Unit	Remarks
PWR_ON	Internal supply for Power-On Input Signal	1.71	1.80	1.89	V	RTC supply (V_BCKP)
	L-level input	-0.30		0.65	V	High input impedance (no internal pull-up)
	H-level input	1.50		4.40	V	High input impedance (no internal pull-up)
	L-level input current		-6		μA	
	PWR_ON low time to switch on the module	50		80	μs	
	PWR_ON low time to switch off the module	1000			ms	

Table 16: PWR_ON pin characteristics (POS domain)

4.2.7 RESET_N pin

Pin Name	Parameter	Min.	Typ.	Max.	Unit	Remarks
RESET_N	Internal supply for External Reset Input Signal	1.71	1.80	1.89	V	RTC supply (V_BCKP)
	L-level input	-0.30		0.51	V	
	H-level input	1.32		2.01	V	
	L-level input current		-180		μA	
	Pull-up resistance		10		kΩ	Internal pull-up to RTC supply (V_BCKP)
	RESET_N low time to perform an HW reset	50			ms	Specification for LISA-U200, LISA-U230, LISA-U260 and LISA-U270 modules
	RESET_N low time to perform an HW reset	500			ms	Specification for LISA-U201 modules

Table 17: RESET_N pin characteristics (ERS domain)

4.2.8 (U)SIM pins

The SIM pins are a dedicated interface to the (U)SIM chip card/IC. The electrical characteristics fulfill the regulatory specification requirements. The values in [Table 18](#) are for information only.

Parameter	Min.	Typ.	Max.	Unit	Remarks
Low-level input	0.00		0.35	V	VSIM = 1.80 V
	0.00		0.57	V	VSIM = 2.90 V
High-level input	1.29		3.30	V	VSIM = 1.80 V
	2.07		3.30	V	VSIM = 2.90 V
Low-level output		0.00	0.35	V	VSIM = 1.80 V, Max value at I _{OL} = +1.0 mA
		0.00	0.35	V	VSIM = 2.90 V, Max value at I _{OL} = +1.0 mA
High-level output	1.26	1.80		V	VSIM = 1.80 V, Min value at I _{OH} = -1.0 mA
	2.03	2.90		V	VSIM = 2.90 V, Min value at I _{OH} = -1.0 mA
Input/Output leakage current			0.7	μA	0.2V < V _{IN} < 3.3V
Internal pull-up resistor on SIM_IO to VSIM		4.7		kΩ	
Clock frequency on SIM_CLK		3.25		MHz	

Table 18: (U)SIM pin characteristics (SIM domain)

4.2.9 Generic Digital Interface pins

Parameter	Min.	Typ.	Max.	Unit	Remarks
Internal supply for GDI domain	1.73	1.80	1.87	V	Digital I/O Interfaces supply (V_INT)
Input characteristic: L-level input	-0.20		0.35	V	
Input characteristic: H-level input	1.31		1.93	V	
Output characteristics: L-level output		0.00	0.20	V	Max value at I _{OL} = +0.1 mA for driver class A
		0.00	0.35	V	Max value at I _{OL} = +6.0 mA for driver class A
		0.00	0.20	V	Max value at I _{OL} = +0.1 mA for driver class B
		0.00	0.35	V	Max value at I _{OL} = +4.0 mA for driver class B
		0.00	0.20	V	Max value at I _{OL} = +0.1 mA for driver class C
		0.00	0.35	V	Max value at I _{OL} = +2.0 mA for driver class C
		0.00	0.45	V	Max value at I _{OL} = +2.0 mA for driver class C_0
		0.00	0.20	V	Max value at I _{OL} = +0.1mA for driver class D
		0.00	0.35	V	Max value at I _{OL} = +1.0 mA for driver class D
Output characteristics: H-level output		0.00	0.20	V	Max value at I _{OL} = +0.1 mA for driver class E
	1.45	1.80		V	Min value at I _{OH} = -6.0 mA for driver class A
	1.60	1.80		V	Min value at I _{OH} = -0.1 mA for driver class A
	1.45	1.80		V	Min value at I _{OH} = -4.0 mA for driver class B
	1.60	1.80		V	Min value at I _{OH} = -0.1 mA for driver class B
	1.45	1.80		V	Min value at I _{OH} = -2.0 mA for driver class C
	1.60	1.80		V	Min value at I _{OH} = -0.1 mA for driver class C
	1.35	1.80		V	Min value at I _{OH} = -2.0 mA for driver class C_0
	1.45	1.80		V	Min value at I _{OH} = -1.0 mA for driver class D
	1.60	1.80		V	Min value at I _{OH} = -0.1 mA for driver class D
	1.60	1.80		V	Min value at I _{OH} = -0.1 mA for driver class E
Input/Output leakage current			0.7	μA	0.2 V < V _{IN} < 1.93 V
Pull-up input current			-240	μA	PU Class a
			-150	μA	PU Class b
			-125	μA	PU Class c
Pull-down input current			+200	μA	PD Class a
			+150	μA	PD Class b
			+45	μA	PD Class c

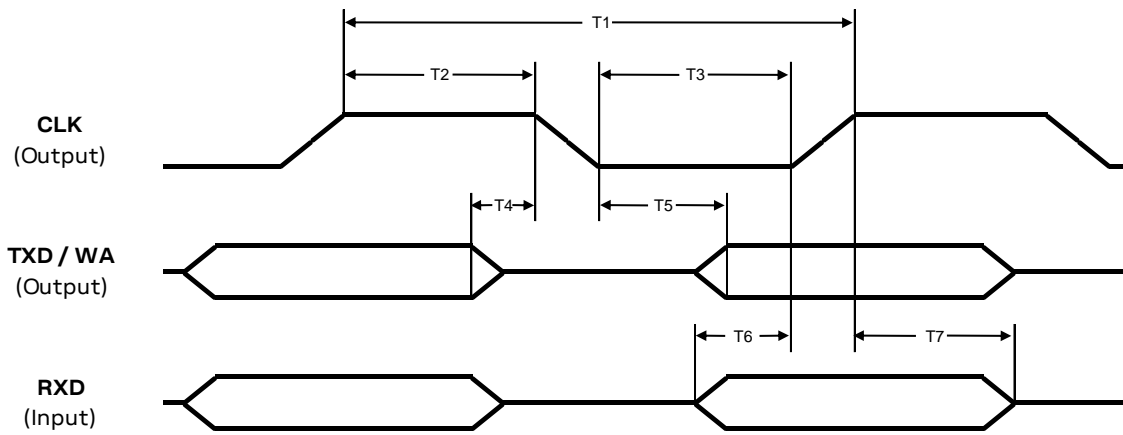
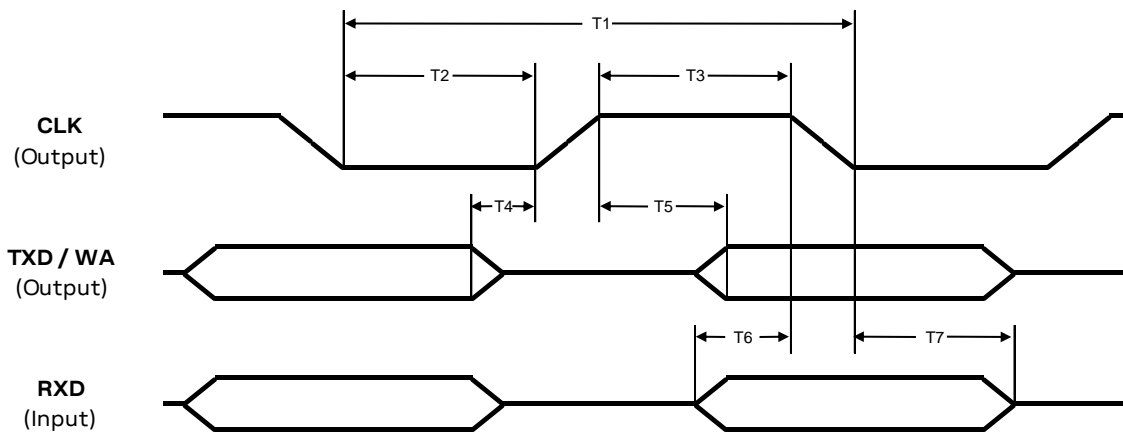
Table 19: Generic Digital Interfaces pin characteristics (GDI domain)

4.2.9.1 AC characteristics of the digital audio interfaces pins

The 4-wire I²S digital audio interfaces can be configured in 4 different modes:

- Normal I²S mode – Master mode
- Normal I²S mode – Slave mode
- PCM mode – Master mode
- PCM mode – Slave mode

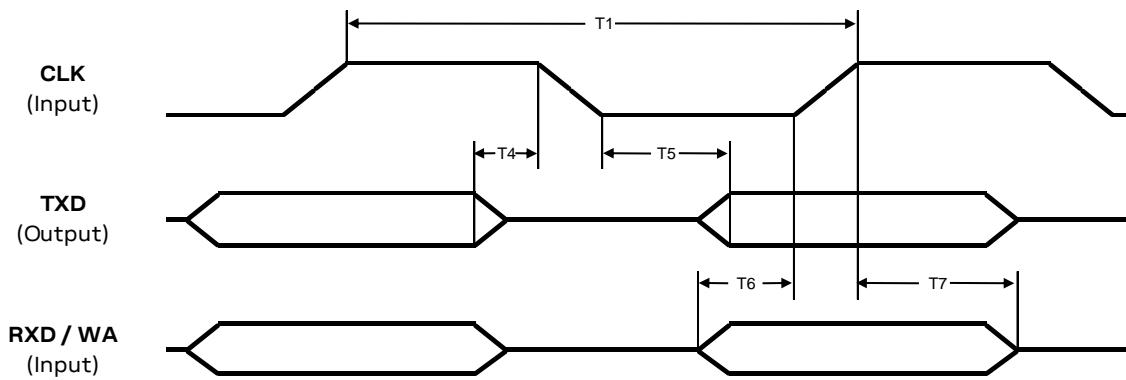
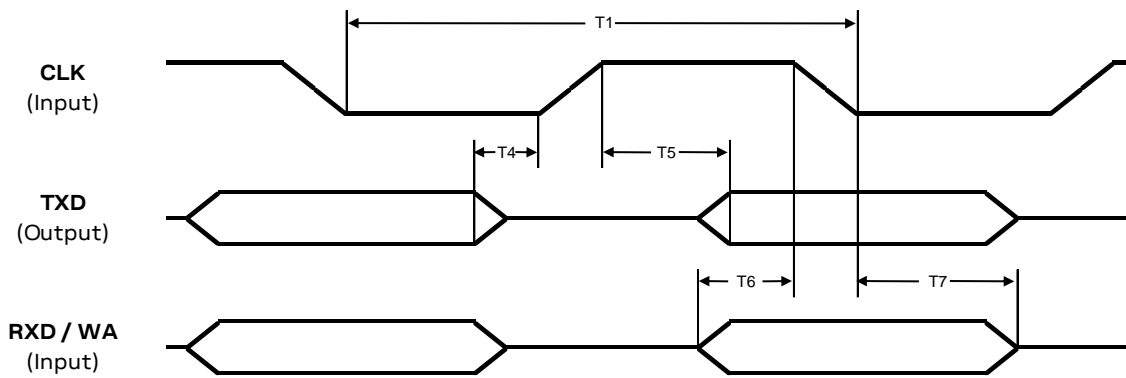
The AC characteristics of the 4 different modes of the I²S digital audio interfaces are detailed below.

Normal I²S mode – Master mode

Figure 3: AC characteristics of digital audio interface in Normal I²S mode (<I2S_mode> = 2,4,6,8,10,12) and Master mode enabled

Figure 4: AC characteristics of digital audio interface in Normal I²S mode (<I2S_mode> = 3,5,7,9,11,13) and Master mode enabled

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks	
T1	I ² S clock period	3.902	3.906		μs	<I2S_sample_rate>=0	
		2.830	2.834		μs	<I2S_sample_rate>=1	
		2.600	2.604		μs	<I2S_sample_rate>=2	
		1.949	1.953		μs	<I2S_sample_rate>=3	
		1.413	1.417		μs	<I2S_sample_rate>=4	
		1.298	1.302		μs	<I2S_sample_rate>=5	
		0.973	0.977		μs	<I2S_sample_rate>=6	
		0.705	0.709		μs	<I2S_sample_rate>=7	
		0.647	0.651		μs	<I2S_sample_rate>=8	
1/T1	I ² S clock frequency		256.0	256.3	kHz	<I2S_sample_rate>=0	
				352.8	353.3	kHz	<I2S_sample_rate>=1
				384.0	384.6	kHz	<I2S_sample_rate>=2
				512.0	513.1	kHz	<I2S_sample_rate>=3
				705.6	707.6	kHz	<I2S_sample_rate>=4
				768.0	770.4	kHz	<I2S_sample_rate>=5
				1024	1028	kHz	<I2S_sample_rate>=6
				1411	1419	kHz	<I2S_sample_rate>=7
				1536	1545	kHz	<I2S_sample_rate>=8

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
T2	I ² S clock high time	1.933	1.953		μs	<I2S_sample_rate>=0
		1.397	1.417		μs	<I2S_sample_rate>=1
		1.282	1.302		μs	<I2S_sample_rate>=2
		0.957	0.977		μs	<I2S_sample_rate>=3
		0.689	0.709		μs	<I2S_sample_rate>=4
		0.631	0.651		μs	<I2S_sample_rate>=5
		0.468	0.488		μs	<I2S_sample_rate>=6
		0.334	0.354		μs	<I2S_sample_rate>=7
		0.306	0.326		μs	<I2S_sample_rate>=8
T3	I ² S clock low time	1.933	1.953		μs	<I2S_sample_rate>=0
		1.397	1.417		μs	<I2S_sample_rate>=1
		1.282	1.302		μs	<I2S_sample_rate>=2
		0.957	0.977		μs	<I2S_sample_rate>=3
		0.689	0.709		μs	<I2S_sample_rate>=4
		0.631	0.651		μs	<I2S_sample_rate>=5
		0.468	0.488		μs	<I2S_sample_rate>=6
		0.334	0.354		μs	<I2S_sample_rate>=7
		0.306	0.326		μs	<I2S_sample_rate>=8
	I ² S word alignment period		125.0		μs	<I2S_sample_rate>=0
			90.70		μs	<I2S_sample_rate>=1
			83.33		μs	<I2S_sample_rate>=2
			62.50		μs	<I2S_sample_rate>=3
			45.35		μs	<I2S_sample_rate>=4
			41.67		μs	<I2S_sample_rate>=5
			31.25		μs	<I2S_sample_rate>=6
			22.68		μs	<I2S_sample_rate>=7
	I ² S word alignment frequency		8.000		kHz	<I2S_sample_rate>=0
			11.03		kHz	<I2S_sample_rate>=1
			12.00		kHz	<I2S_sample_rate>=2
			16.00		kHz	<I2S_sample_rate>=3
			22.05		kHz	<I2S_sample_rate>=4
			24.00		kHz	<I2S_sample_rate>=5
			32.00		kHz	<I2S_sample_rate>=6
			44.10		kHz	<I2S_sample_rate>=7
T4	I ² S TXD invalid before I ² S CLK high end (before shifting edge of I ² S CLK)			24	ns	<I2S_mode> = 2,4,6,8,10,12
	I ² S TXD invalid before I ² S CLK low end (before shifting edge of I ² S CLK)			24	ns	<I2S_mode> = 3,5,7,9,11,13
T5	I ² S TXD valid after I ² S CLK low begin (after shifting edge of I ² S CLK)			32	ns	<I2S_mode> = 2,4,6,8,10,12
	I ² S TXD valid after I ² S CLK high begin (after shifting edge of I ² S CLK)			32	ns	<I2S_mode> = 3,5,7,9,11,13
T6	I ² S RXD setup time before I ² S CLK low end (before latching edge of I ² S CLK)	60			ns	<I2S_mode> = 2,4,6,8,10,12
	I ² S RXD setup time before I ² S CLK high end (before latching edge of I ² S CLK)	60			ns	<I2S_mode> = 3,5,7,9,11,13
T7	I ² S RXD hold time after I ² S CLK high begin (after latching edge of I ² S CLK)	10			ns	<I2S_mode> = 2,4,6,8,10,12
	I ² S RXD hold time after I ² S CLK low begin (after latching edge of I ² S CLK)	10			ns	<I2S_mode> = 3,5,7,9,11,13

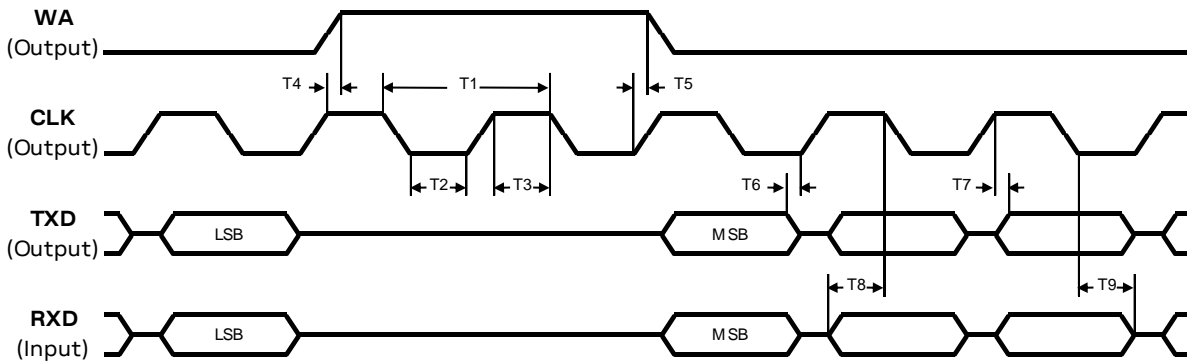
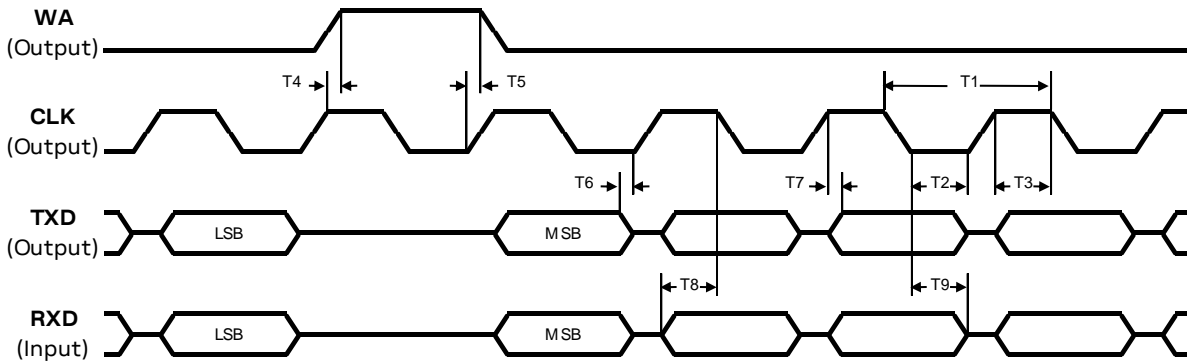
Table 20: AC characteristics of digital audio interface in Normal I²S mode and Master mode enabled

Normal I²S mode – Slave mode

Figure 5: AC characteristics of digital audio interface in Normal I²S mode (<I2S_mode> = 2,4,6,8,10,12) and Slave mode enabled

Figure 6: AC characteristics of digital audio interface in Normal I²S mode (<I2S_mode> = 3,5,7,9,11,13) and Slave mode enabled

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
T1	I ² S clock period	3.906			μs	<I2S_sample_rate>=0
		2.834			μs	<I2S_sample_rate>=1
		2.604			μs	<I2S_sample_rate>=2
		1.953			μs	<I2S_sample_rate>=3
		1.417			μs	<I2S_sample_rate>=4
		1.302			μs	<I2S_sample_rate>=5
		0.977			μs	<I2S_sample_rate>=6
		0.709			μs	<I2S_sample_rate>=7
		0.651			μs	<I2S_sample_rate>=8
1/T1	I ² S clock frequency			256.0	kHz	<I2S_sample_rate>=0
				352.8	kHz	<I2S_sample_rate>=1
				384.0	kHz	<I2S_sample_rate>=2
				512.0	kHz	<I2S_sample_rate>=3
				705.6	kHz	<I2S_sample_rate>=4
				768.0	kHz	<I2S_sample_rate>=5
				1024	kHz	<I2S_sample_rate>=6
				1411	kHz	<I2S_sample_rate>=7
				1536	kHz	<I2S_sample_rate>=8
	I ² S word alignment period	125.0			μs	<I2S_sample_rate>=0
		90.70			μs	<I2S_sample_rate>=1

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
		83.33			μs	<I2S_sample_rate>=2
		62.50			μs	<I2S_sample_rate>=3
		45.35			μs	<I2S_sample_rate>=4
		41.67			μs	<I2S_sample_rate>=5
		31.25			μs	<I2S_sample_rate>=6
		22.68			μs	<I2S_sample_rate>=7
		20.83			μs	<I2S_sample_rate>=8
	I ² S word alignment frequency			8.000	kHz	<I2S_sample_rate>=0
				11.03	kHz	<I2S_sample_rate>=1
				12.00	kHz	<I2S_sample_rate>=2
				16.00	kHz	<I2S_sample_rate>=3
				22.05	kHz	<I2S_sample_rate>=4
				24.00	kHz	<I2S_sample_rate>=5
				32.00	kHz	<I2S_sample_rate>=6
				44.10	kHz	<I2S_sample_rate>=7
				48.00	kHz	<I2S_sample_rate>=8
T4	I ² S TXD invalid before I ² S CLK falling edge (before shifting edge of I ² S CLK)			24	ns	<I2S_mode> = 2,4,6,8,10,12
	I ² S TXD invalid before I ² S CLK rising edge (before shifting edge of I ² S CLK)			24	ns	<I2S_mode> = 3,5,7,9,11,13
T5	I ² S TXD valid after I ² S CLK falling edge (after shifting edge of I ² S CLK)			32	ns	<I2S_mode> = 2,4,6,8,10,12
	I ² S TXD valid after I ² S CLK rising edge (after shifting edge of I ² S CLK)			32	ns	<I2S_mode> = 3,5,7,9,11,13
T6	I ² S RXD setup time before I ² S CLK rising edge (before latching edge of I ² S CLK)	60			ns	<I2S_mode> = 2,4,6,8,10,12
	I ² S RXD setup time before I ² S CLK falling edge (before latching edge of I ² S CLK)	60			ns	<I2S_mode> = 3,5,7,9,11,13
T7	I ² S RXD hold time after I ² S CLK rising edge (after latching edge of I ² S CLK)	10			ns	<I2S_mode> = 2,4,6,8,10,12
	I ² S RXD hold time after I ² S CLK falling edge (after latching edge of I ² S CLK)	10			ns	<I2S_mode> = 3,5,7,9,11,13

Table 21: AC characteristics of digital audio interface in Normal I²S mode and Slave mode enabled

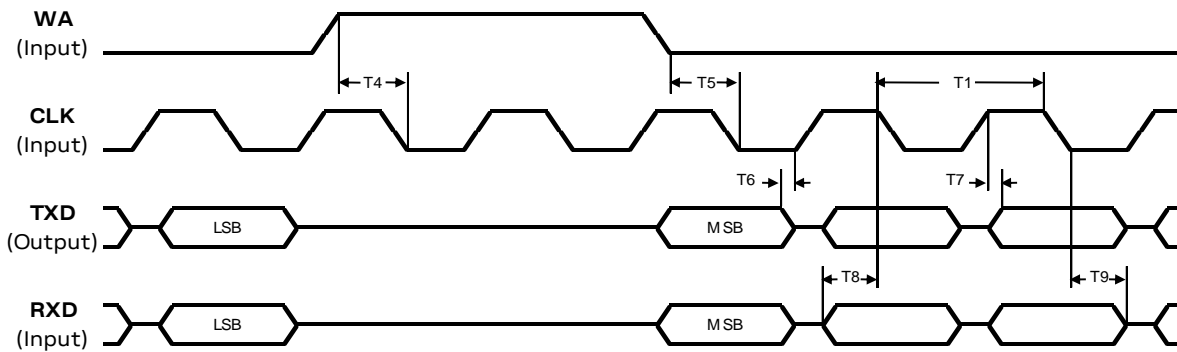
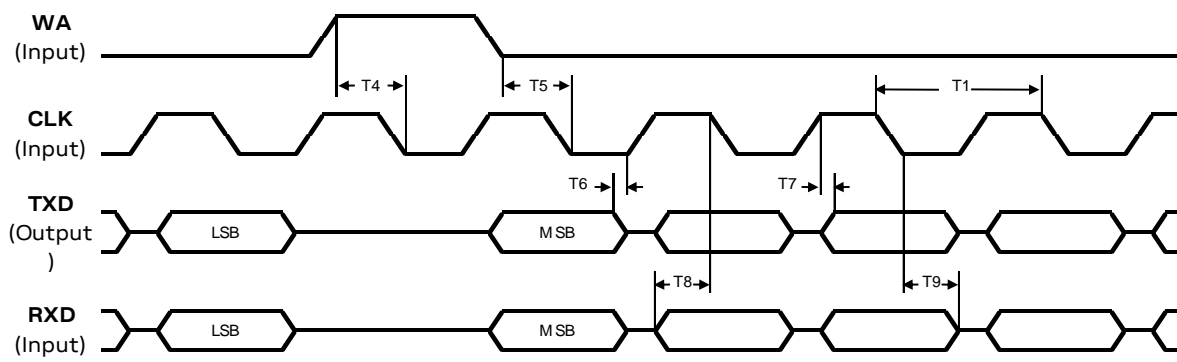
PCM mode – Master mode

Figure 7: AC characteristics of digital audio interface in PCM mode (<I2S_mode> = 0) and Master mode enabled

Figure 8: AC characteristics of digital audio interface in PCM mode (<I2S_mode> = 1) and Master mode enabled

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
T1	I ² S clock period	6.940	6.944		μs	<I2S_mode>=0, <I2S_sample_rate>=0
		7.349	7.353		μs	<I2S_mode>=1, <I2S_sample_rate>=0
		5.035	5.039		μs	<I2S_mode>=0, <I2S_sample_rate>=1
		5.331	5.335		μs	<I2S_mode>=1, <I2S_sample_rate>=1
		4.626	4.630		μs	<I2S_mode>=0, <I2S_sample_rate>=2
		4.898	4.902		μs	<I2S_mode>=1, <I2S_sample_rate>=2
		3.468	3.472		μs	<I2S_mode>=0, <I2S_sample_rate>=3
		3.672	3.676		μs	<I2S_mode>=1, <I2S_sample_rate>=3
		2.516	2.520		μs	<I2S_mode>=0, <I2S_sample_rate>=4
		2.664	2.668		μs	<I2S_mode>=1, <I2S_sample_rate>=4
		2.311	2.315		μs	<I2S_mode>=0, <I2S_sample_rate>=5
		2.447	2.451		μs	<I2S_mode>=1, <I2S_sample_rate>=5
		1.732	1.736		μs	<I2S_mode>=0, <I2S_sample_rate>=6
		1.834	1.838		μs	<I2S_mode>=1, <I2S_sample_rate>=6
		1.256	1.260		μs	<I2S_mode>=0, <I2S_sample_rate>=7
		1.330	1.334		μs	<I2S_mode>=1, <I2S_sample_rate>=7
1.153	1.157		μs	<I2S_mode>=0, <I2S_sample_rate>=8		
1.221	1.225		μs	<I2S_mode>=1, <I2S_sample_rate>=8		
1/T1	I ² S clock frequency		144.0	144.1	kHz	<I2S_mode>=0, <I2S_sample_rate>=0
			136.0	136.1	kHz	<I2S_mode>=1, <I2S_sample_rate>=0
			198.5	198.6	kHz	<I2S_mode>=0, <I2S_sample_rate>=1
			187.4	187.6	kHz	<I2S_mode>=1, <I2S_sample_rate>=1

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
			216.0	216.2	kHz	<I2S_mode>=0, <I2S_sample_rate>=2
			204.0	204.2	kHz	<I2S_mode>=1, <I2S_sample_rate>=2
			288.0	288.3	kHz	<I2S_mode>=0, <I2S_sample_rate>=3
			272.0	272.3	kHz	<I2S_mode>=1, <I2S_sample_rate>=3
			396.9	397.5	kHz	<I2S_mode>=0, <I2S_sample_rate>=4
			374.9	375.4	kHz	<I2S_mode>=1, <I2S_sample_rate>=4
			432.0	432.7	kHz	<I2S_mode>=0, <I2S_sample_rate>=5
			408.0	408.7	kHz	<I2S_mode>=1, <I2S_sample_rate>=5
			576.0	577.3	kHz	<I2S_mode>=0, <I2S_sample_rate>=6
			544.0	545.2	kHz	<I2S_mode>=1, <I2S_sample_rate>=6
			793.8	796.3	kHz	<I2S_mode>=0, <I2S_sample_rate>=7
			749.7	752.0	kHz	<I2S_mode>=1, <I2S_sample_rate>=7
			864.0	867.0	kHz	<I2S_mode>=0, <I2S_sample_rate>=8
			816.0	818.7	kHz	<I2S_mode>=1, <I2S_sample_rate>=8
T2	I ² S clock low time	3.452	3.472		μs	<I2S_mode>=0, <I2S_sample_rate>=0
		3.656	3.676		μs	<I2S_mode>=1, <I2S_sample_rate>=0
		2.500	2.520		μs	<I2S_mode>=0, <I2S_sample_rate>=1
		2.648	2.668		μs	<I2S_mode>=1, <I2S_sample_rate>=1
		2.295	2.315		μs	<I2S_mode>=0, <I2S_sample_rate>=2
		2.431	2.451		μs	<I2S_mode>=1, <I2S_sample_rate>=2
		1.716	1.736		μs	<I2S_mode>=0, <I2S_sample_rate>=3
		1.818	1.838		μs	<I2S_mode>=1, <I2S_sample_rate>=3
		1.240	1.260		μs	<I2S_mode>=0, <I2S_sample_rate>=4
		1.314	1.334		μs	<I2S_mode>=1, <I2S_sample_rate>=4
		1.137	1.157		μs	<I2S_mode>=0, <I2S_sample_rate>=5
		1.205	1.225		μs	<I2S_mode>=1, <I2S_sample_rate>=5
		0.848	0.868		μs	<I2S_mode>=0, <I2S_sample_rate>=6
		0.899	0.919		μs	<I2S_mode>=1, <I2S_sample_rate>=6
		0.610	0.630		μs	<I2S_mode>=0, <I2S_sample_rate>=7
		0.647	0.667		μs	<I2S_mode>=1, <I2S_sample_rate>=7
		0.559	0.579		μs	<I2S_mode>=0, <I2S_sample_rate>=8
		0.593	0.613		μs	<I2S_mode>=1, <I2S_sample_rate>=8
T3	I ² S clock high time	3.452	3.472		μs	<I2S_mode>=0, <I2S_sample_rate>=0
		3.656	3.676		μs	<I2S_mode>=1, <I2S_sample_rate>=0
		2.500	2.520		μs	<I2S_mode>=0, <I2S_sample_rate>=1
		2.648	2.668		μs	<I2S_mode>=1, <I2S_sample_rate>=1
		2.295	2.315		μs	<I2S_mode>=0, <I2S_sample_rate>=2
		2.431	2.451		μs	<I2S_mode>=1, <I2S_sample_rate>=2
		1.716	1.736		μs	<I2S_mode>=0, <I2S_sample_rate>=3
		1.818	1.838		μs	<I2S_mode>=1, <I2S_sample_rate>=3
		1.240	1.260		μs	<I2S_mode>=0, <I2S_sample_rate>=4
		1.314	1.334		μs	<I2S_mode>=1, <I2S_sample_rate>=4
		1.137	1.157		μs	<I2S_mode>=0, <I2S_sample_rate>=5
		1.205	1.225		μs	<I2S_mode>=1, <I2S_sample_rate>=5
		0.848	0.868		μs	<I2S_mode>=0, <I2S_sample_rate>=6
		0.899	0.919		μs	<I2S_mode>=1, <I2S_sample_rate>=6
		0.610	0.630		μs	<I2S_mode>=0, <I2S_sample_rate>=7
		0.647	0.667		μs	<I2S_mode>=1, <I2S_sample_rate>=7
		0.559	0.579		μs	<I2S_mode>=0, <I2S_sample_rate>=8
		0.593	0.613		μs	<I2S_mode>=1, <I2S_sample_rate>=8
	I ² S word alignment period		125.0		μs	<I2S_sample_rate>=0
			90.70		μs	<I2S_sample_rate>=1
			83.33		μs	<I2S_sample_rate>=2
			62.50		μs	<I2S_sample_rate>=3

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
			45.35		μs	<I2S_sample_rate>=4
			41.67		μs	<I2S_sample_rate>=5
			31.25		μs	<I2S_sample_rate>=6
			22.68		μs	<I2S_sample_rate>=7
			20.83		μs	<I2S_sample_rate>=8
	I ² S word alignment frequency		8.000		kHz	<I2S_sample_rate>=0
			11.03		kHz	<I2S_sample_rate>=1
			12.00		kHz	<I2S_sample_rate>=2
			16.00		kHz	<I2S_sample_rate>=3
			22.05		kHz	<I2S_sample_rate>=4
			24.00		kHz	<I2S_sample_rate>=5
			32.00		kHz	<I2S_sample_rate>=6
			44.10		kHz	<I2S_sample_rate>=7
			48.00		kHz	<I2S_sample_rate>=8
T4	I ² S CLK high begin to I ² S WA high begin	-24		32	ns	<I2S_mode> = 0
T5	I ² S CLK low end to I ² S WA high end	-24		32	ns	<I2S_mode> = 0
T6	I ² S TXD invalid before I ² S CLK low end			24	ns	<I2S_mode> = 0
T7	I ² S TXD valid after I ² S CLK high begin			22	ns	<I2S_mode> = 0
T8	I ² S RXD setup time before I ² S CLK high end	60			ns	<I2S_mode> = 0
T9	I ² S RXD hold time after I ² S CLK low begin	12			ns	<I2S_mode> = 0

Table 22: AC characteristics of digital audio interface in PCM mode (<I2S_mode> = 0,1) and Master mode enabled

PCM mode – Slave mode

Figure 9: AC characteristics of digital audio interface in PCM mode (<I2S_mode> = 0) and Slave mode enabled

Figure 10: AC characteristics of digital audio interface in PCM mode (<I2S_mode> = 1) and Slave mode enabled

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
T1	I ² S clock period	6.944			μ s	<I2S_mode>=0, <I2S_sample_rate>=0
		7.353			μ s	<I2S_mode>=1, <I2S_sample_rate>=0
		5.039			μ s	<I2S_mode>=0, <I2S_sample_rate>=1
		5.335			μ s	<I2S_mode>=1, <I2S_sample_rate>=1
		4.630			μ s	<I2S_mode>=0, <I2S_sample_rate>=2
		4.902			μ s	<I2S_mode>=1, <I2S_sample_rate>=2
		3.472			μ s	<I2S_mode>=0, <I2S_sample_rate>=3
		3.676			μ s	<I2S_mode>=1, <I2S_sample_rate>=3
		2.520			μ s	<I2S_mode>=0, <I2S_sample_rate>=4
		2.668			μ s	<I2S_mode>=1, <I2S_sample_rate>=4
		2.315			μ s	<I2S_mode>=0, <I2S_sample_rate>=5
		2.451			μ s	<I2S_mode>=1, <I2S_sample_rate>=5
		1.736			μ s	<I2S_mode>=0, <I2S_sample_rate>=6
		1.838			μ s	<I2S_mode>=1, <I2S_sample_rate>=6
		1.260			μ s	<I2S_mode>=0, <I2S_sample_rate>=7
		1.334			μ s	<I2S_mode>=1, <I2S_sample_rate>=7
1.157			μ s	<I2S_mode>=0, <I2S_sample_rate>=8		
1.225			μ s	<I2S_mode>=1, <I2S_sample_rate>=8		

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
1/T1	I ² S clock frequency	144.0			kHz	<I2S_mode>=0, <I2S_sample_rate>=0
		136.0			kHz	<I2S_mode>=1, <I2S_sample_rate>=0
		198.5			kHz	<I2S_mode>=0, <I2S_sample_rate>=1
		187.4			kHz	<I2S_mode>=1, <I2S_sample_rate>=1
		216.0			kHz	<I2S_mode>=0, <I2S_sample_rate>=2
		204.0			kHz	<I2S_mode>=1, <I2S_sample_rate>=2
		288.0			kHz	<I2S_mode>=0, <I2S_sample_rate>=3
		272.0			kHz	<I2S_mode>=1, <I2S_sample_rate>=3
		396.9			kHz	<I2S_mode>=0, <I2S_sample_rate>=4
		374.9			kHz	<I2S_mode>=1, <I2S_sample_rate>=4
		432.0			kHz	<I2S_mode>=0, <I2S_sample_rate>=5
		408.0			kHz	<I2S_mode>=1, <I2S_sample_rate>=5
		576.0			kHz	<I2S_mode>=0, <I2S_sample_rate>=6
		544.0			kHz	<I2S_mode>=1, <I2S_sample_rate>=6
		793.8			kHz	<I2S_mode>=0, <I2S_sample_rate>=7
		749.7			kHz	<I2S_mode>=1, <I2S_sample_rate>=7
		864.0			kHz	<I2S_mode>=0, <I2S_sample_rate>=8
		816.0			kHz	<I2S_mode>=1, <I2S_sample_rate>=8
	I ² S word alignment period	125.0			μs	<I2S_sample_rate>=0
		90.70			μs	<I2S_sample_rate>=1
		83.33			μs	<I2S_sample_rate>=2
		62.50			μs	<I2S_sample_rate>=3
		45.35			μs	<I2S_sample_rate>=4
		41.67			μs	<I2S_sample_rate>=5
		31.25			μs	<I2S_sample_rate>=6
		22.68			μs	<I2S_sample_rate>=7
20.83			μs	<I2S_sample_rate>=8		
	I ² S word alignment frequency	8.000			kHz	<I2S_sample_rate>=0
		11.03			kHz	<I2S_sample_rate>=1
		12.00			kHz	<I2S_sample_rate>=2
		16.00			kHz	<I2S_sample_rate>=3
		22.05			kHz	<I2S_sample_rate>=4
		24.00			kHz	<I2S_sample_rate>=5
		32.00			kHz	<I2S_sample_rate>=6
		44.10			kHz	<I2S_sample_rate>=7
48.00			kHz	<I2S_sample_rate>=8		
T4	WA high begin before CLK low begin (latching edge of CLK)	36			ns	<I2S_mode> = 0
T5	WA low begin before CLK low begin (latching edge of CLK)	36			ns	<I2S_mode> = 0
T6	TXD invalid before CLK rising edge (shifting edge of CLK)			12	ns	<I2S_mode> = 0
T7	TXD valid after CLK rising edge (shifting edge of CLK)			79	ns	<I2S_mode> = 0
T8	RXD setup time before CLK fall edge (latching edge of CLK)	22			ns	<I2S_mode> = 0
T9	RXD hold time after CLK falling edge (latching edge of CLK)	24			ns	<I2S_mode> = 0

Table 23: AC characteristics of digital audio interface in PCM mode (<I2S_mode> = 0,1) and Slave mode enabled

4.2.9.2 AC characteristics of the Digital Clock Output pin

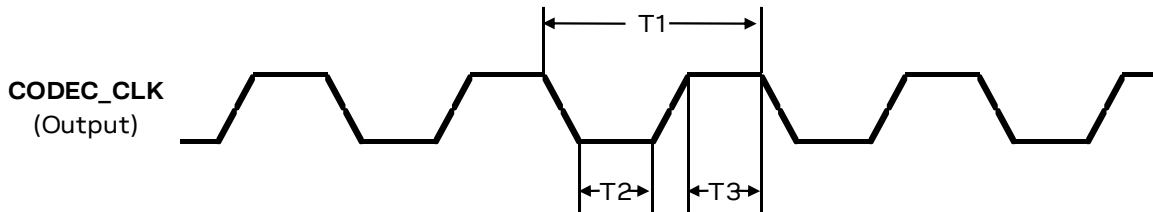


Figure 11: AC characteristics of CODEC_CLK digital clock output

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
T1	CODEC_CLK clock period		38		ns	CODEC_CLK output set to 26 MHz
			77		ns	CODEC_CLK output set to 13 MHz
1/T1	CODEC_CLK clock frequency		26		MHz	CODEC_CLK output set to 26 MHz
			13		MHz	CODEC_CLK output set to 13 MHz
T2	CODEC_CLK clock low time	10			ns	CODEC_CLK output set to 26 MHz
		26			ns	CODEC_CLK output set to 13 MHz
T3	CODEC_CLK clock high time	10			ns	CODEC_CLK output set to 26 MHz
		26			ns	CODEC_CLK output set to 13 MHz

Table 24: AC characteristics of CODEC_CLK digital clock output

4.2.9.3 AC characteristics of the SPI / IPC pins

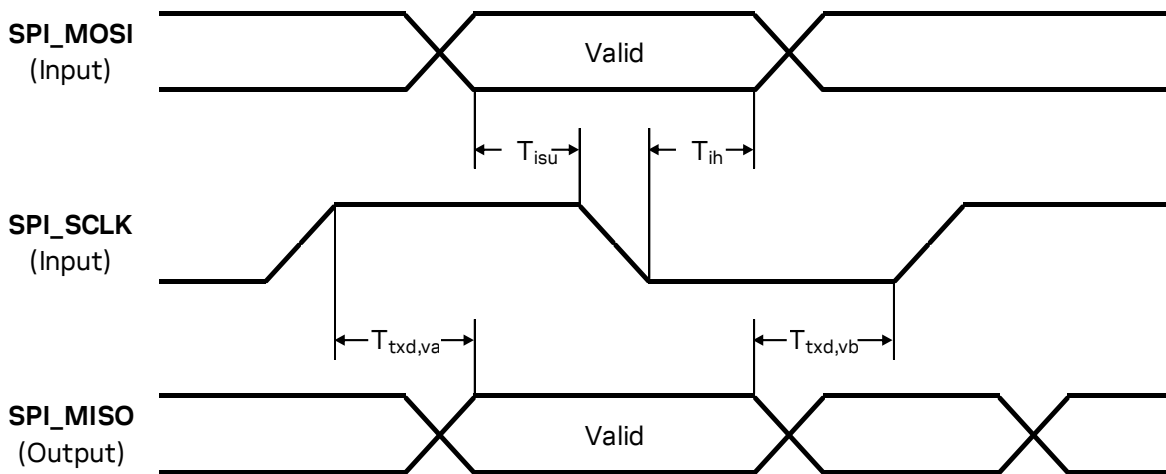


Figure 12: SPI_MOSI, SPI_MISO, SPI_SCLK timings

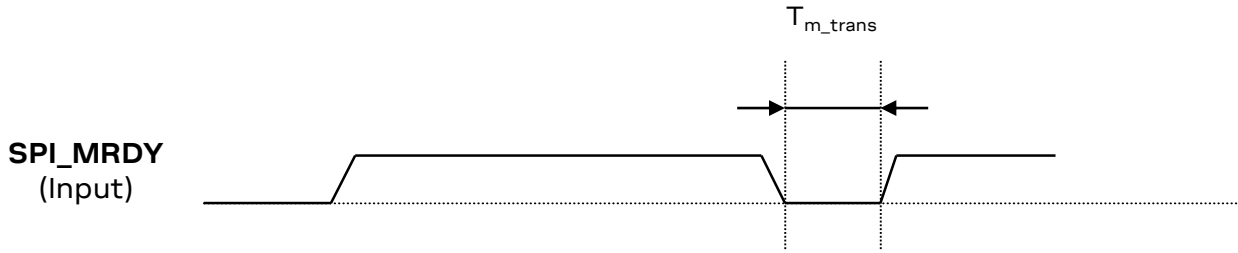


Figure 13: SPI_MRDIY transition

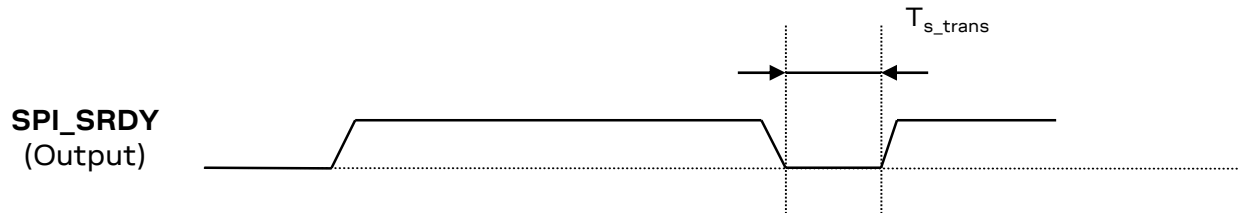


Figure 14: SPI_SRDIY transition

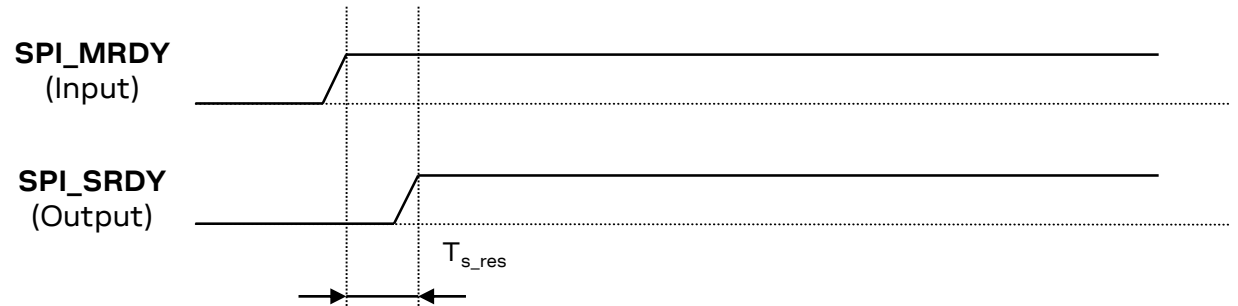


Figure 15: SPI_SRDIY response

Parameter	Description	Min.	Typ.	Max.	Unit	Remarks
	SPI_SCLK frequency	0.26		26.0	MHz	
	SPI_SCLK period	38.5		3846.2	ns	
T_{isu}	Receive data setup time	5			ns	
T_{ih}	Receive data hold time	5			ns	
$T_{txd,va}$	Transmit data valid after clock rising edge			13	ns	
$T_{txd,vb}$	Transmit data valid before clock rising edge			0	ns	
T_{m_trans}	Time between two master data transfers	80			ns	Power saving disabled by AT+UPSV
		62			μ s	Power saving enabled by AT+UPSV
T_{s_trans}	Time between two slave data transfers	80			ns	
T_{s_res}	SPI_SRDIY active after SPI_MRDIY active			200	μ s	Power saving disabled by AT+UPSV
				10	ms	Power saving enabled by AT+UPSV

Table 25: AC characteristics of SPI interface

4.2.10 USB pins

USB data lines (**USB_D+** and **USB_D-**) are compliant to the USB 2.0 high-speed specification. See the Universal Serial Bus Revision 2.0 specification [12] for the detailed electrical characteristics.

Parameter	Min.	Typ.	Max.	Unit	Remarks
USB detection voltage on pin VUSB_DET	4.40	5.00	5.25	V	
Current sink at VUSB_DET		30		μA	
High-speed squelch detection threshold (input differential signal amplitude)	100		150	mV	
High speed disconnect detection threshold (input differential signal amplitude)	525		625	mV	
High-speed data signaling input common mode voltage range	-50		500	mV	
High-speed idle output level	-10		10	mV	
High-speed data signaling output high level	360		440	mV	
High-speed data signaling output low level	-10		10	mV	
Chirp J level (output differential voltage)	700		1100	mV	
Chirp K level (output differential voltage)	-900		-500	mV	

Table 26: USB pin characteristics

4.2.11 DDC (I²C) pins

DDC (I²C) lines (**SCL** and **SDA**) are compliant to the I²C-bus standard mode specification. See the I²C-Bus Specification [13] for the detailed electrical characteristics.

Parameter	Min.	Typ.	Max.	Unit	Remarks
Internal supply for DDC domain	1.73	1.80	1.87	V	Digital I/O Interfaces supply (V_INT)
L-level input	-0.20		0.35	V	
H-level input	1.31		1.93	V	
L-level output		0.00	0.35	V	Max value at I _{OL} = +1.0 mA
Input/Output leakage current			0.7	μA	0.2 V < V _{IN} < 1.93 V
Clock frequency on SCL		100		kHz	



Table 27: DDC (I²C) pin characteristics (DDC domain)

4.3 Parameters for ATEX applications

This section provides useful parameters and information to integrate LISA-U2 series modules in applications intended for use in areas with potentially explosive atmospheres (ATEX), describing:

Total internal capacitance and inductance of LISA-U2 series modules (see [Table 28](#))

Maximum RF output power and voltage at the antenna pin of LISA-U2 series modules (see [Table 29](#))

-  Any specific applicable requirement for the implementation of the apparatus integrating LISA-U2 series modules, intended for use in potentially explosive atmospheres, must be fulfilled according to the exact applicable standards: check the detailed requisites on the pertinent normative for the application, as for example the IEC 60079-0 [\[20\]](#), IEC 60079-11 [\[21\]](#), IEC 60079-26 [\[22\]](#) standards.
-  The certification of the application device that integrates a LISA-U2 series module and the compliance of the application device with all the applicable certification schemes, directives and standards required for use in potentially explosive atmospheres are the sole responsibility of the application device manufacturer.

[Table 11](#) describes the maximum total internal capacitance and the maximum total internal inductance, considering internal parts tolerance, provided by LISA-U2 series modules.


Module	Parameter	Description	Value	Unit
LISA-U200, LISA-U230, LISA-U260, LISA-U270	Ci	Maximum total internal capacitance	167.4	μF
	Li	Maximum total internal inductance	26.3	μH
LISA-U201	Ci	Maximum total internal capacitance	169.6	μF
	Li	Maximum total internal inductance	9.4	μH

Table 28: LISA-U2 series maximum total internal capacitance and maximum total internal inductance

[Table 29](#) describes the maximum RF output power transmitted by LISA-U2 series modules from the RF antenna pin (**ANT**) as Power Class 4 Mobile Stations for GSM 850 / E-GSM 900 bands, and the corresponding maximum voltage into a 50 Ω system load.

Module	Parameter	Description	Value	Unit
LISA-U2 series	ANT Pout	Maximum RF output power from ANT pin	35.0	dBm
	ANT Vout on 50 Ω	Maximum voltage from ANT pin into a 50 Ω system	12.6	Vrms

Table 29: LISA-U2 series antenna pin (ANT) maximum RF output power and corresponding maximum voltage into a 50 Ω load

-  LISA-U2 series modules do not contain internal blocks that increase the input voltage (e.g. like step-up, duplicators, boosters, etc.) except for the RF antenna pin (**ANT**), for which the maximum RF output power and corresponding maximum voltage into a 50 Ω system are illustrated in [Table 29](#).

5 Mechanical specifications

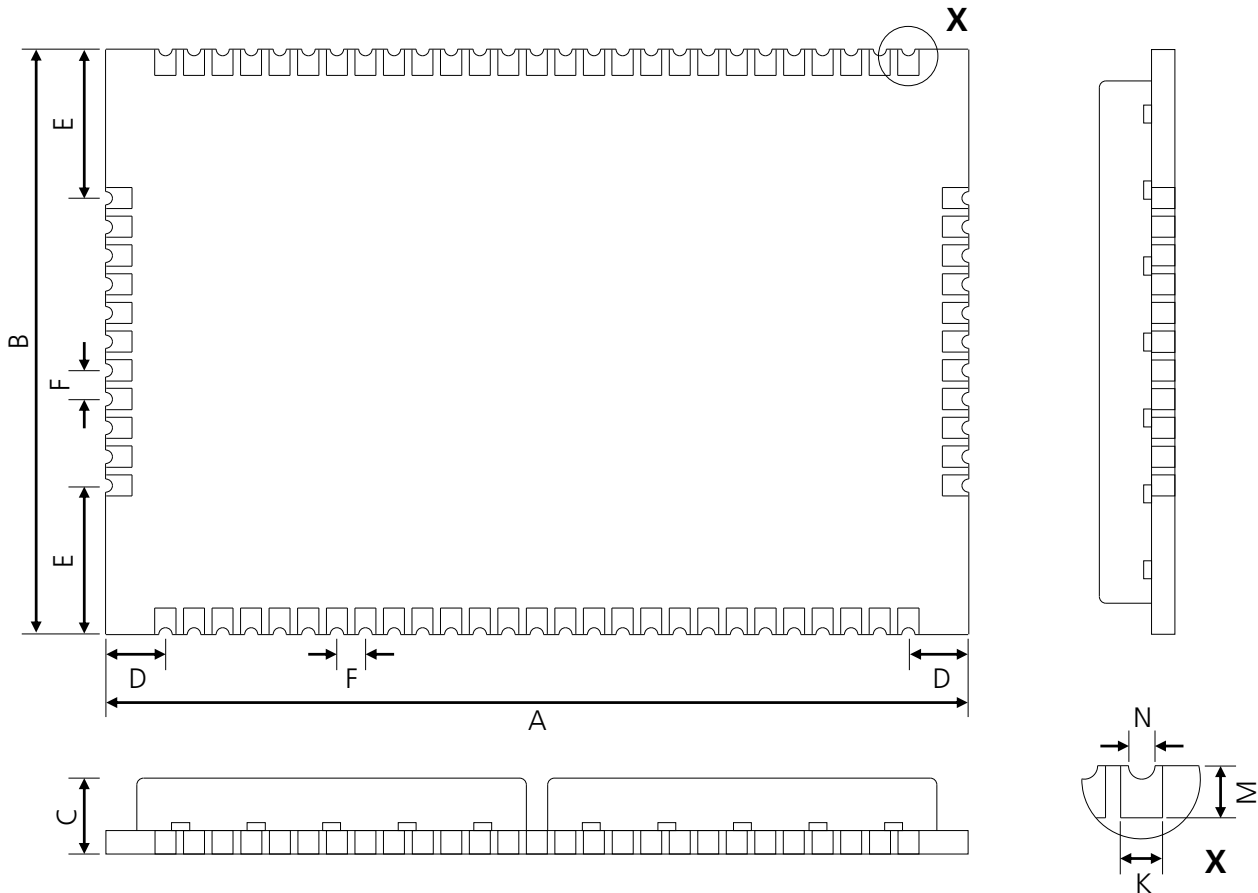


Figure 16: Dimensions (LISA-U2 series bottom and side views)

Parameter	Description	Typical	Tolerance
A	Module Height [mm]	33.2 (1307.1 mil)	+0.20/-0.20 (+7.9/-7.9 mil)
B	Module Width [mm]	22.4 (881.9 mil)	+0.20/-0.20 (+7.9/-7.9 mil)
C	Module Total Thickness [mm]	2.6 (102.4 mil)	+0.27/-0.17 (+10.6/-6.7 mil)
D	Horizontal Edge to Pin Pitch [mm]	2.3 (90.6 mil)	+0.20/-0.20 (+7.9/-7.9 mil)
E	Vertical Edge to Pin Pitch [mm]	5.7 (224.4 mil)	+0.20/-0.20 (+7.9/-7.9 mil)
F	Pin to Pin Pitch [mm]	1.1 (43.3 mil)	+0.02/-0.02 (+0.8/-0.8 mil)
K	Pad width [mm]	0.8 (31.5 mil)	+0.02/-0.02 (+0.8/-0.8 mil)
M	Pad height [mm]	1.0 (39.4 mil)	+0.10/-0.10 (+3.9/-3.9 mil)
N	Pad half-moon diameter [mm]	0.5 (19.7 mil)	+0.10/-0.10 (+3.9/-3.9 mil)
Weight	Module Weight [g]	< 5	

Note: the values in mil have been calculated from the corresponding values in mm.

Table 30: Dimensions

- Module height tolerance ± 0.20 mm may be exceeded close to the corners of the PCB due to the cutting process: in the worst case, the height could be $+0.40$ mm longer than the typical value.
- For information regarding the Footprint and Paste Mask recommended for the application board, see the LISA-U2 series System Integration Manual [6].

6 Reliability tests and approvals

6.1 Reliability tests

Tests for product family qualifications are according to ISO 16750 “Road vehicles - Environmental conditions and testing for electrical and electronic equipment”, and appropriate standards.

6.2 Approvals



Products marked with this lead-free symbol on the product label comply with the Directive 2002/95/EC (RoHS) and the Directive 2011/65/EU (RoHS2) of the European Parliament and the Council on the Restriction of Use of certain Hazardous Substances in Electrical and Electronic Equipment.

LISA-U2 modules are RoHS2 compliant.

No natural rubbers, hygroscopic materials, or materials containing asbestos are employed

Table 31 lists the LISA-U2 series main regulatory and mobile network operators’ approvals.

Directive / Standard / Regulatory	LISA-U200	LISA-U201	LISA-U230	LISA-U260	LISA-U270
CE (European Conformity)	•	•	•	•	•
FCC (US approval)	•	•	•	•	
FCC identification number	XPYLISAU200	XPYLISAU201	XPYLISAU230	XPYLISAU200	
ISED (Canadian approval) ²⁰	•	•	•	•	
IC certification number	8595A-LISAU200N	8595A-LISAU201	8595A-LISAU230N	8595A-LISAU200N	
RCM (Australian compliance)	•	•	•		
Giteki (Japanese approval)	•				•
NCC (Taiwanese approval)	•				•
KCC (Korean Certification)	•				•
ANATEL (Brazilian approval)	•	•			
ICASA (South African approval)	•				•
CCC (Chinese Certification)	•	•	•		•
NTC (Thailand approval)	•	•			
AT&T (Network Operator)	•	•	•	•	
NTT DoCoMo (Network Operator)	•				
SoftBank (Network Operator)					•
SKT (Network Operator)	•				
Telstra (Network Operator)	•				
Telecom NZ (Network Operator)	•				
Vodafone (Network Operator)	•		•		•
Vivo (Network Operator)	•				
Orange (Network Operator)	•				•
Bell Mobility (Network Operator)	•				
Rogers (Network Operator)	•		•	•	

Table 31: LISA-U2 series main regulatory and mobile network operators’ approvals

For all the certificates of compliancy and for the complete list of approvals (including countries’, conformance’ and network operators’ approvals) of LISA-U2 series modules, see our website (www.u-blox.com) or contact the u-blox office or sales representative nearest you.

²⁰ Formerly known as IC (Industry Canada)

7 Product handling & soldering

7.1 Packaging

LISA-U2 modules are delivered as hermetically sealed, reeled tapes to enable efficient production, production lot set-up and tear-down. For more information about packaging, see the u-blox Package Information Guide [\[17\]](#).




Figure 17: Reeled LISA-U2 modules

7.1.1 Reels

LISA-U2 modules are deliverable in quantities of 150 pieces on a reel. LISA-U2 modules are delivered using reel type B as described in the u-blox Package Information Guide [\[17\]](#).

Parameter	Specification
Reel type	B
Delivery quantity	150

Table 32: Reel information for LISA-U2 modules

 Quantities of less than 150 pieces are also available. Contact u-blox for more information.

7.1.2 Tapes

Figure 18 shows the position and orientation of LISA-U2 modules as they are delivered on tape. The dimensions of the tapes are specified in Figure 19.

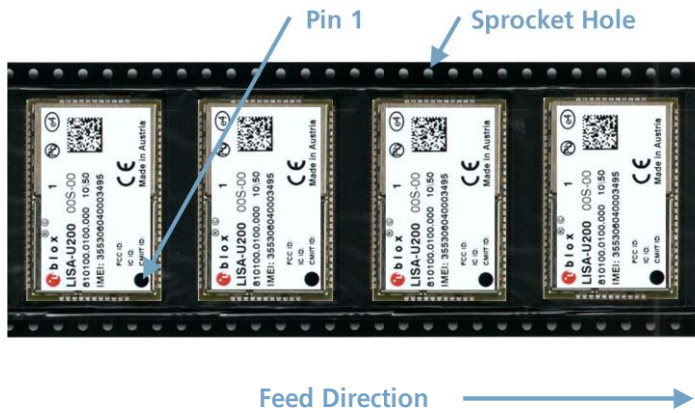


Figure 18: Orientation for the LISA-U2 modules on tape

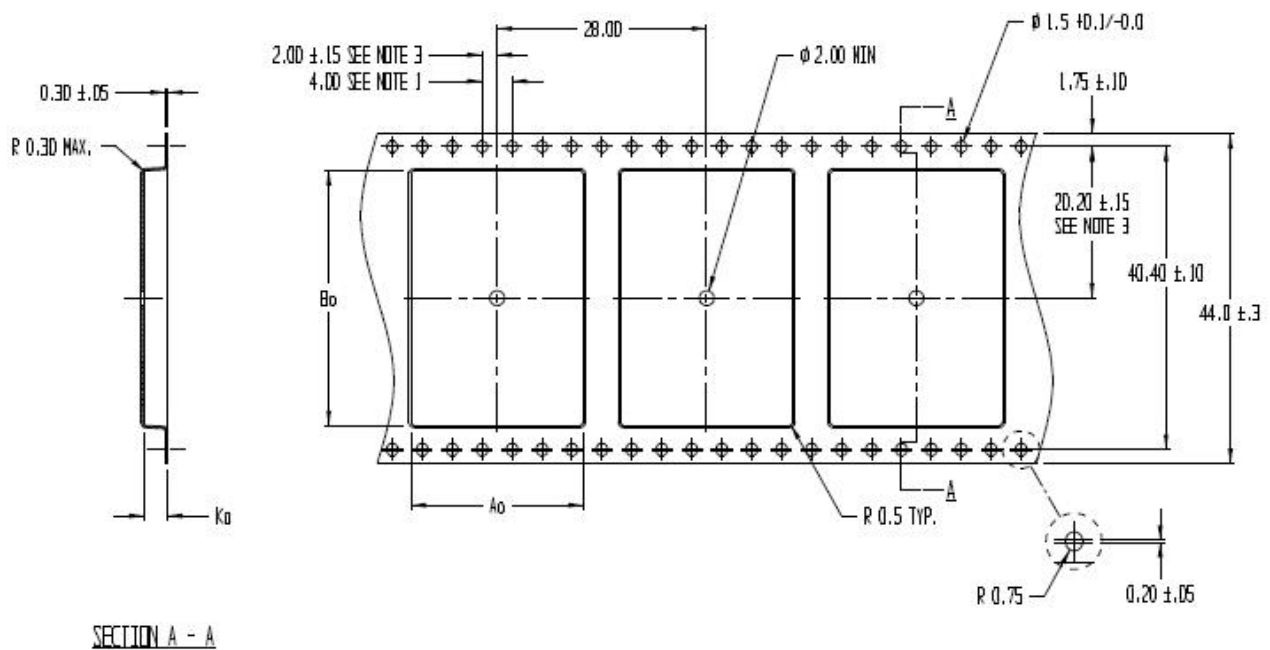


Figure 19: LISA-U2 series tape dimensions (mm)

Parameter	Value
A_0	23.0
B_0	34.0
K_0	3.2

Table 33: LISA-U2 series tape dimensions (mm)

- Note 1: 10 sprocket hole pitch cumulative tolerance ± 0.2 .
- Note 2: the camber is compliant with EIA 481.
- Note 3: the pocket position relative to sprocket hole is measured as true position of pocket, not pocket hole.
- Note 4: A_0 and B_0 are calculated on a plane at a distance "R" above the bottom of the pocket.

7.2 Moisture Sensitivity Levels


-  LISA-U2 modules are Moisture Sensitive Devices (MSD) in accordance to the IPC/JEDEC specification.

The Moisture Sensitivity Level (MSL) relates to the packaging and handling precautions required. LISA-U2 modules are rated at MSL level 4. For more information regarding moisture sensitivity levels, labeling, storage and drying, see the u-blox Package Information Guide [17].


-  For the MSL standard, see IPC/JEDEC J-STD-020 (can be downloaded from www.jedec.org).

7.3 Reflow soldering

Reflow profiles are to be selected according to u-blox recommendations (see the LISA-U2 series System Integration Manual [6]).

-  Failure to observe these recommendations can result in severe damage to the device!

7.4 ESD precautions

-  LISA-U2 modules contain highly sensitive electronic circuitry and are Electrostatic Sensitive Devices (ESD). Handling LISA-U2 modules without adequate ESD protection may destroy or damage them permanently.

LISA-U2 modules are Electrostatic Sensitive Devices (ESD) and require special ESD precautions typically applied to ESD sensitive components.

Table 8 details the maximum ESD ratings of the LISA-U2 module.

Adequate ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the LISA-U2 module.

ESD precautions should be implemented on the application board where the module is mounted, as described in the LISA-U2 series System Integration Manual [6].

-  Failure to observe these precautions can result in severe damage to the device!

8 Default settings


Interface	AT Settings	Comments
UART interface	Enabled	Multiplexing mode can be enabled by AT+CMUX command providing following channels: <ul style="list-style-type: none"> • Channel 0: control channel • Channel 1 – 5: AT commands / data connection • Channel 6: GNSS tunneling • Channel 7: SAP (SIM Access Profile)
	AT+IPR=0	Autobauding enabled
	AT+ICF=3,1	Frame format: 8 bits, no parity, 1 stop bit
		 Where AT+IPR=0 is the default value, the +ICF value in the profile is not applied (+IPR=0 overrules the +ICF setting) and the automatic frame detection is active.
	AT&K3	HW flow control enabled
	AT&S1	DSR line set ON in data mode and set OFF in command mode
	AT&D1	Upon an ON-to-OFF transition of DTR, the DCE enters online command state and issues an OK result code
	AT&C1	Circuit 109 changes in accordance with the Carrier detect status; ON if the Carrier is detected, OFF otherwise
USB interface	Enabled	7 CDCs are available, configured as described in the following list: <ul style="list-style-type: none"> • USB1: AT commands / data connection • USB2: AT commands / data connection • USB3: AT commands / data connection • USB4: GNSS tunneling • USB5: Primary Log (debug purpose) • USB6: Secondary Log (debug purpose) • USB7: SAP (SIM Access Profile)
	AT&K3	HW flow control enabled
	AT&S1	DSR line set ON in data mode and set OFF in command mode
	AT&D1	Upon an ON-to-OFF transition of DTR, the DCE enters online command state and issues an OK result code
	AT&C1	Circuit 109 changes in accordance with the Carrier detect status; ON if the Carrier is detected, OFF otherwise
SPI interface	Enabled	Multiplexing mode can be enabled by AT+CMUX command providing following channels: <ul style="list-style-type: none"> • Channel 0: control channel • Channel 1 – 5: AT commands / data connection • Channel 6: GNSS tunneling • Channel 7: SAP (SIM Access Profile)
	AT&K3	HW flow control enabled
	AT&S1	DSR line set ON in data mode and set OFF in command mode
	AT&D1	Upon an ON-to-OFF transition of DTR, the DCE enters online command state and issues an OK result code
	AT&C1	Circuit 109 changes in accordance with the Carrier detect status; ON if the Carrier is detected, OFF otherwise
Power Saving	AT+UPSV=0	Disabled
Network registration	AT+COPS=0	Self network registration

Table 34: Default settings

See the u-blox AT Commands Manual [\[4\]](#) and the LISA-U2 series System Integration Manual [\[6\]](#) for information about further settings.

9 Labeling and ordering information

9.1 Product labeling

The labels of LISA-U2 series modules include important product information as described in this section. Figure 20 illustrates a label of the LISA-U2 series modules, and includes: u-blox logo, production lot, Pb-free marking, product type number, IMEI number, applicable certification numbers and markings, and production country.

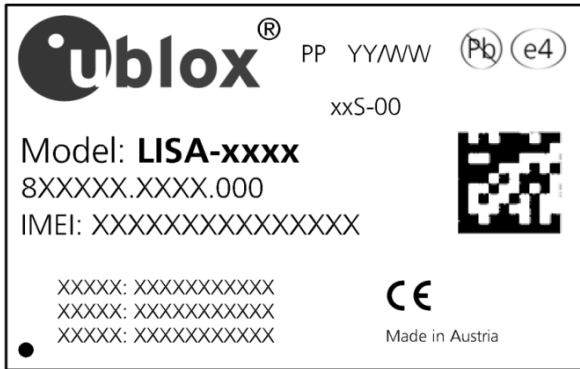


Figure 20: LISA-U2 module label

For information about the approval codes and for all the certificates of compliancy of LISA-U2 series modules, see our website www.u-blox.com.

9.2 Explanation of codes

Three different product code formats are used. The **Product Name** is used in documentation such as this data sheet and identifies all u-blox products, independent of packaging and quality grade. The **Ordering Code** includes options and quality, while the **Type Number** includes the hardware and firmware versions. Table 35 details these 3 different formats:

Format	Structure
Product Name	LISA-TGVV
Ordering Code	LISA-TGVV-TTQ
Type Number	LISA-TGVV-TTQ-XX

Table 35: Product code formats

Table 36 explains the parts of the product code.

Code	Meaning	Example
PPP(P)	Form factor (3 or 4 digit, typically 4 for cellular products)	LISA
TG	Platform (Technology and Generation) <ul style="list-style-type: none"> • Dominant technology: G:GSM; U: HSUPA; C:CDMA 1xRTT; N: NB-IoT; R: LTE low data rate (Cat 1 and below); L: LTE high data rate (Cat.3 and above) • Generation: 1...9 	U2
VV	Variant function set based on the same platform [00...99]	00
TT	Major product version [00...99]	00
Q	Quality grade/production site <ul style="list-style-type: none"> • S = professional • A = automotive 	S
XX	Minor product version (not relevant for certification)	Default value is 00

Table 36: Part identification code

9.3 Ordering information

Ordering No.	Product
LISA-U200-01S	HSPA 800/850/900/1700/1900/2100 MHz, quad-band GPRS/EDGE, voice and data, HSDPA category 8, 33.2 x 22.4 x 2.6 mm, 150 pcs/reel
LISA-U200-02S	HSPA 800/850/900/1700/1900/2100 MHz, quad-band GPRS/EDGE, voice and data, HSDPA category 8, 33.2 x 22.4 x 2.6 mm, 150 pcs/reel
LISA-U200-03S	HSPA 800/850/900/1700/1900/2100 MHz, quad-band GPRS/EDGE, voice and data, HSDPA category 8, 33.2 x 22.4 x 2.6 mm, 150 pcs/reel
LISA-U200-52S	HSPA 800/850/900/1700/1900/2100 MHz, quad-band GPRS/EDGE, voice and data, HSDPA category 8, approved by SKT Korean network operator, 33.2 x 22.4 x 2.6 mm, 150 pcs/reel
LISA-U200-62S	HSPA 800/850/900/1700/1900/2100 MHz, quad-band GPRS/EDGE, voice and data, HSDPA category 8, approved by NTT DoCoMo Japanese network operator, 33.2 x 22.4 x 2.6 mm, 150 pcs/reel
LISA-U200-83S	HSPA 800/850/900/1700/1900/2100 MHz, quad-band GPRS/EDGE, voice and data, HSDPA category 8, FOTA available, 33.2 x 22.4 x 2.6 mm, 150 pcs/reel
LISA-U201-03S	HSPA 800/850/900/1900/2100 MHz, quad-band GPRS/EDGE, voice and data, HSDPA category 8, 33.2 x 22.4 x 2.6 mm, 150 pcs/reel
LISA-U201-83S	HSPA 800/850/900/1900/2100 MHz, quad-band GPRS/EDGE, voice and data, HSDPA category 8, FOTA available, 33.2 x 22.4 x 2.6 mm, 150 pcs/reel
LISA-U230-01S	HSPA 800/850/900/1700/1900/2100 MHz, quad-band GPRS/EDGE, voice and data, HSDPA category 14, 33.2 x 22.4 x 2.6 mm, 150 pcs/reel
LISA-U260-01S	HSPA 850/1900 MHz, quad-band GPRS/EDGE, voice and data, HSDPA category 8, 33.2 x 22.4 x 2.6 mm, 150 pcs/reel
LISA-U260-02S	HSPA 850/1900 MHz, quad-band GPRS/EDGE, voice and data, HSDPA category 8, 33.2 x 22.4 x 2.6 mm, 150 pcs/reel
LISA-U270-01S	HSPA 900/2100 MHz, quad-band GPRS/EDGE, voice and data, HSDPA category 8, 33.2 x 22.4 x 2.6 mm, 150 pcs/reel
LISA-U270-02S	HSPA 900/2100 MHz, quad-band GPRS/EDGE, voice and data, HSDPA category 8, 33.2 x 22.4 x 2.6 mm, 150 pcs/reel
LISA-U270-62S	HSPA 900/2100 MHz, quad-band GPRS/EDGE, voice and data, HSDPA category 8, approved and locked for SoftBank Japanese network operator, 33.2 x 22.4 x 2.6 mm, 150 pcs/reel
LISA-U270-63S	HSPA 900/2100 MHz, quad-band GPRS/EDGE, voice and data, HSDPA category 8, approved and locked for SoftBank Japanese network operator, 33.2 x 22.4 x 2.6 mm, 150 pcs/reel
LISA-U270-68S	HSPA 900/2100 MHz, quad-band GPRS/EDGE, voice and data, HSDPA category 8, approved and locked for SoftBank Japanese network operator, 33.2 x 22.4 x 2.6 mm, 150 pcs/reel

Table 37: Product ordering codes

Appendix

A Glossary

Abbreviation	Definition
ACM	Application Communication Module
AMR	Automatic Meter Reading
ANATEL	Agência Nacional de Telecomunicações
AOCC	Advice of Charge Charging
APN	Access Point Name
ATEX	EU Explosive Atmosphere Directive
BER	Bit Error Rate
BIP	Bearer Independent Protocol
CCC	Chinese Compulsory Certification
CDC	Communication Device Class
CDMA	Code-Division Multiple Access
CE	Certification Mark for EHS compliance in the European Economic Area
CLK	Clock
CMOS	Complementary Metal-Oxide-Semiconductor
CPOL	Clock Polarity (for SPI)
CS	Chip Select
CTS	Clear To Send
DC	Direct Current
DCD	Data Carrier Detect
DCE	Data Communication Equipment
DCS	Digital Cellular System
DDC	Display Data Channel
DL	Down Link (Reception)
DRX	Discontinuous Reception
DSR	Data Set Ready
DTE	Data Terminal Equipment
DTMF	Dual Tone Multi Frequency
DTR	Data Terminal Ready
EDGE	Enhanced Data rates for GSM Evolution
EGSM	Extended GSM
EOL	End of Life
ERS	External Reset Input Signal
ESD	Electrostatic Sensitive Device
FCC	Federal Communications Commission
FDD	Frequency Division Duplex
FOAT	Firmware (update) Over AT commands
FOTA	Firmware (update) Over-The-Air
FW	Firmware
GCF	Global Certification Forum
GDI	Generic Digital Interface
GERA	GSM EGPRS Radio Access
GLONASS	GLobal Navigation Satellite System (Russian)


Abbreviation	Definition
GMSK	Gaussian Minimum-Shift Keying modulation
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input/Output
GPRS	General Packet Radio Services
GPS	Global Positioning System
GSM	Global System for Mobile communications
GSMA	GSM (Groupe Spéciale Mobile) Association
HDLC	High-level Data Link Control
HSDPA	High Speed Downlink Packet Access
HSPA	High Speed Packet Access
HSUPA	High Speed Uplink Packet Access
I/O	Input/Output
I ² C	Inter-Integrated Circuit
I ² S	Inter-IC Sound
IC	Integrated Circuit
ICASA	Independent Communications Authority of South Africa
IEC	International Electrotechnical Commission
IMEI	International Mobile Equipment Identity
IPC	Institute for Interconnecting and Packaging Electronic Circuits
ISED	Innovation, Science and Economic Development (Canadian government)
ISO	International Organization for Standardization
ITU	International Telecommunications Union
KCC	Korea Communications Commission
LCS	LoCation Services (protocol)
LTE	Long-Term Evolution
M2M	Machine to Machine
ME	Mobile Equipment
MISO	Multiple Input Single Output
MOSI	Master Output Slave Input
MS	Mobile Station
MSD	Moisture Sensitive Device
MSL	Moisture Sensitivity Level
MUX	Multiplexer
NCC	National Communications Commission
NITZ	Network Identification and Time Zone
NOM	Network Operating Mode
NTC	National Telecommunication Commission
OSI	Open Systems Interconnection
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PCN	Product Change Notification
PD	Pull-Down
PDU	Protocol Data Unit
PLMN	Public Land Mobile Network
PMU	Power Management Unit
PPS	Protocol and Parameter Selection

Abbreviation	Definition
PSAP	Public Safety Answering Point
PTCRB	PCS Type Certification Review Board
PU	Pull-Up
PU/PD	Pull-Up/Pull-Down
RAM	Random Access Memory
RCM	Regulatory Compliance Mark
RF	Radio Frequency
RI	Ring Indicator
RIL	Radio Interface Layer
RMAC	Remote Monitoring Automation and Control
RMC	Reference Measurement Channel
RRC	Radio Resource Control
RRLP	Radio Resource LCS Protocol
RTC	Real Time Counter / Real Time Clock
RTS	Request To Send
SAP	SIM Access Profile
SCL	Serial Clock
SDA	Serial Data
SMLC	Serving Mobile Location Centre
SMS	Short Message Service
SMT	Surface-Mount Technology
SPI	Serial Peripheral Interface
SRDY	Slave Ready
SSL	Secure Sockets Layer
TCP	Transmission Control Protocol
TLS	Transport Layer Security
TS	Technical Specification
TXD	Transmit Data
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
UE	User Equipment
UL	Uplink (Transmission)
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USB	Universal Serial Bus
USSD	Unstructured Supplementary Services Data
UTC	Coordinated Universal Time
VCC	Voltage Collector Collector
VSWR	Voltage Standing Wave Ratio
WA	Word Alignment
WCDMA	Wideband Code-Division Multiple Access

Table 38: Explanation of the abbreviations and terms used

Related documents

- [1] 3GPP TS 27.007 - AT command set for User Equipment (UE)
- [2] 3GPP TS 27.005 - Use of Data Terminal Equipment - Data Circuit terminating; Equipment (DTE - DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)
- [3] 3GPP TS 27.010 - Terminal Equipment to User Equipment (TE-UE) multiplexer protocol
- [4] u-blox AT Commands Manual, Doc. No. UBX-13002752
- [5] u-blox Android RIL Production delivery Application note, Doc. No. UBX-13002041
- [6] u-blox LISA-U2 series System Integration Manual, Doc. No. UBX-13001118
- [7] u-blox GNSS Implementation Application Note, Doc. No. UBX-13001849
- [8] 3GPP TS 26.267 - eCall Data Transfer; In-band modem solution; General description
- [9] 3GPP TS 44.031 - Location Services (LCS); Mobile Station (MS) - Serving Mobile Location Centre (SMLC) Radio Resource LCS Protocol (RRLP)
- [10] ITU-T Recommendation V24, 02-2000. List of definitions for interchange circuits between Data Terminal Equipment (DTE) and Data Connection Equipment (DCE)
- [11] u-blox Mux Implementation Application Note for cellular modules, Doc. No. UBX-13001887
- [12] Universal Serial Bus Revision 2.0 specification,
http://www.usb.org/developers/docs/usb20_docs/
- [13] I²C-bus specification and user manual - Rev. 5 - 9 October 2012 - NXP Semiconductors,
http://www.nxp.com/documents/user_manual/UM10204.pdf
- [14] u-blox SPI Interface Application Note, Doc. No. UBX-13001919
- [15] 3GPP TS 34.121-1 - User Equipment conformance specification; Radio transmission and reception (FDD); Part 1: Conformance specification
- [16] 3GPP TS 51.010-1 - Mobile Station conformance specification; Part 1: Conformance specification
- [17] u-blox Package Information Guide, Doc. No. GPS-X-11004
- [18] 3GPP TS 25.331 - Radio Resource Control (RRC); Protocol specification
- [19] GSMA IoT Device Connection Efficiency Guidelines
- [20] IEC 60079-0 - Explosive atmospheres, Part 0: Equipment general requirements
- [21] IEC 60079-11 - Explosive atmospheres, Part 11: Equipment protection by intrinsic safety 'i'
- [22] IEC 60079-26 - Explosive atmospheres, Part 26: Equipment with EPL Ga

 For regular updates to u-blox documentation and to receive product change notifications, register on our homepage (www.u-blox.com).

Revision history

Revision	Date	Name	Status / Comments
-	25-Jul-2011	lpah	Initial release (draft)
1	12-Oct-2011	sses	First release for LISA-U200-00S, LISA-U200-01x, LISA-U230-01x
2	22-Nov-2011	sses	Updated status to Advance Information Added Antenna Supervisor support by LISA-U200-00S; Added module switch-on by RESET_N support; Updated LISA-U2x0-01x features in GPIO section; Updated ESD maximum rating table
3	02-Feb-2012	sses	Updated status to Preliminary Updated current consumption table; Updated features support in module power off and GPIO sections
A	15-May-2012	sses / lpah	Updated status to Objective Specification Updated PWR_ON low time to switch-on the module; Removed Audio over USB support; Added UART autobauding feature support
A1	20-Jul-2012	sses / lpah	Updated status to Preliminary Updated LISA-U2x0-01x GPRS/EDGE multi-slot class support; Updated list of available USB drivers; Updated module dimensions tolerances
A2	28-Sep-2012	lpah	Updated status to Advance Information First release for LISA-U260-01S, LISA-U270-01S
A3	26-Nov-2012	lpah	Updated status to Preliminary status (Last revision with old doc number, 3G.G3-HW-11004)
B	11-Jul-2013	lpah	Updated status to Advance Information First release for LISA-U200-02S, LISA-U200-61S, LISA-U200-62S, LISA-U260-02S, LISA-U270-02S, LISA-U270-62S
B1	20-Aug-2013	lpah	Updated status to Preliminary (Early Production Information)
B2	29-Aug-2013	smos	Changes in Tables 1 and 36 (variant 61S removed)
R12	14-Apr-2014	lpah	First release for LISA-U200-52S, LISA-U200-82S Section 1.5: added Windows Mobile 6.5 and Android 4.2 and 4.3
R13	15-May-2015	sfal	Extended applicability to LISA-U200-03S and LISA-U201-03S. Added related features. Removed LISA-U200-00S (which is in EOL). Updated approvals section 6.2 and current consumption table of section 4.2.4.
R14	26-Jun-2015	sfal	Advance Information document status
R15	10-Aug-2015	sfal	Early Production Information document status Extended applicability to LISA-U200-83S and LISA-U270-68S
R16	17-Feb-2016	sfal	Extended applicability to LISA-U201-83S
R17	12-May-2016	lpah	Extended applicability to LISA-U201-03A and LISA-U270-63S
R18	07-Oct-2016	lpah	Updated status to Production Information Extended applicability to the LISA-U200-62S-02 and removed LISA-U201-03A, LISA-U200-82S
R19	03-Jan-2018	lpah	"Disclosure restriction" replaces "Document status" on page 2 and document footer. Extended document applicability to new type numbers
R20	24-Jan-2019	sses	Extended applicability to the LISA-U200-01S-03, LISA-U200-03S-02, LISA-U200-52S-03, LISA-U200-62S-04, LISA-U230-01S-03, LISA-U270-63S-02 Updated products' status Revised approvals info Updated RESET_N specifications for LISA-U201 modules

Contact

For complete contact information, visit us at www.u-blox.com.

u-blox Offices

North, Central and South America

u-blox America, Inc.

Phone: +1 703 483 3180
E-mail: info_us@u-blox.com

Regional Office West Coast:

Phone: +1 408 573 3640
E-mail: info_us@u-blox.com

Technical Support:

Phone: +1 703 483 3185
E-mail: support@u-blox.com

Headquarters

Europe, Middle East, Africa

u-blox AG

Phone: +41 44 722 74 44
E-mail: info@u-blox.com
Support: support@u-blox.com

Asia, Australia, Pacific

u-blox Singapore Pte. Ltd.

Phone: +65 6734 3811
E-mail: info_ap@u-blox.com
Support: support_ap@u-blox.com

Regional Office Australia:

Phone: +61 2 8448 2016
E-mail: info_anz@u-blox.com
Support: support_ap@u-blox.com

Regional Office China (Beijing):

Phone: +86 10 68 133 545
E-mail: info_cn@u-blox.com
Support: support_cn@u-blox.com

Regional Office China (Chongqing):

Phone: +86 23 6815 1588
E-mail: info_cn@u-blox.com
Support: support_cn@u-blox.com

Regional Office China (Shanghai):

Phone: +86 21 6090 4832
E-mail: info_cn@u-blox.com
Support: support_cn@u-blox.com

Regional Office China (Shenzhen):

Phone: +86 755 8627 1083
E-mail: info_cn@u-blox.com
Support: support_cn@u-blox.com

Regional Office India:

Phone: +91 80 405 092 00
E-mail: info_in@u-blox.com
Support: support_in@u-blox.com

Regional Office Japan (Osaka):

Phone: +81 6 6941 3660
E-mail: info_jp@u-blox.com
Support: support_jp@u-blox.com

Regional Office Japan (Tokyo):

Phone: +81 3 5775 3850
E-mail: info_jp@u-blox.com
Support: support_jp@u-blox.com

Regional Office Korea:

Phone: +82 2 542 0861
E-mail: info_kr@u-blox.com
Support: support_kr@u-blox.com

Regional Office Taiwan:

Phone: +886 2 2657 1090
E-mail: info_tw@u-blox.com
Support: support_tw@u-blox.com