Industrial MLC
CF Card
-240 Series
Product Manual

June 7, 2023

www.cactus-tech.com

The information in this manual is believed to be accurate at the time of publication but is subject to change without notice. Cactus Technologies Limited shall not be liable for technical or editorial errors or omissions contained herein; nor for incidental or consequential damages resulting from the furnishing, performance, or use of this material.

Cactus Technologies® makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Cactus Technologies® assume any liability arising out of the application or use of its products, and specifically disclaims any and all liability, including without limitation consequential or incidental damages.

Cactus Technologies® products are not designed, intended or authorized for use as components in systems intended for surgical implant into the body or in other applications intended to support or sustain life or for any application where the failure of a Cactus Technologies® product can result in personal injury or death. Users of Cactus Technologies® products for such unintended and unauthorized applications shall assume all risk of such use and shall indemnify and hold Cactus Technologies® and its officers, employees, subsidiaries, affiliates and distributors harmless against all claims, costs, damages, expenses and attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended and unauthorized use, even if such claim alleges that Cactus Technologies® was negligent regarding the design or manufacture of the part.

Table of Contents

1.Introduction to Cactus Technologies Industrial MLC CF -240 Series Products

Features:

- Solid state design with no moving parts
- Industry standard CF Type I form factor
- Supports TrueIDE Mode
- Supports ATA PIO Modes 0-6 in TrueIDE Mode
- Supports MultiWord DMA Modes 0-4 in TrueIDE Mode
- Supports UDMA Modes 0-7
- Supports ATA Security Feature Set
- 70-bit/1KB BCH ECC
- Intelligent power management to reduce power consumption
- Dual voltage support: 3.3V/5.0V

Overview:

Cactus Technologies® -240 Series CompactFlash Memory Card (CF) is a high capacity solid-state flash memory product that complies with the Compact Flash Association standard. It also supports True IDE Mode, which is electrically compatible with an IDE disk drive. CompactFlash Memory Cards provide up to 128GB of formatted storage capacity in the CF Type I form factor.

Cactus Technologies® Industrial MLC CF products use high quality Industrial Grade MLC NAND flash from Kioxia Corporation. In addition, it includes an on-card intelligent controller that manages interface protocols, data storage and retrieval as well as ECC, defect handling and diagnostics, power management, and clock control.

1.1. Supported Standards

Cactus Technologies® CompactFlash Memory Cards are fully compliant with the following specifications:

- *PCMCIA PC Card Standard v2.1*
- *PCMCIA PC Card ATA Specification*
- *CompactFlash Specification 6.0*
- ANSI ATA8

1.1. Product Features

Cactus Technologies® Industrial MLC CompactFlash Cards contain a high level, intelligent controller. This intelligent controller provides many capabilities not found in other types of memory cards. These capabilities include the following:

- Standard ATA register and command set (same as found on most magnetic disk drives).
- Manages details of erasing and programming flash memory independent of the host system
- Sophisticated defect managing capabilities (similar to magnetic disk drives).
- Sophisticated system for error recovery using powerful error correction code (ECC).
- Intelligent power management for low power operation.

1.1.1. Host and Technology Independence

Cactus Technologies® Industrial MLC CF Cards appears as a standard ATA disk drive to the host system. The card utilizes a 512-byte sector which is the same as that in an IDE magnetic disk drive. To write or read a sector (or multiple sectors), the host computer software simply issues an ATA Read or Write command to the card as per the ATA protocol. The host software then waits for the command to complete. The host system does not get involved in the details of how the flash memory is erased, programmed or read as this is all managed by the built-in controller in the card. Also, with the intelligent on-board controller, the host system software will not require changing as new flash memory evolves. Thus, systems that support Cactus Technologies® Industrial MLC CF products today will continue to work with future Cactus Technologies® Industrial MLC CF cards built with new flash technology without having to update or change host software.

1.1.2. Defect and Error Management

Cactus Technologies® Industrial MLC CF cards contain a sophisticated defect and error management system similar to those found in magnetic disk drives. The defect management is completely transparent to the host and does not consume any user data space.

The soft error rate for Cactus Technologies® Industrial MLC CF cards is much lower than that of magnetic disk drives. In the extremely rare case where a read error does occur, the card has sophisticated ECC to recover the data.

These defect and error management systems, coupled with the solid-state construction, give Cactus Technologies® Industrial MLC CF cards unparalleled reliability.

1.1.3. Intelligent Power Management

Cactus Technologies® Industrial MLC CF cards employ sophisticated power management algorithms to conserve power. Upon completion of a command, the card will automatically enter sleep mode if no further commands are received. In most situations, the card will be in sleep mode except when the host is accessing it, thus conserving power. The delay from command completion to entering sleep mode can be adjusted.

When the card is in sleep mode, any command issued to the card will cause it to exit sleep and respond.

1.1.4. Power Supply Requirements

This is a dual voltage product, which means it will operate at a voltage range of 3.30 volts ±5% or 5.00 volts ± 10%.

2.Product Specifications

For all the following specifications, values are defined at ambient temperature and nominal supply voltage unless otherwise stated.

2.1. System Environmental Specifications

Table 2-1. Environmental Specifications

		Cactus Technologies® -240 CF Products
Temperature	Operating:	0°C to 70°C (standard temp.) -40° C to +85° C (extended temp.)
Humidity	Operating & Non-Operating:	8% to 95%, non-condensing
Acoustic Noise		0 dB
Vibration	Operating & Non-Operating:	30 G peak to peak maximum
Shock	Operating & Non-Operating:	3,000 G maximum
Altitude (relative to sea level)	Operating & Non-Operating:	100,000 feet maximum

2.2. System Power Requirements

Table 2-2. Power Requirements

		Cactus Technologies® -240 CF Products
DC Input Voltage (VCC) **100 mV max. ripple (p-p)**		5.0V ± 10% 3.3V ± 5%
(Maximum Average Value) **See Notes.**	Sleep: Reading: Writing:	1mA 4GB, 8GB: 200mA 16-128GB: 275mA 4GB, 8GB: 120mA 16GB: 165mA 32GB, 64GB: 260mA 128GB: 330mA

NOTES: All values quoted are typical at ambient temperature and nominal supply voltage unless otherwise stated.

Sleep mode is specified under the condition that all card inputs are static CMOS levels and in a “Not Busy“ operating state.

2.3. System Performance

All performance numbers are typical values assuming the card controller is in the default (i.e., fastest) mode.

Table 2-3. Performance

Read Transfer Rate	4GB, 8GB 16-128GB	up to 80MB/s up to 110MB/s
Write Transfer Rate	4GB 8GB 16GB 32GB,64GB 128GB	up to 15MB/s up to 30MB/s up to 50MB/s up to 70MB/s up to 80MB/s

* Please note that for maximum performance in TrueIDE UDMA modes, proper termination and PCB layout guidelines as described in the ATA specifications must be followed to minimize signal integrity problems. Maximum transfer rates are achieved on 4GB or higher capacity cards.

2.4. System Reliability

Table 2-4. Reliability

Data Reliability	< 1 non-recoverable error in 10^{14} bits READ
Estimated TBW*	4GB: 12TB 8GB: 24TB 16GB: 48TB 32GB: 96TB 64GB: 192TB 128GB: 384TB

**Note: TBW estimation is for large block sequential writes*

2.5. Physical Specifications

The following sections provide the physical specifications for Cactus Technologies® Industrial MLC CompactFlash products.

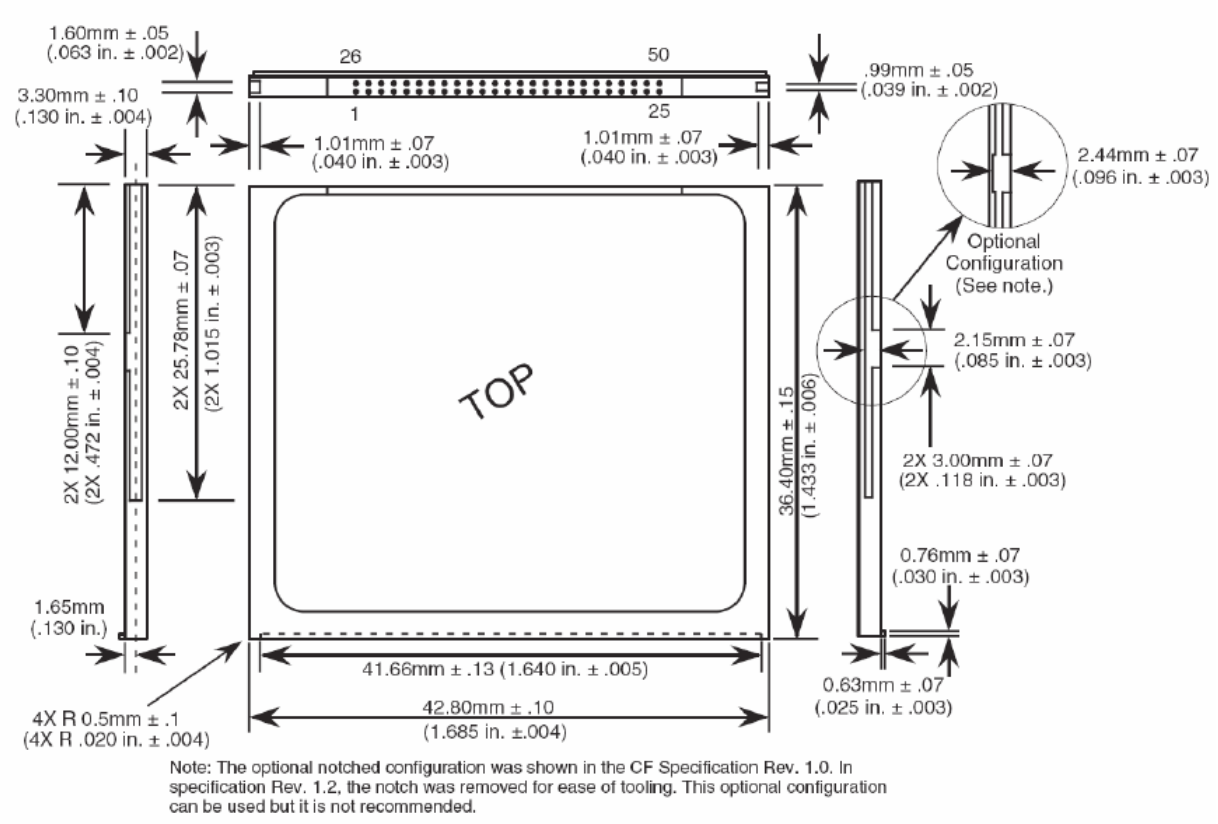
2.5.1. CompactFlash Physical Specifications

Refer to Table 2-5 and see Figure 2-2 for CompactFlash Memory Card physical specifications and dimensions.

Table 2-5. CompactFlash Physical Specifications

	CompactFlash
Weight:	11.4 g (.40 oz) typical, 14.2 g (.50 oz) maximum
Length:	36.40 ± 0.15 mm (1.433 ±.006 in)
Width:	42.80 ± 0.10 mm (1.685 ±.004 in)
Thickness:	3.3 mm ± 0.10 mm (.130 ±.004 in) (Excluding Lip)

Figure 2-1. CompactFlash Memory Card Dimensions



Note: The optional notched configuration was shown in the CF Specification Rev. 1.0. In specification Rev. 1.2, the notch was removed for ease of tooling. This optional configuration can be used but it is not recommended.

2.6. Capacity Specifications

Cactus Technologies® Industrial MLC CF Cards are available in capacities of 4,8,16,32,64 & 128GBytes.

3.Interface Description

The following sections provide detailed information on Cactus Technologies® Industrial MLC CompactFlash card interface.

3.1. CF Pin Assignments and Pin Type

The signal/pin assignments are listed in Table 3-6. Low active signals have a "-" prefix. Pin types are Input, Output or Input/Output. Sections 3.3.1 to 3.3.4 define the DC characteristics for all input and output type structures.

Table 3-6. CompactFlash Pin Assignments and Pin Type

PC Card Memory Mode			PC Card I/O Mode			True IDE Mode		
Pin Num	Signal Name	Pin Type	Pin Num	Signal Name	Pin Type	Pin Num	Signal Name	Pin Type
1	GND		1	GND		1	GND	
2	D03	I/O	2	D03	I/O	2	D03	I/O
3	D04	I/O	3	D04	I/O	3	D04	I/O
4	D05	I/O	4	D05	I/O	4	D05	I/O
5	D06	I/O	5	D06	I/O	5	D06	I/O
6	D07	I/O	6	D07	I/O	6	D07	I/O
7	-CE1	I	7	-CE1	I	7	-CS0	I
8	A10	I	8	A10	I	8	A10[2]	I
9	-OE	I	9	-OE	I	9	-ATA SEL	I
10	A09	I	10	A09	I	10	A09[2]	I
11	A08	I	11	A08	I	11	A08[2]	I
12	A07	I	12	A07	I	12	A07[2]	I
13	VCC		13	VCC		13	VCC	
14	A06	I	14	A06	I	14	A06[2]	I
15	A05	I	15	A05	I	15	A05[2]	I
16	A04	I	16	A04	I	16	A04[2]	I
17	A03	I	17	A03	I	17	A03[2]	I
18	A02	I	18	A02	I	18	A02	I
19	A01	I	19	A01	I	19	A01	I
20	A00	I	20	A00	I	20	A00	I
21	D00	I/O	21	D00	I/O	21	D00	I/O
22	D01	I/O	22	D01	I/O	22	D01	I/O
23	D02	I/O	23	D02	I/O	23	D02	I/O
24	WP	O	24	-IOIS16	O	24	-IOCS16	O
25	-CD2	O	25	-CD2	O	25	-CD2	O
26	-CD1	O	26	-CD1	O	26	-CD1	O
27	D11[1]	I/O	27	D11[1]	I/O	27	D11[1]	I/O
28	D12[1]	I/O	28	D12[1]	I/O	28	D12[1]	I/O
29	D13[1]	I/O	29	D13[1]	I/O	29	D13[1]	I/O
30	D14[1]	I/O	30	D14[1]	I/O	30	D14[1]	I/O
31	D15[1]	I/O	31	D15[1]	I/O	31	D15[1]	I/O
32	-CE2[1]	I	32	-CE2[1]	I	32	-CS1[1]	I
33	-VS1	O	33	-VS1	O	33	-VS1	O

PC Card Memory Mode			PC Card I/O Mode			True IDE Mode		
34	-IORD	I	34	-IORD	I	34	-IORD HSTROBE[5] -HDMARDY[6]	I
35	-IOWR	I	35	-IOWR	I	35	-IOWR STOP[7]	I
36	-WE	I	36	-WE	I	36	-WE[3]	I
37	RDY/BSY	O	37	IREQ	O	37	INTRQ	O
38	VCC		38	VCC		38	VCC	
39	-CSEL	I	39	-CSEL	I	39	-CSEL	I
40	-VS2	O	40	-VS2	O	40	-VS2	O
41	RESET	I	41	RESET	I	41	-RESET	I
42	-WAIT	O	42	-WAIT	O	42	IORDY -DDMARDY[5] DSTROBE[6]	O
43	-INPACK	O	43	-INPACK	O	43	DMARQ	O
44	-REG	I	44	-REG	I	44	-DMACK	I
45	BVD2	I/O	45	-SPKR	I/O	45	-DASP	I/O
46	BVD1	I/O	46	-STSCHG	I/O	46	-PDIAG	I/O
47	D08[1]	I/O	47	D08[1]	I/O	47	D08[1]	I/O
48	D09[1]	I/O	48	D09[1]	I/O	48	D09[1]	I/O
49	D10[1]	I/O	49	D10[1]	I/O	49	D10[1]	I/O
50	GND		50	GND		50	GND	

NOTE:

1. These signals are required only for 16-bit access and not required when installed in 8-bit systems. For lowest power dissipation, leave these signals open.
2. Should be grounded by the host.
3. Should be tied to VCC by the host.
4. Please refer to Section 3.2 for definitions of In, Out type.
5. Signal usage when UDMA write protocol is active.
6. Signal usage when UDMA read protocol is active.
7. Signal usage when UDMA protocol is active.

3.1. Signal Description

Cactus Technologies® Industrial MLC CompactFlash products can be configured to operate in either I/O mode or memory mode as per the *PCMCIA Release 2.1 specification*. The configuration of the CompactFlash cards are controlled using the standard PCMCIA configuration registers starting at address 200h in the Attribute Memory space of the CompactFlash Memory Card. Cactus Technologies® Industrial MLC CompactFlash cards also supports a TrueIDE mode. This mode is entered by grounding the –OE pin on power up.

Table 3-7 describes the I/O signals. Signals whose source is the host are designated as inputs while signals that the CompactFlash Memory Card sources are outputs. CompactFlash Card logic levels conform to those specified in the *PCMCIA Release 2.1 Specification*. See Section 3.3 for definitions of Input and Output type.

Table 3-7. Signal Description

Signal Name	Dir.	Description
A10—A0 (CF Card Memory Mode)	I	These address lines along with the -REG signal are used to select the following: The I/O port address registers within the CompactFlash Card, the memory mapped port address registers within the card, a byte in the card's information structure and its configuration control and status registers.
A10—A0 (CF Card I/O Mode)		This signal is the same as the CF Card Memory Mode signal.
A2—A0 (True IDE Mode) A10—A3 (True IDE Mode)	I	In True IDE Mode only A[2:0] is used to select the one of eight registers in the Task File. In True IDE Mode these remaining address lines should be grounded by the host.
BVD1 (CF Card Memory Mode)	I/O	This signal is asserted high as the BVD1 signal since a battery is not used with this product.
-STSCHG (CF Card I/O Mode) Status Changed		This signal is asserted low to alert the host to changes in the RDY/-BSY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status Register.
-PDIAG (True IDE Mode)		In True IDE Mode, this input/output is the Pass Diagnostic signal in the Master/Slave handshake protocol.
BVD2 (CF Card Memory Mode)	I/O	This output line is always driven to a high state in Memory Mode since a battery is not required for this product.
-SPKR (CF Card I/O Mode)		This output line is always driven to a high state in I/O Mode since this product does not support the audio function.
-DASP (True IDE Mode)		In True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
-CD1, -CD2 (CF Card Memory Mode)	O	These Card Detect pins are connected to ground on the CompactFlash Card. They are used by the host to determine if the card is fully inserted into its socket.
-CD1, -CD2 (CF Card I/O Mode)		This signal is the same for all modes.
-CD1, -CD2 (True IDE Mode)		This signal is the same for all modes.
-CE1, -CE2 (CF Card Memory Mode) Card Enable	I	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. -CE2 always accesses the odd byte of the word. -CE1 accesses the even byte or the Odd byte of the word depending on A0 and -CE2. A multiplexing scheme based on A0, -CE1, and -CE2 allows 8 bit hosts to access all data on D0-D7. See Tables 3-11, 3-12, 3-15, and 3-16.
-CE1, -CE2 (CF Card I/O Mode) Card Enable		This signal is the same as the CF Card Memory Mode signal.
-CS0, -CS1 (True IDE Mode)		In True IDE Mode -CS0 is the chip select for the task file registers while -CS1 is used to select the Alternate Status Register and the Device Control Register.
-CSEL (CF Card Memory Mode)	I	This signal is not used for this mode.
-CSEL (CF Card I/O Mode)		This signal is not used for this mode.
-CSEL (True IDE Mode)		This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.

Signal Name	Dir.	Description
D15—D00 (CF Card Memory Mode)	I/O	These lines carry the Data, Commands and Status information between the host and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word.
D15—D00 (CF Card I/O Mode)		These signals are the same as the CF Card Memory Mode signal.
D15—D00 (True IDE Mode)		In True IDE Mode all Task File operations occur in byte mode on the low order bus D00-D07 while all data transfers are 16 bits using D00-D15.
GND (CF Card Memory Mode)	--	Ground.
GND (CF Card I/O Mode)		This signal is the same for all modes.
GND (True IDE Mode)		This signal is the same for all modes.
-INPACK (CF Card Memory Mode)	O	This signal is not used in this mode.
-INPACK (CF Card I/O Mode) Input Acknowledge		The Input Acknowledge signal is asserted by the CompactFlash Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the card and the CPU.
DMARQ (True IDE Mode)		In True IDE Mode, this pin is an output from the card to request DMA mode transfer.
-IORD (CF Card Memory Mode)	I	This signal is not used in this mode.
-IORD (CF Card I/O Mode)		This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the CompactFlash Card when the card is configured to use the I/O interface.
-IORD (True IDE Mode, UDMA not active) -HDMARDY (TrueIDE Mode, UDMA read) HSTROBE (TrueIDE Mode, UDMA write)		In True IDE Mode, when UDMA protocol is not active, this signal has the same function as in CF Card I/O Mode. In TrueIDE Mode, when UDMA read protocol is active, this signal is asserted by the host to indicate that it is ready to receive data-in bursts. In TrueIDE Mode, when UDMA write protocol is active, this signal is the data out strobe sent by the host. Data is latched by the device on both rising and falling edges of this signal.
-IOWR (CF Card Memory Mode)	I	This signal is not used in this mode.
-IOWR (CF Card I/O Mode)		The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompactFlash controller registers when the card is configured to use the I/O interface. The clocking will occur on the negative to positive edge of the signal (trailing edge).
-IOWR (True IDE Mode, UDMA not active) STOP (TrueIDE Mode, UDMA active)		In True IDE Mode, when UDMA protocol is not active, this signal has the same function as in CF Card I/O Mode. In TrueIDE Mode, when UDMA protocol is active, host asserts this signal to terminate the UDMA transfer.

Signal Name	Dir.	Description
-OE (CF Card Memory Mode)	I	This is an Output Enable strobe generated by the host interface. It is used to read data from the CompactFlash Card in Memory Mode and to read the CIS and configuration registers.
-OE (CF Card I/O Mode)		In CF Card I/O Mode, this signal is used to read the CIS and configuration registers.
-ATA SEL (True IDE Mode)		To enable True IDE Mode, this input should be grounded by the host.
RDY/-BSY (CF Card Memory Mode)	O	In Memory Mode this signal is set high when the CompactFlash Card is ready to accept a new data transfer operation and held low when the card is busy. The Host memory card socket must provide a pull-up resistor. At power up and at Reset, the RDY/-BSY signal is held low (busy) until the CompactFlash Card has completed its power up or reset function. No access of any type should be made to the CompactFlash Card during this time. The RDY/-BSY signal is held high (disabled from being busy) whenever the following condition is true: The CompactFlash Card has been powered up with +RESET continuously disconnected or asserted.
-IREQ (CF Card I/O Mode)		I/O Operation—After the CompactFlash Card has been configured for I/O operation, this signal is used as -Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt.
INTRQ (True IDE Mode)		In True IDE Mode, this signal is the active high Interrupt Request to the host.
-REG (CF Card Memory Mode) Attribute Memory Select	I	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory.
-REG (CF Card I/O Mode)		The signal must also be active (low) during I/O Cycles when the I/O address is on the Bus.
-DMACK (True IDE Mode)		In True IDE Mode, this is an input from the host to signal that the DMA request from the device has been acknowledged.
RESET (CF Card Memory Mode)	I	When the pin is high, this signal resets the CompactFlash Card. The card is Reset only at power up if this pin is left high or open from power-up. The card is also reset when the Soft Reset bit in the Card Configuration Option Register is set.
RESET (CF Card I/O Mode)		This signal is the same as the CF Card Memory Mode signal.
-RESET (True IDE Mode)		In True IDE Mode, this input pin is the active low hardware reset from the host.
VCC (CF Card Memory Mode)	--	+5 V, +3.3 V power.
VCC (CF Card I/O Mode)		This signal is the same for all modes.
VCC (True IDE Mode)		This signal is the same for all modes.
-VS1 -VS2 (CF Card Memory Mode)	O	Voltage Sense Signals. -VS1 is grounded so that the CompactFlash Card CIS can be read at 3.3 volts and -VS2 is open and reserved by CF Card for a secondary voltage.
-VS1 -VS2 (CF Card I/O Mode)		This signal is the same for all modes.
-VS1 -VS2 (True IDE Mode)		This signal is the same for all modes.
-WAIT (CF Card Memory Mode)	O	The –WAIT signal is driven by the CompactFlash Card to signal to the host to delay completion of the memory cycle in progress.

Signal Name	Dir.	Description
-WAIT (CF Card I/O Mode)		The –WAIT signal is driven by the CompactFlash Card to signal to the host to delay completion of the I/O cycle in progress.
-IORDY (True IDE Mode, UDMA not active) -DDMARDY (TrueIDE Mode, UDMA write active) DSTROBE (TrueIDE Mode, UDMA read active)		In TrueIDE Mode, when UDMA protocol is not active, this signal is driven by the device to extend the I/O cycle in progress. In TrueIDE Mode, when UDMA write protocol is active, this signal is asserted by the device to indicate that it is ready to receive a data out burst. In TrueIDE Mode, when UDMA read protocol is active, this signal is the data strobe sent by the device to the host. The host latches data on both the rising and falling edges of this signal.
-WE (CF Card Memory Mode)	I	This is a signal driven by the host and used for strobing memory write data to the registers of the CompactFlash Card when the card is configured in the memory interface mode. It is also used for writing the configuration registers.
-WE (CF Card I/O Mode)		In CF Card I/O Mode, this signal is used for writing the configuration registers.
Reserved (True IDE Mode)		In True IDE Mode this input signal is not used and should be connected to VCC by the host.
WP (CF Card Memory Mode) Write Protect	O	Memory Mode—The CompactFlash Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.
-IOIS16 (CF Card I/O Mode)		I/O Operation—When the CompactFlash Card is configured for I/O Operation, Pin 24 is used for the -I/O Selected is 16 Bit Port (-IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port.
-IOCS16 (True IDE Mode)		In True IDE Mode, this output signal is asserted low when this device is expecting a word data transfer cycle.

3.2. Electrical Specification

The following table defines all D.C. Characteristics for the -240 series CompactFlash Memory Card. Unless otherwise stated, conditions are:

Vcc = 5V ± 10% or Vcc = 3.3V ± 5%
Ta = -40°C to 85°C

3.2.1. Absolute Maximum Ratings

Parameter	Symbol	MIN	MAX	Units
Storage Temperature	Ts	-55	100	°C
Operating Temperature	T_A	-40	85	°C
Vcc with respect to GND	Vcc	-0.3	6.5	V

3.2.2. DC Characteristics

Parameter	Symbol	MIN	MAX	Units
Input Voltage	Vin	-0.5	Vcc + 0.5	V
Output Voltage	Vout	-0.3	Vcc + 0.3	V
Operating Current Sleep Mode Active	I_{CC}		 1 335	mA

3.2.3. AC Characteristics

Cactus Technologies® CF Cards meet all the timing requirements as specified in *CompactFlash Specification 4.1 and PCMCIA PC Card Standard v2.1*. Please refer to those documents for details on interface AC timing diagrams and specifications.

3.3. Card Configuration

CompactFlash Memory Cards are identified by information in the Card Information Structure (CIS). The entries in Table 3-8 and Table 3-9 show how to access the various registers and address spaces in the memory cards.

Table 3-8. Registers and Memory Space Decoding

-CE2	-CE1	-REG	-OE	-WE	A10	A9	A8-A4	A3	A2	A1	A0	SELECTED SPACE
1	1	X	X	X	X	X	XX	X	X	X	X	Standby
X	0	0	0	1	X	1	XX	X	X	X	0	Configuration Registers Read
1	0	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 Bit D7-D0)
0	1	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 Bit D15-D8)
0	0	1	0	1	X	X	XX	X	X	X	0	Common Memory Read (16 Bit D15-D0)
X	0	0	1	0	X	1	XX	X	X	X	0	Configuration Registers Write
1	0	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 Bit D7-D0)
0	1	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 Bit D15-D8)
0	0	1	1	0	X	X	XX	X	X	X	0	Common Memory Write (16 Bit D15-D0)
X	0	0	0	1	0	0	XX	X	X	X	0	Card Information Structure Read
1	0	0	1	0	0	0	XX	X	X	X	0	Invalid Access (CIS Write)
1	0	0	0	1	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Read)
1	0	0	1	0	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Write)
0	1	0	0	1	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Read)
0	1	0	1	0	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Write)

Table 3-9. Configuration Registers Decoding

-CE2	-CE1	-REG	-OE	-WE	A10	A9	A8-A4	A3	A2	A1	A0	SELECTED REGISTER
X	0	0	0	1	0	1	00	0	0	0	0	Configuration Option Reg Read
X	0	0	1	0	0	1	00	0	0	0	0	Configuration Option Reg Write
X	0	0	0	1	0	1	00	0	0	1	0	Card Status Register Read
X	0	0	1	0	0	1	00	0	0	1	0	Card Status Register Write
X	0	0	0	1	0	1	00	0	1	0	0	Pin Replacement Register Read
X	0	0	1	0	0	1	00	0	1	0	0	Pin Replacement Register Write
X	0	0	0	1	0	1	00	0	1	1	0	Socket and Copy Register Read
X	0	0	1	0	0	1	00	0	1	1	0	Socket and Copy Register Write

NOTE: The location of the card configuration registers should always be read from the CIS since these locations may vary in future products. No writes should be performed to the CompactFlash Memory Card attribute memory except to the card configuration register addresses. All other attribute memory locations are reserved.

3.3.1. Attribute Memory Function

Attribute memory is a space where CompactFlash Memory Card CIS and configurations registers are stored, and is limited to 8-bit wide accesses only at even addresses.

As in the Main Memory Read functions, the signals -CE1 and -CE2 control the even-byte and odd-byte address, but only the even-byte data is valid during the Attribute Memory access. Refer to Table 3-10 for signal states and bus validity for the Attribute Memory function.

Table 3-10. Attribute Memory Function

Function Mode	-REG	-CE2	-CE1	A9	A0	-OE	-WE	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	X	High Z	High Z
Read Byte Access CIS ROM (8 bits)	L	H	L	L	L	L	H	High Z	Even Byte
Write Byte Access CIS (8 bits) (Invalid)	L	H	L	L	L	H	L	Do not care	Even Byte
Read Byte Access Configuration (8 bits)	L	H	L	H	L	L	H	High Z	Even Byte
Write Byte Access Configuration (8 bits)	L	H	L	H	L	H	L	Do not care	Even Byte
Read Word Access CIS (16 bits)	L	L	L	L	X	L	H	Not Valid	Even Byte
Write Word Access CIS (16 bits) (Invalid)	L	L	L	L	X	H	L	Do not care	Even Byte
Read Word Access Configuration (16 bits)	L	L	L	H	X	L	H	Not Valid	Even Byte
Write Word Access Configuration (16 bits)	L	L	L	H	X	H	L	Do not care	Even Byte

NOTE: The -CE signal or both the -OE signal and the -WE signal must be de-asserted between consecutive cycle operations.

3.3.2. Configuration Option Register (Address 200h in Attribute Memory)

The Configuration Option Register is used to configure the cards interface, address decoding and interrupt and to issue a soft reset to the CompactFlash Memory Card.

Operation	D7	D6	D5	D4	D3	D2	D1	D0
R/W	SRESET	LevlREQ	Conf5	Conf4	Conf3	Conf2	Conf1	Conf0

SRESET Soft Reset—Setting this bit to one (1), waiting the minimum reset width time and returning to zero (0) places the CompactFlash Memory Card in the Reset state. Setting this bit to one (1) is equivalent to assertion of the +RESET signal except that the SRESET bit is not cleared. Returning this bit to zero (0) leaves the CompactFlash Memory Card in the same un-configured, Reset state as following power-up and hardware reset. This bit is set to zero (0) by power-up and hardware reset. Using the Soft Reset is considered a hard Reset by the ATA Commands. Contrast with Soft Reset in the Device Control Register.

LevlREQ This bit is set to one (1) when Level Mode Interrupt is selected, and zero (0) when Pulse Mode is selected. Set to zero (0) by Reset.

Conf5—Conf0 Configuration Index. Set to zero (0) by reset. It's used to select operation mode of the CompactFlash Memory Card as shown below.

NOTE: Conf5 and Conf4 are reserved and must be written as zero (0).

Table 3-11. Card Configurations

Conf5	Conf4	Conf3	Conf2	Conf1	Conf0	Disk Card Mode
0	0	0	0	0	0	Memory Mapped
0	0	0	0	0	1	I/O Mapped, Any 16 byte system decoded boundary
0	0	0	0	1	0	I/O Mapped, 1F0-1F7/3F6-3F7
0	0	0	0	1	1	I/O Mapped, 170-177/376-377

3.3.3. Card Configuration and Status Register (Address 202h in Attribute Memory)

The Card Configuration and Status Register contain information about the Card’s condition.

Table 3-12. Card Configuration and Status Register Organization

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Changed	SigChg	IOis8	0	0	PwrDwn	Int	0
Write	0	SigChg	IOis8	0	0	PwrDwn	0	0

Changed Indicates that one or both of the Pin Replacement register CRdy, or CWProt bits are set to one (1). When the Changed bit is set, -STSCHG Pin 46 is held low if the SigChg bit is a One (1) and the CompactFlash Memory Card is configured for the I/O interface.

SigChg This bit is set and reset by the host to enable and disable a state-change “signal” from the Status Register, the Changed bit control pin 46 the Changed Status signal. If no state change signal is desired, this bit should be set to zero (0) and pin 46 (-STSCHG) signal will be held high while the CompactFlash Memory Card is configured for I/O.

IOis8 The host sets this bit to a one (1) if the CompactFlash Memory Card is to be configured in an 8-bit I/O mode. The CompactFlash Card is always configured for both 8- and 16-bit I/O, so this bit is ignored.

PwrDwn This bit indicates whether the host requests the CompactFlash Memory Card to be in the power saving or active mode. When the bit is one (1), the CompactFlash Card enters a power down mode. When zero (0), the host is requesting the CompactFlash Card to enter the active mode. The PC Card Rdy/-Bsy value becomes BUSY when this bit is changed. Rdy/-Bsy will not become Ready until the power state requested has been entered. The CompactFlash Card automatically powers down when it is idle and powers back up when it receives a command.

Int This bit represents the internal state of the interrupt request. This value is available whether or not I/O interface has been configured. This signal remains true until the condition that caused the interrupt request has been serviced. If interrupts are disabled by the -IEN bit in the Device Control Register, this bit is a zero (0).

3.3.4. Pin Replacement Register (Address 204h in Attribute Memory)

Table 3-13. Pin Replacement Register

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	0	CRdy/-Bsy	CWProt	1	1	RRdy/-Bsy	RWProt
Write	0	0	CRdy/-Bsy	CWProt	0	0	MRdy/-Bsy	MWProt

CRdy/-Bsy This bit is set to one (1) when the bit RRdy/-Bsy changes state. This bit can also be written by the host.

CWProt This bit is set to one (1) when the RWprot changes state. This bit may also be written by the host.

RRdy/-Bsy This bit is used to determine the internal state of the Rdy/-Bsy signal. This bit may be used to determine the state of the Ready/-Busy as this pin has been reallocated for use as Interrupt Request on an I/O card. When written, this bit acts as a mask for writing the corresponding bit CRdy/-Bsy.

RWProt This bit is always zero (0) since the CompactFlash Memory Card does not have a Write Protect switch. When written, this bit acts as a mask for writing the corresponding bit CWProt.

MRdy/-Bsy This bit acts as a mask for writing the corresponding bit CRdy/-Bsy.

MWProt This bit when written acts as a mask for writing the corresponding bit CWProt.

Table 3-14. Pin Replacement Changed Bit/Mask Bit Values

Initial Value of (C) Status	Written by Host		Final "C" Bit	Comments
	"C" Bit	"M" Bit		
0	X	0	0	Unchanged
1	X	0	1	Unchanged
X	0	1	0	Cleared by Host
X	1	1	1	Set by Host

3.3.5. Socket and Copy Register (Address 206h in Attribute Memory)

This register contains additional configuration information. This register is always written by the system before writing the card's Configuration Index Register.

Table 3-15. Socket and Copy Register Organization

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Reserved	0	0	Drive #	0	0	0	0
Write	0	0	0	Drive # (0)	X	X	X	X

Reserved This bit is reserved for future standardization. This bit must be set to zero (0) by the software when the register is written.

Drive # This bit indicates the drive number of the card if twin card configuration is supported.

X The socket number is ignored by the CompactFlash Memory Card.

3.4. I/O Transfer Function

The I/O transfer to or from the CompactFlash Memory Card can be either 8 or 16 bits. When a 16-bit accessible port is addressed, the signal -IOIS16 is asserted by the CompactFlash Card. Otherwise, the -IOIS16 signal is de-asserted. When a 16-bit transfer is attempted, and the -IOIS16 signal is not asserted by the CompactFlash Card, the system must generate a pair of 8-bit references to access the word's even byte and odd byte. The CompactFlash Card permits both 8- and 16-bit accesses to all of its I/O addresses, so -IOIS16 is asserted for all addresses to which the CompactFlash Card responds (refer to Table 3-16).

Table 3-16. I/O Function

Function Code	-REG	-CE2	-CE1	A0	-IORD	-IOWR	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte Input Access (8 bits)	L L	H H	L L	L H	L L	H H	High Z High Z	Even-Byte Odd-Byte
Byte Output Access (8 bits)	L L	H H	L L	L H	H H	L L	Do not care Do not care	Even-Byte Odd-Byte
Word Input Access (16 bits)	L	L	L	L	L	H	Odd-Byte	Even-Byte
Word Output Access (16 bits)	L	L	L	L	H	L	Odd-Byte	Even-Byte
I/O Read Inhibit	H	X	X	X	L	H	Do not care	Do not care
I/O Write Inhibit	H	X	X	X	H	L	High Z	High Z
High Byte Input Only (8 bits)	L	L	H	X	L	H	Odd-Byte	High Z
High Byte Output Only (8 bits)	L	L	H	X	H	L	Odd-Byte	Do not care

3.5. Common Memory Transfer Function

The Common Memory transfer to or from the CompactFlash card can be either 8 or 16 bits. The CompactFlash cards permit both 8- and 16-bit accesses to all of its Common addresses (refer to Table 3-17).

Table 3-17. Common Memory Function

Function Code	-REG	-CE2	-CE1	A0	-OE	-WE	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte ReadAccess (8 bits)	H H	H H	L L	L H	L L	H H	High Z High Z	Even-Byte Odd-Byte
Byte Write Access (8 bits)	H H	H H	L L	L H	H H	L L	Do not care Do not care	Even-Byte Odd-Byte
Word Read Access (16 bits)	H	L	L	X	L	H	Odd-Byte	Even-Byte
Word Write Access (16 bits)	H	L	L	X	H	L	Odd-Byte	Even-Byte
Odd Byte Read Only (8 bits)	H	L	H	X	L	H	Odd-Byte	High Z
Odd Byte Write Only (8 bits)	H	L	H	X	H	L	Odd-Byte	Do not care

3.6. True IDE Mode I/O Transfer Function

CompactFlash card can be configured in a True IDE Mode of operation. The card is configured in this mode only when the -OE input signal is grounded by the host when power is applied to the card. In True IDE Mode, the CF Card protocol and configuration are disabled and only I/O operations to the Task File and Data Register are allowed. In addition, No Memory or Attribute Registers are accessible to the host.

NOTE: Removing and reinserting the CompactFlash Memory Card while the host computer's power is on will reconfigure the CompactFlash Card to PC Card ATA mode from the original True IDE Mode. To configure the CompactFlash Card in True IDE Mode, the 50-pin socket must be power cycled with the CompactFlash Card inserted and -OE (output enable) grounded by the host.

Table 3-18 defines the function of the operations for the True IDE Mode.

Table 3-18. IDE Mode I/O Function

Function Code	-CE2	-CE1	A0	-IORD	-IOWR	D15-D8	D7-D0
Invalid Mode	L	L	X	X	X	High Z	High Z
Standby Mode	H	H	X	X	X	High Z	High Z
Task File Write	H	L	1-7h	H	L	Do not care	Data In
Task File Read	H	L	1-7h	L	H	High Z	Data Out
Data Register Write	H	L	0	H	L	Odd-Byte In	Even-Byte In
Data Register Read	H	L	0	L	H	Odd-Byte Out	Even-Byte Out
Control Register Write	L	H	6h	H	L	Do not care	Control In
Alt Status Read	L	H	6h	L	H	High Z	Status Out

4.ATA Drive Register Set Definition and Protocol

CompactFlash Memory Card can be configured as a high performance I/O device through the following ways:

- Standard PC-AT disk I/O address spaces 1F0h-1F7h, 3F6h-3F7h (primary); 170h-177h, 376h-377h (secondary) with IRQ 14 (or other available IRQ).
- Any system decoded 16-byte I/O block using any available IRQ.
- Memory space.

The communication to or from the CompactFlash Memory Card is done using the Task File registers, which provide all the necessary registers for control and status information. The PC Card interface connects peripherals to the host using four register mapping methods. Table 4-19 is a detailed description of these methods.

Table 4-19. I/O Configurations

Standard Configurations				
Config Index	**IO or Memory**	**Address**	**Drive #**	**Description**
0	Memory	0-F, 400-7FF	0	Memory Mapped
1	I/O	XX0-XXF	0	I/O Mapped 16 Contiguous Registers
2	I/O	1F0-1F7, 3F6-3F7	0	Primary I/O Mapped Drive 0
2	I/O	1F0-1F7, 3F6-3F7	1	Primary I/O Mapped Drive 1
3	I/O	170-177, 376-377	0	Secondary I/O Mapped Drive 0
3	I/O	170-177, 376-377	1	Secondary I/O Mapped Drive 1

4.1. I/O Primary and Secondary Address Configurations

Table 4-20. Primary and Secondary I/O Decoding

-REG	A9-A4	A3	A2	A1	A0	-IORD=0	-IOWR=0	Note
0	1F(17)	0	0	0	0	Even RD Data	Even WR Data	1, 2
0	1F(17)	0	0	0	1	Error Register	Features	1
0	1F(17)	0	0	1	0	Sector Count	Sector Count	
0	1F(17)	0	0	1	1	Sector No.	Sector No.	
0	1F(17)	0	1	0	0	Cylinder Low	Cylinder Low	
0	1F(17)	0	1	0	1	Cylinder High	Cylinder High	
0	1F(17)	0	1	1	0	Select Card/Head	Select Card/Head	
0	1F(17)	0	1	1	1	Status	Command	
0	3F(37)	0	1	1	0	Alt Status	Device Control	
0	3F(37)	0	1	1	1	Drive Address	Reserved	

1. Register 0 is accessed with -CE1 low and -CE2 low (and A0 = Do not care) as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte accesses to the offset 0 with -CE1 low and -CE2 high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers that lie at offset 1. When accessed twice as byte register with -CE1 low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access.

2. A byte access to register 0 with -CE1 high and -CE2 low accesses the error (read) or feature (write) register.

4.2. Contiguous I/O Mapped Addressing

When the system decodes a contiguous block of I/O registers to select the CompactFlash Memory Card, the registers are accessed in the block of I/O space decoded by the system in Table 4-21.

Table 4-21. Contiguous I/O Decoding

-REG	A3	A2	A1	A0	Offset	-IORD=0	-IOWR=0	Notes
0	0	0	0	0	0	Even RD Data	Even WR Data	1
0	0	0	0	1	1	Error	Features	2
0	0	0	1	0	2	Sector Count	Sector Count	
0	0	0	1	1	3	Sector No.	Sector No.	
0	0	1	0	0	4	Cylinder Low	Cylinder Low	
0	0	1	0	1	5	Cylinder High	Cylinder High	
0	0	1	1	0	6	Select Card/Head	Select Card/Head	
0	0	1	1	1	7	Status	Command	
0	1	0	0	0	8	Dup Even RD Data	Dup. Even WR Data	2
0	1	0	0	1	9	Dup. Odd RD Data	Dup. Odd WR Data	2
0	1	1	0	1	D	Dup. Error	Dup. Features	2
0	1	1	1	0	E	Alt Status	Device Ctl	
0	1	1	1	1	F	Drive Address	Reserved	

NOTES: 1. Register 0 is accessed with -CE1 low and -CE2 low (and A0 = Do not care) as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte accesses to the offset 0 with -CE1 low and -CE2 high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers that lie at offset 1. When accessed twice as byte register with -CE1 low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access.

A byte access to register 0 with -CE1 high and -CE2 low accesses the error (read) or feature (write) register.

2. Registers at offset 8, 9 and D are non-overlapping duplicates of the registers at offset 0 and 1.
Register 8 is equivalent to register 0, while register 9 accesses the odd byte. Therefore, if the registers are byte accessed in the order 9 then 8 the data will be transferred odd byte then even byte.
Repeated byte accesses to register 8 or 0 will access consecutive (even than odd) bytes from the data buffer. Repeated word accesses to register 8, 9 or 0 will access consecutive words from the data buffer. Repeated byte accesses to register 9 are not supported. However, repeated alternating byte accesses to registers 8 then 9 will access consecutive (even then odd) bytes from the data buffer. Byte accesses to register 9 access only the odd byte of the data.

3. Address lines that are not indicated are ignored by the CompactFlash Memory Card for accessing all the registers in this table.

4.3. Memory Mapped Addressing

When the CompactFlash Memory Card registers are accessed via memory references, the registers appear in the common memory space window: 0-2K bytes as shown in Table 4-22.

Table 4-22. Memory Mapped Decoding

-REG	A10	A9-A4	A3	A2	A1	A0	Offset	-OE=0	-WE=0	Notes
1	0	X	0	0	0	0	0	Even RD Data	Even WR Data	1
1	0	X	0	0	0	1	1	Error	Features	2
1	0	X	0	0	1	0	2	Sector Count	Sector Count	
1	0	X	0	0	1	1	3	Sector No.	Sector No.	
1	0	X	0	1	0	0	4	Cylinder Low	Cylinder Low	
1	0	X	0	1	0	1	5	Cylinder High	Cylinder High	
1	0	X	0	1	1	0	6	Select Card/Head	Select Card/Head	
1	0	X	0	1	1	1	7	Status	Command	
1	0	X	1	0	0	0	8	Dup. Even RD Data	Dup. Even WR Data	2
1	0	X	1	0	0	1	9	Dup. Odd RD Data	Dup. Odd WR Data	2
1	0	X	1	1	0	1	D	Dup. Error	Dup. Features	2
1	0	X	1	1	1	0	E	Alt Status	Device Ctl	
1	0	X	1	1	1	1	F	Drive Address	Reserved	
1	1	X	X	X	X	0	8	Even RD Data	Even WR Data	3
1	1	X	X	X	X	1	9	Odd RD Data	Odd WR Data	3

NOTES: 1. Register 0 is accessed with -CE1 low and -CE2 low as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte accesses to the offset 0 with -CE1 low and -CE2 high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers that lie at offset 1. When accessed twice as byte register with -CE1 low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access.
A byte access to address 0 with -CE1 high and -CE2 low accesses the error (read) or feature (write) register.

2. Registers at offset 8, 9 and D are non-overlapping duplicates of the registers at offset 0 and 1.
Register 8 is equivalent to register 0, while register 9 accesses the odd byte. Therefore, if the registers are byte accessed in the order 9 then 8 the data will be transferred odd byte then even byte.
Repeated byte accesses to register 8 or 0 will access consecutive (even then odd) bytes from the data buffer. Repeated word accesses to register 8, 9 or 0 will access consecutive words from the data buffer. Repeated byte accesses to register 9 are not supported. However, repeated alternating byte accesses to registers 8 then 9 will access consecutive (even then odd) bytes from the data buffer. Byte accesses to register 9 access only the odd byte of the data.

3. Accesses to even addresses between 400h and 7FFh access register 8. Accesses to odd addresses between 400h and 7FFh access register 9. This 1 KByte memory window to the data register is provided so that hosts can perform memory to memory block moves to the data register when the register lies in memory space.
Some hosts, such as the X86 processors, must increment both the source and destination addresses when executing the memory to memory block move instruction. Some PC Card socket adapters also have auto incrementing address logic embedded within them. This address window allows these hosts and adapters to function efficiently.

Note that this entire window accesses the Data Register FIFO and does not allow random access to the data buffer within the CompactFlash Memory Card.

4.4. True IDE Mode Addressing

When the CompactFlash Memory Card is configured in True IDE Mode the I/O decoding is as listed in Table 4-23.

Table 4-23. True IDE Mode I/O Decoding

-CE2	-CE1	A2	A1	A0	-IORD=0	-IOWR=0
1	0	0	0	0	Even RD Data	Even WR Data
1	0	0	0	1	Error Register	Features
1	0	0	1	0	Sector Count	Sector Count
1	0	0	1	1	Sector No.	Sector No.
1	0	1	0	0	Cylinder Low	Cylinder Low
1	0	1	0	1	Cylinder High	Cylinder High
1	0	1	1	0	Select Card/Head	Select Card/Head
1	0	1	1	1	Status	Command
0	1	1	1	0	Alt Status	Device Control
0	1	1	1	1	Drive Address	Reserved

4.5. ATA Registers

NOTE: In accordance with the PCMCIA specification: each of the registers below which is located at an odd offset address may be accessed at its normal address and also the corresponding even address (normal address -1) using data bus lines (D15-D8) when -CE1 is high and -CE2 is low unless -IOIS16 is high (not asserted) and an I/O cycle is being performed.

4.5.1. Data Register (Address—1F0[170];Offset 0, 8, 9)

The Data Register is a 16-bit register, and it is used to transfer data blocks between the CF card data buffer and the Host. This register overlaps the Error Register. Table 4-24 describes the combinations of data register access and is provided to assist in understanding the overlapped Data Register and Error/Feature Register rather than to attempt to define general PCMCIA word and byte access modes and operations. See the PCMCIA PC Card Standard Release 2.0 for definitions of the Card Accessing Modes for I/O and Memory cycles.

NOTE: Because of the overlapped registers, access to the 1F1, 171 or offset 1 are not defined for word (-CE2 = 0 and -CE1 = 0) operations. Accesses to these locations are treated as accesses to the Word Data Register. The duplicated registers at offsets 8, 9 and Dh have no restrictions on the operations that can be performed by the socket.

Table 4-24. Data Register

Data Register	CE2-	CE1-	A0	Offset	Data Bus
Word Data Register	0	0	X	0,8,9	D15-D0
Even Data Register	1	0	0	0,8	D7-D0
Odd Data Register	1	0	1	9	D7-D0
Odd Data Register	0	1	X	8,9	D15-D8
Error/Feature Register	1	0	1	1, Dh	D7-D0
Error/Feature Register	0	1	X	1	D15-D8

Data Register	CE2-	CE1-	A0	Offset	Data Bus
Error/Feature Register	0	0	X	Dh	D15-D8

4.5.2. Error Register (Address—1F1[171]; Offset 1, 0Dh Read Only)

This register contains additional information about the source of an error when an error is indicated in bit 0 of the Status register. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
BBK	UNC	0	IDNF	0	ABRT	0	AMNF

This register is also accessed on data bits D15-D8 during a write operation to offset 0 with -CE2 low and -CE1 high.

Bit 7 (BBK) This bit is set when a Bad Block is detected.
Bit 6 (UNC) This bit is set when an Uncorrectable Error is encountered.
Bit 5 This bit is 0.
Bit 4 (IDNF) The requested sector ID is in error or cannot be found.
Bit 3 This bit is 0.
Bit 2 (Abort) This bit is set if the command has been aborted because of a status condition: (Not Ready, Write Fault, etc.) or when an invalid command has been issued.
Bit 1 This bit is 0.
Bit 0 (AMNF) This bit is set in case of a general error.

4.5.3. Feature Register (Address—1F1[171]; Offset 1, 0Dh Write Only

This register provides information regarding features of the CF card that the host can utilize. This register is also accessed on data bits D15-D8 during a write operation to Offset 0 with -CE2 low and -CE1 high (except in True IDE Mode operation).

4.5.4. Sector Count Register (Address—1F2[172]; Offset 2)

This register contains the number of sectors of data requested to be transferred on a read or write operation between the host and the CompactFlash Memory Card. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at command completion. If not successfully completed, the register contains the number of sectors that need to be transferred in order to complete the request.

4.5.5. Sector Number (LBA 7-0) Register (Address—1F3[173]; Offset 3)

This register contains the starting sector number or bits 7-0 of the Logical Block Address (LBA) for any CompactFlash Memory Card data access for the subsequent command.

4.5.6. Cylinder Low (LBA 15-8) Register (Address—1F4[174]; Offset 4)

This register contains the low order 8 bits of the starting cylinder address or bits 15-8 of the Logical Block Address.

4.5.7. Cylinder High (LBA 23-16) Register (Address—1F5[175]; Offset 5)

This register contains the high order bits of the starting cylinder address or bits 23-16 of the Logical Block Address.

4.5.8. Drive/Head (LBA 27-24) Register (Address 1F6[176]; Offset 6)

The Drive/Head register is used to select the drive and head. It is also used to select LBA addressing instead of cylinder/head/sector addressing. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
1	LBA	1	DRV	HS3	HS2	HS1	HS0

Bit 7 This bit is set to 1.
Bit 6 LBA is a flag to select either Cylinder/Head/Sector (CHS) or Logical Block Address Mode (LBA). When LBA=0, Cylinder/Head/Sector mode is selected. When LBA=1, Logical Block Address is selected. In Logical Block Mode, the Logical Block Address is interpreted as follows:
LBA07-LBA00: Sector Number Register D7-D0.
LBA15-LBA08: Cylinder Low Register D7-D0.
LBA23-LBA16: Cylinder High Register D7-D0.
LBA27-LBA24: Drive/Head Register bits HS3-HS0.
Bit 5 This bit is set to 1.
Bit 4 (DRV) This bit will have the following meaning. DRV is the drive number. When DRV=0, drive (card) 0 is selected When DRV=1, drive (card) 1 is selected. In PCMCIA Mode operation, Card 0 or 1 is selected using the copy field of the PC Card Socket and Copy configuration register.
Bit 3 (HS3) When operating in the Cylinder, Head, Sector mode, this is bit 3 of the head number. It is Bit 27 in the Logical Block Address mode.
Bit 2 (HS2) When operating in the Cylinder, Head, Sector mode, this is bit 2 of the head number. It is Bit 26 in the Logical Block Address mode.
Bit 1 (HS1) When operating in the Cylinder, Head, Sector mode, this is bit 1 of the head number. It is Bit 25 in the Logical Block Address mode.
Bit 0 (HS0) When operating in the Cylinder, Head, Sector mode, this is bit 0 of the head number. It is Bit 24 in the Logical Block Address mode.

4.5.9. Status and Alternate Status Registers (Address 1F7[177] and 3F6[376]; Offsets 7 and Eh)

These registers return the status when read by the host. Reading the Status register does clear a pending interrupt while reading the Auxiliary Status register does not. The meaning of the status bits are described as follows:

D7	D6	D5	D4	D3	D2	D1	D0
BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR

Bit 7 (BUSY) The busy bit is set when the drive has access to the command buffer and registers and the host is locked out from accessing the command register and buffer. No other bits in this register are valid when this bit is set to a 1.

Bit 6 (RDY) RDY indicates whether the device is capable of performing operations requested by the host. This bit is cleared at power up and remains cleared until the drive is ready to accept a command.

Bit 5 (DWF) This bit, if set, indicates a write fault has occurred.

Bit 4 (DSC) This bit is set when the drive is ready.

Bit 3 (DRQ) The Data Request is set when the drive requires that information be transferred either to or from the host through the Data register.

Bit 2 (CORR) This bit is set when a Correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector read operation.

Bit 1 (IDX) This bit is always set to 0.

Bit 0 (ERR) This bit is set when the previous command has ended in some type of error. The bits in the Error register contain additional information describing the error.

4.5.10. Device Control Register (Address—3F6[376]; Offset Eh)

This register is used to control the card interrupt request and to issue an ATA soft reset to the card. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	1	SW Rst	-IEn	0

Bit 7 This bit is an X (Do not care).

Bit 6 This bit is an X (Do not care).

Bit 5 This bit is an X (Do not care).

Bit 4 This bit is an X (Do not care).

Bit 3 This bit is ignored by the card.

Bit 2 (SW Rst) This bit is set to 1 in order to force the card to perform an AT Disk controller Soft Reset operation. This does not change the PC Card Configuration Registers (4.3.2 to 4.3.5) as a hardware Reset does. The card remains in Reset until this bit is reset to '0'.

Bit 1 (-IEn) The Interrupt Enable bit enables interrupts when the bit is 0. When the bit is 1, interrupts from the card are disabled. This bit also controls the Int bit in the Configuration and Status Register. This bit is set to 0 at power on and Reset.

Bit 0 This bit is ignored by the card.

4.5.11. Card (Drive) Address Register (Address 3F7[377]; Offset Fh)

This register is provided for compatibility with the AT disk drive interface. It is recommended that this register not be mapped into the host's I/O space because of potential conflicts on Bit 7. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
X	-WTG	-HS3	-HS2	-HS1	-HS0	-nDS1	-nDS0

Bit 7 This bit is unknown.
Implementation Note:
Conflicts may occur on the host data bus when this bit is provided by a Floppy Disk Controller operating at the same addresses as the drive. Following are some possible solutions to this problem for the PC Card implementation:

1. Locate the drive at a non-conflicting address (i.e., Secondary address (377) or in an independently decoded Address Space when a Floppy Disk Controller is located at the Primary addresses).
2. Do not install a Floppy and a drive product in the system at the same time.
3. Implement a socket adapter that can be programmed to (conditionally) tri-state D7 of I/0 address 3F7/377 when a drive is installed and conversely to tri-state D6-D0 of I/O address 3F7/377 when a floppy controller is installed.
4. Do not use the drive's Drive Address register. This may be accomplished by either a) If possible, program the host adapter to enable only I/O addresses 1F0-1F7, 3F6 (or 170-177, 176) to the drive or b) if provided use an additional Primary/Secondary configuration in the drive that does not respond to accesses to I/O locations 3F7 and 377. With either of these implementations, the host software must not attempt to use information in the Drive Address Register.

Bit 6 (-WTG) This bit is 0 when a write operation is in progress, otherwise, it is 1.
Bit 5 (-HS3) This bit is the negation of bit 3 in the Drive/Head register.
Bit 4 (-HS2) This bit is the negation of bit 2 in the Drive/Head register.
Bit 3 (-HS1) This bit is the negation of bit 1 in the Drive/Head register.
Bit 2 (-HS0) This bit is the negation of bit 0 in the Drive/Head register.
Bit 1 (-nDS1) This bit is 0 when drive 1 is active and selected.
Bit 0 (-nDS0) This bit is 0 when the drive 0 is active and selected.

4.6. S.M.A.R.T. Support

Cactus Technologies® Industrial MLC CF cards support extended attributes reporting through the S.M.A.R.T Feature Set. The following subcommands are supported when programmed into the Feature Register:

Value	Command	Value	Command
D0h	Read Data	D4h	Execute Off-line Immediate
D1h	Read Attributes Threshold	D8h	Enable S.M.A.R.T Operations
D2h	Enable/Disable Autosave	D9h	Disable S.M.A.R.T Operations
D3h	Save Attribute Values	DAh	Return Status

4.6.1. S.M.A.R.T Data Structure

The Read Data command returns 512 bytes of data in the following format:

Byte	F/V	Description
0-1	X	Revision code
2-361	X	Vendor Specific
362	V	Off-line data collection status
363	X	Self-test execution status byte
364-365	V	Total time in seconds to complete off-line data collection activity
366	X	Vendor specific

Byte	F/V	Description
367	F	Off-line data collection capabilities
368-369	F	S.M.A.R.T capabilities
370	F	Error logging capabilities: bit 0: 1 – device error logging supported bits1-7: reserved
371	X	Vendor specific
372	F	Short self-test routine recommended polling time (in minutes)
373	F	Extended self-test routine recommended polling time (in minutes)
374	F	Conveyance self-test routine recommended polling time (in minutes)
375-385	R	Reserved
386-395	F	Firmware Version/Date Code
396-399	R	Reserved
400-406	F	'SMI2232EN'
407-511	R	Reserved

Notes:

1. F = content is fixed
2. V = content is variable
3. X = content is vendor specific
4. R = content is reserved

4.6.2. S.M.A.R.T Attributes

The attributes returned in bytes 2 – 361 of the Read Data command are listed below. Each attribute occupies 12 byte of data. Bytes 1-2 are status flags, bytes 3-4 are reserved bytes and byte 11 is checksum; these bytes are not shown in the table below:

Attribute ID	Attribute values						Attribute Name
(byte 0)	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9	Byte 10	
01h	LSB	MSB	00	00	00	00	Read error rate
05h	LSB	MSB	00	00	00	00	Reallocated sector count
0Ch	LSB	MSB	00	00	00	00	Power cycle count
A1h	LSB	MSB	00	00	00	00	# of valid spare blocks
A2h	LSB	MSB	00	00	00	00	# of child pair

A3h	LSB	MSB	00	00	00	00	# of initial invalid blocks
A4h	LSB			MSB	00	00	# of total erase count
A5h	LSB			MSB	00	00	Max. Erase count
A6h	LSB			MSB	00	00	Min. Erase count
A7h	LSB			MSB	00	00	Avg. Erase count
C0h	LSB			MSB	00	00	Power-off retract count
C7h	LSB	MSB	00	00	00	00	UDMA CRC error count
F1h	LSB					MSB	Total LBAs written (in units of 32MB)
F2h	LSB					MSB	Total LBAs read (in units of 32MB)

Appendix A.Ordering Information

Model KCXYZ-240

Where:X is card capacities:

4G ---------- 4GB
8G ---------- 8GB
16G ---------- 16GB
32G ---------- 32GB
64G ---------- 64GB
128G ---------- 128GB

Where Y is card configuration
R ---------- Removable card
F ---------- Fixed card

Where Z is temperature grade:
blank ---------- standard temp.
I ---------- extended temp.

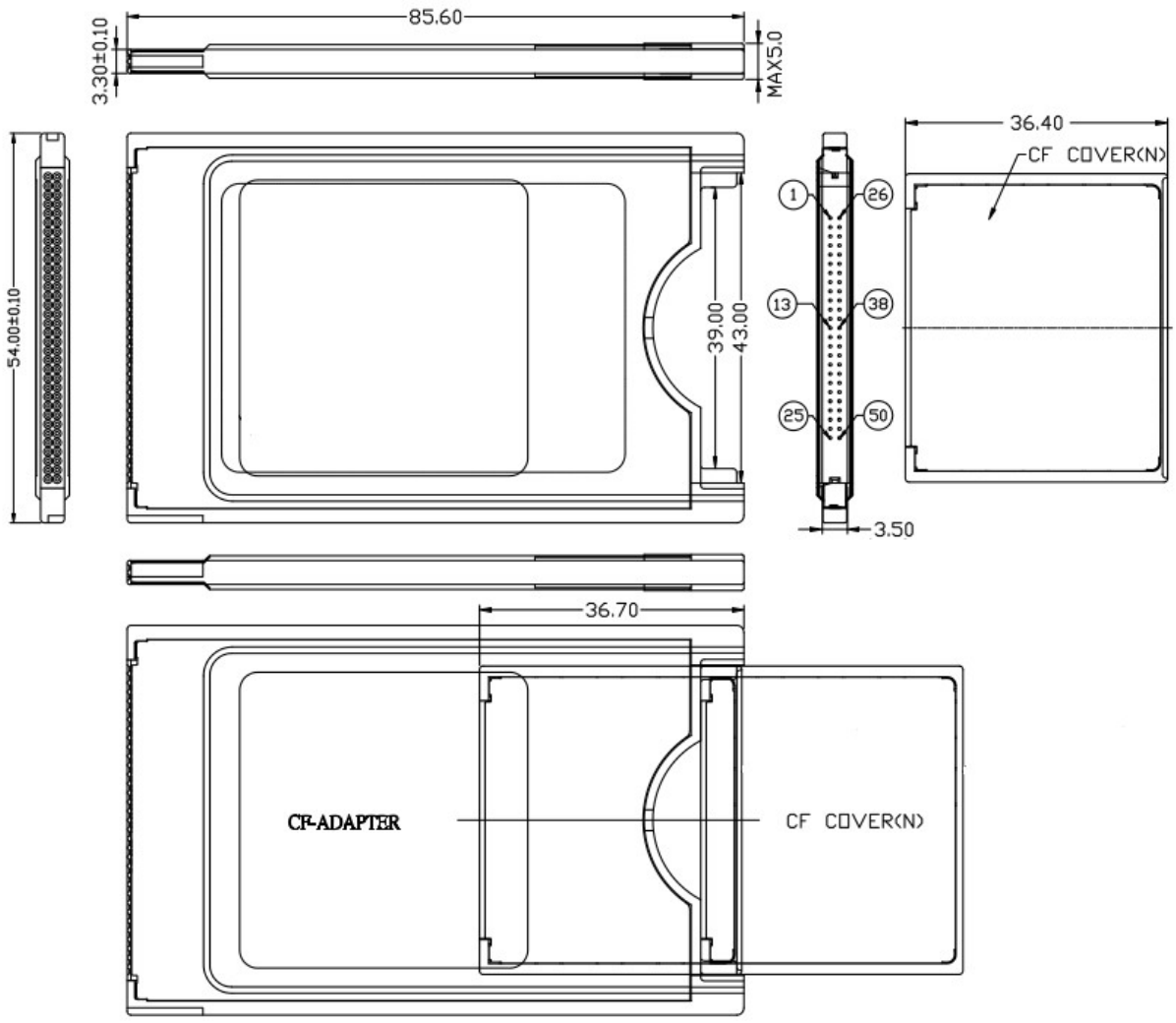
If your systems cannot accept removable CF card (R), please order Fixed CF card (F).

Example:

(1) 4GB CF Removable ---------- KC4GR-240
(2) 4GB CF Fixed ---------- KC4GF-240
(3) 4GB CF Removable, extended temp. ---------- KC4GRI-240

Appendix A.CF To PC Card Adapter Information

For customers who would like to use the Cactus CompactFlash cards in their existing PC Card sockets, we offer a CF to PC Card adapter. The physical dimensions of this adapter are as shown below:



To order this adapter, please use the following product code:

KADPT-CF02

Appendix B.Technical Support Services

Email: tech@cactus-tech.com

Appendix C.Cactus Worldwide Sales Offices

Email: sales@cactus-tech.com

US Office:

Cactus USA
3112 Windsor Road , Suite A356
Austin, Texas 78703
Tel: (512) 775 0746
Email: americas@cactus-tech.com

Appendix D.Limited Warranty

I. WARRANTY STATEMENT

Cactus Technologies® warrants its Industrial MLC Grade products only to be free of any defects in materials or workmanship that would prevent them from functioning properly for two years from the date of purchase or when rated TBW is exceeded, whichever occurs first. This express warranty is extended by Cactus Technologies Limited

II. GENERAL PROVISIONS

This warranty sets forth the full extent of Cactus Technologies® responsibilities regarding the Cactus Technologies® Industrial MLC Grade Flash Storage Products. Cactus Technologies® , at its sole option, will repair, replace or refund the purchase price of the defective product. Cactus Technologies® guarantees our products meet all specifications detailed in our product manuals. Although Cactus Technologies® products are designed to withstand harsh environments and have the highest specifications in the industry, they are not warranted to never have failure and Cactus Technologies® does not warranty against incidental or consequential damages. Accordingly, in any use of products in life support systems or other applications where failure could cause injury or loss of life, the products should only be incorporated in systems designed with appropriate redundancy, fault tolerant or backup features.

III. WHAT THIS WARRANTY COVERS

For products found to be defective, Cactus Technologies® will have the option of repairing or replacing the defective product, if the following conditions are met:

A. The defective product is returned to Cactus Technologies® for failure analysis as soon as possible after the failure occurs.

B. An incident card filled out by the user, explaining the conditions of usage and the nature of the failure, accompanies each returned defective product.

C. No evidence is found of abuse or operation of products not in accordance with the published specifications, or of exceeding storage or maximum ratings or operating conditions.

All failing products returned to Cactus Technologies® under the provisions of this limited warranty shall be tested to the product's functional and performance specifications. Upon confirmation of failure, each product will be analyzed, by whatever means necessary, to determine the root cause of failure. If the root cause of failure is found to be not covered by the above provisions, then the product will be returned to the customer with a report indicating why the failure was not covered under the warranty.

This warranty does not cover defects, malfunctions, performance failures or damages to the unit resulting from use in other than its normal and customary manner, misuse, accident or neglect; or improper alterations or repairs.

Cactus Technologies® reserves the right to repair or replace, at its discretion, any product returned by its customers, even if such product is not covered under warranty, but is under no obligation to do so.

IV.RECEIVING WARRANTY SERVICE

According to Cactus Technologies® warranty procedure, defective product should be returned only with prior authorization from Cactus Technologies Limited Please contact Cactus Technologies® Customer Service department with the following information: product model number and description, nature of defect, conditions of use, proof of purchase and purchase date. If approved, Cactus Technologies will issue a Return Material Authorization or Product Repair Authorization number and shipping information.