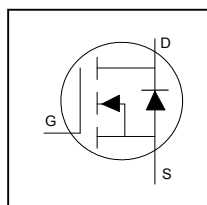


HEXFET® Power MOSFET

**Application**

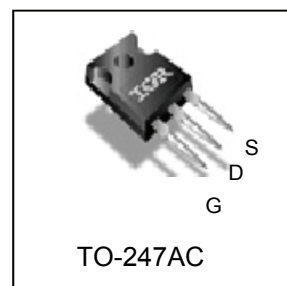
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits



<b>V<sub>DSS</sub></b>	<b>200V</b>
<b>R<sub>DS(on)</sub> typ.</b>	<b>17mΩ</b>
	<b>max</b>
<b>I<sub>D</sub></b>	<b>75A</b>

**Benefits**

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free, RoHS Compliant



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFP4127PbF	TO-247AC	Tube	25	IRFP4127PbF

	Parameter	Max.	Units
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	75	A
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	53	
I <sub>DM</sub>	Pulsed Drain Current ①	300	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Maximum Power Dissipation	341	W
	Linear Derating Factor	2.3	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery dv/dt③	57	V/ns
T <sub>J</sub> T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting Torque, 6-32 or M3 Screw	10 lbf·in (1.1 N·m)	

**Avalanche Characteristics**

E <sub>AS</sub> (Thermally limited)	Single Pulse Avalanche Energy ②	244	mJ
-------------------------------------	---------------------------------	-----	----

**Thermal Resistance**

	Parameter	Typ.	Max.	Units
R <sub>θJC</sub>	Junction-to-Case ④	—	0.4	°C/W
R <sub>θCS</sub>	Case-to-Sink, Flat Greased Surface	0.24	—	
R <sub>θJA</sub>	Junction-to-Ambient ⑦⑧	—	40	

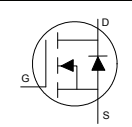
**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	200	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.23	—	V/°C	Reference to 25°C, I <sub>D</sub> = 5mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	17	21	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 44A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	3.0	—	5.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	20	μA	V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 200V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V
R <sub>G</sub>	Gate Resistance	—	3.0	—	Ω	

**Dynamic Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)**

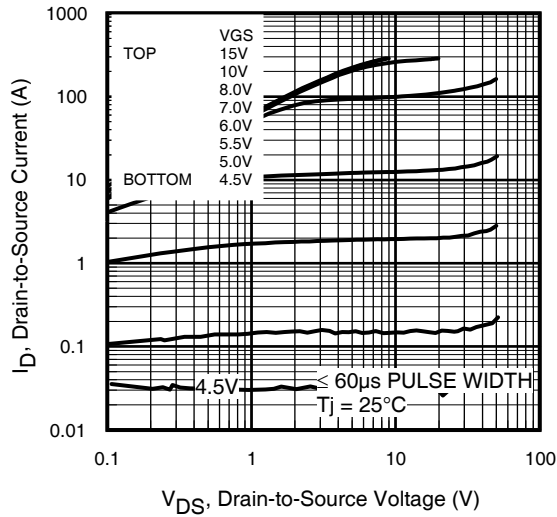
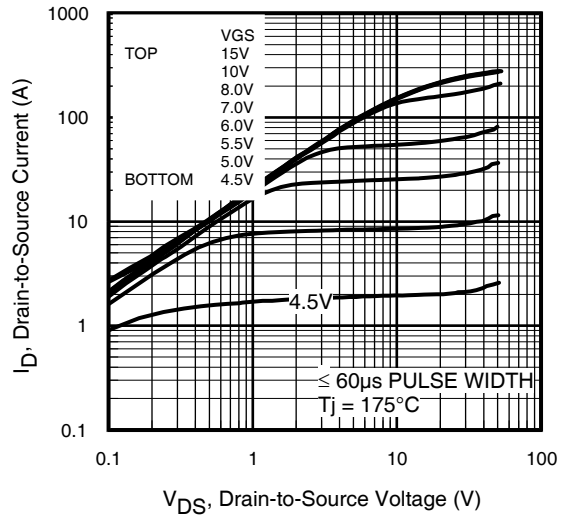
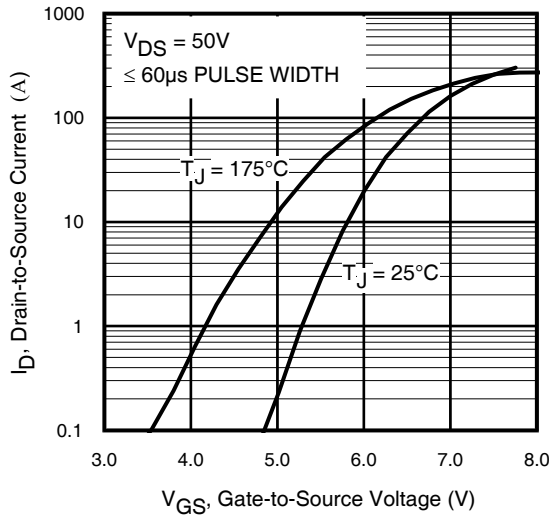
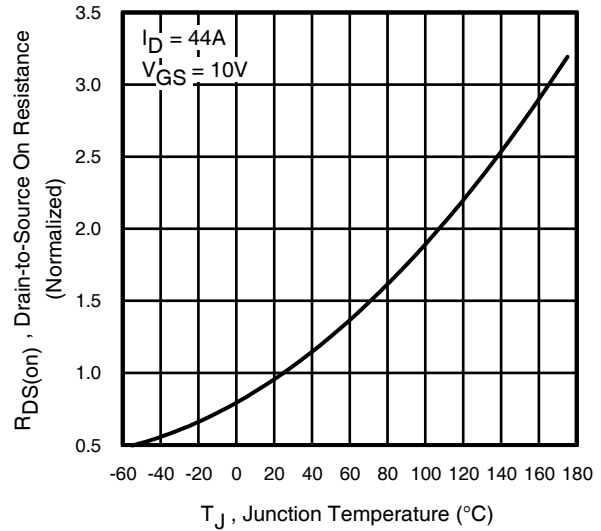
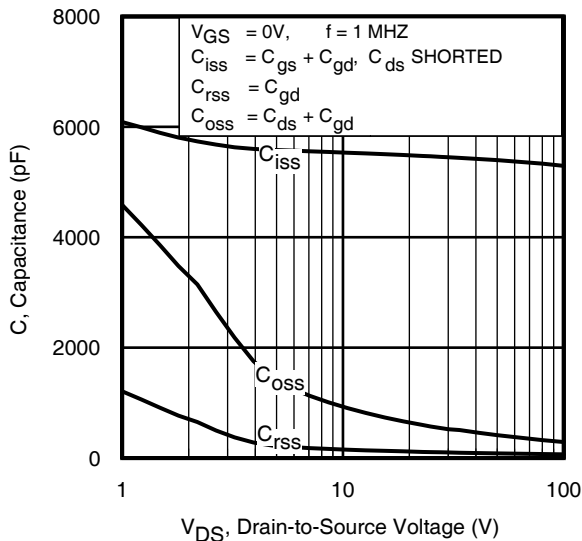
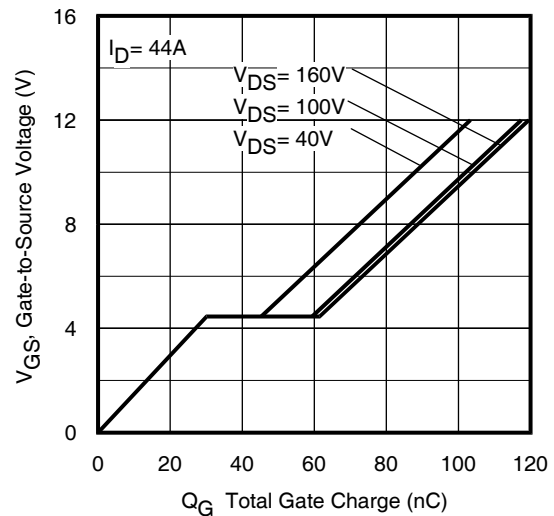
g <sub>fs</sub>	Forward Transconductance	45	—	—	S	V <sub>DS</sub> = 50V, I <sub>D</sub> = 44A
Q <sub>g</sub>	Total Gate Charge	—	100	150	nC	I <sub>D</sub> = 44A
Q <sub>gs</sub>	Gate-to-Source Charge	—	30	—		V <sub>DS</sub> = 100V
Q <sub>gd</sub>	Gate-to-Drain Charge	—	31	—		V <sub>GS</sub> = 10V
Q <sub>sync</sub>	Total Gate Charge Sync. (Q <sub>g</sub> - Q <sub>gd</sub> )	—	69	—		I <sub>D</sub> = 44A, V <sub>DS</sub> = 0V, V <sub>GS</sub> = 10V
t <sub>d(on)</sub>	Turn-On Delay Time	—	17	—	ns	V <sub>DD</sub> = 100V
t <sub>r</sub>	Rise Time	—	18	—		I <sub>D</sub> = 44A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	56	—		R <sub>G</sub> = 2.7Ω
t <sub>f</sub>	Fall Time	—	22	—		V <sub>GS</sub> = 10V
C <sub>iss</sub>	Input Capacitance	—	5380	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	410	—		V <sub>DS</sub> = 50V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	86	—		f = 1.0MHz
C <sub>oss eff.(ER)</sub>	Effective Output Capacitance (Energy Related)	—	360	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 160V <sup>⑥</sup>
C <sub>oss eff.(TR)</sub>	Output Capacitance (Time Related)	—	590	—		See Fig.11
						V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 160V <sup>⑤</sup>

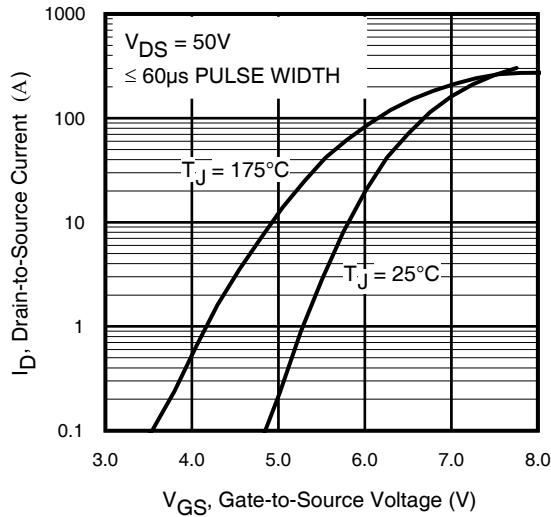
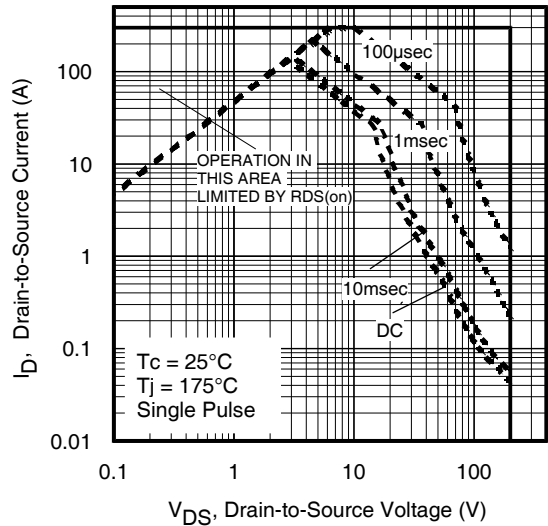
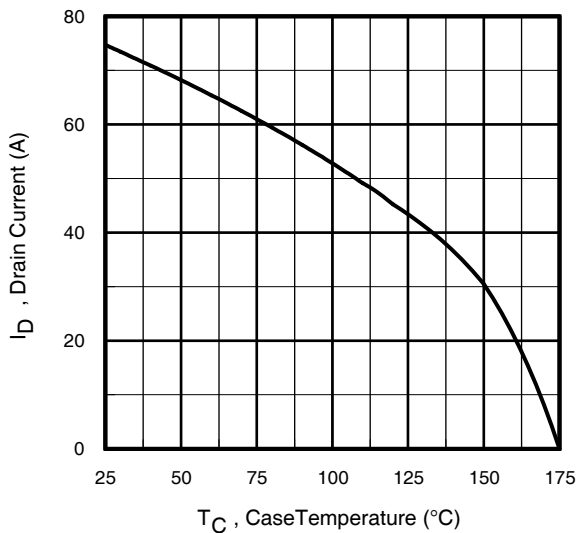
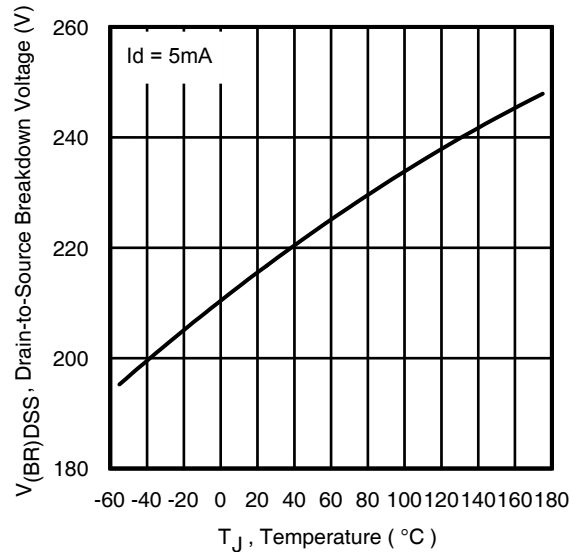
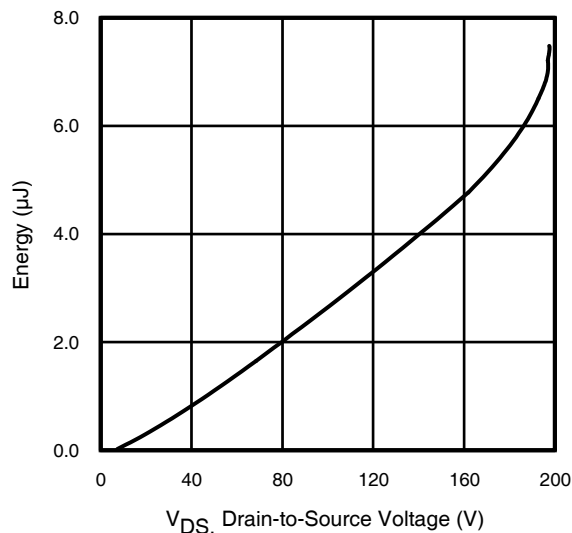
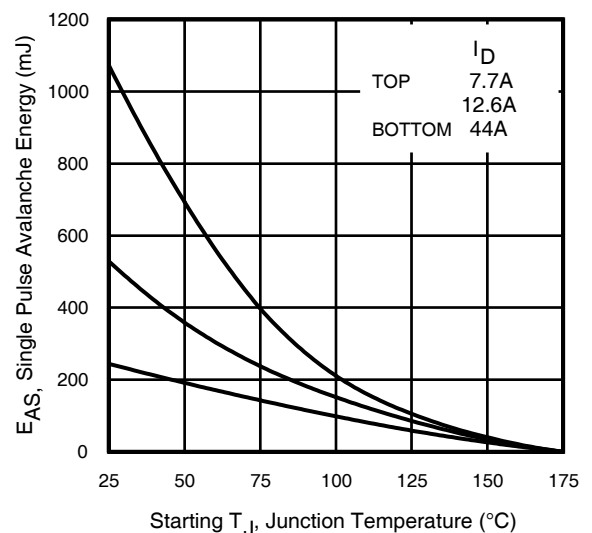
**Diode Characteristics**

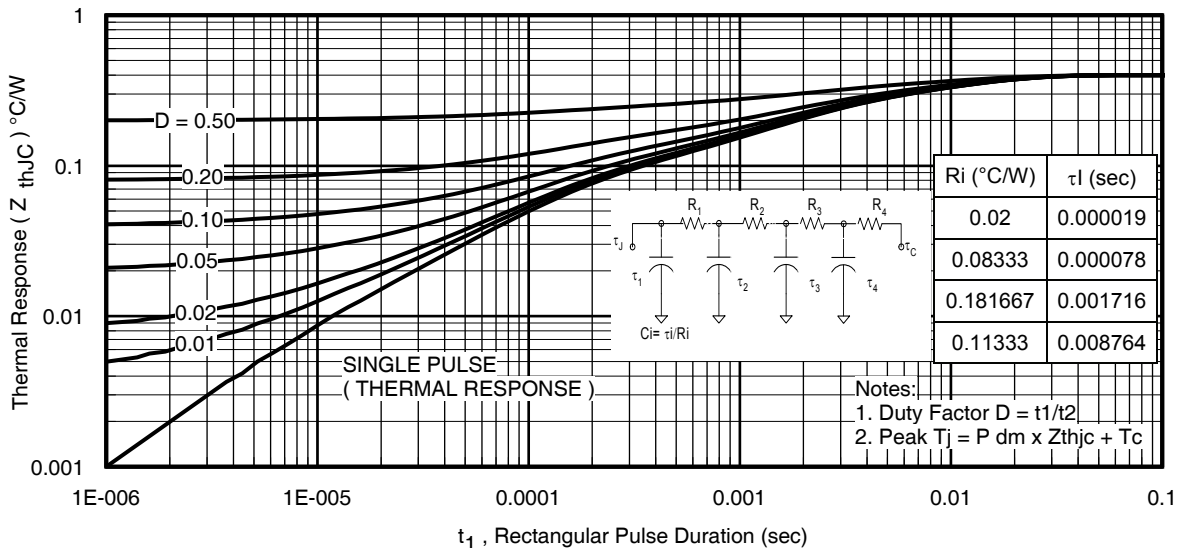
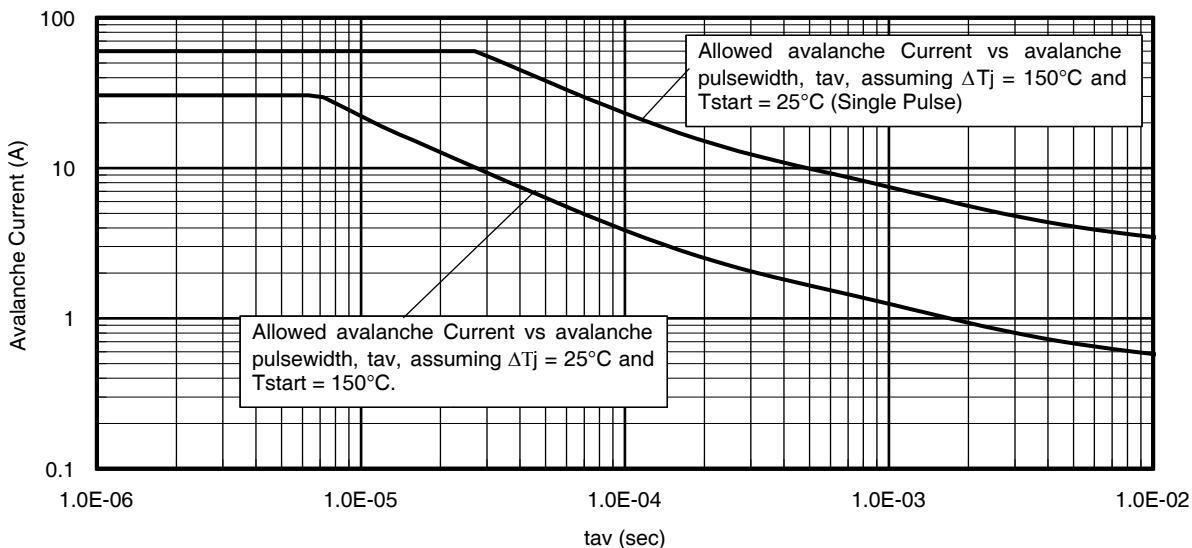
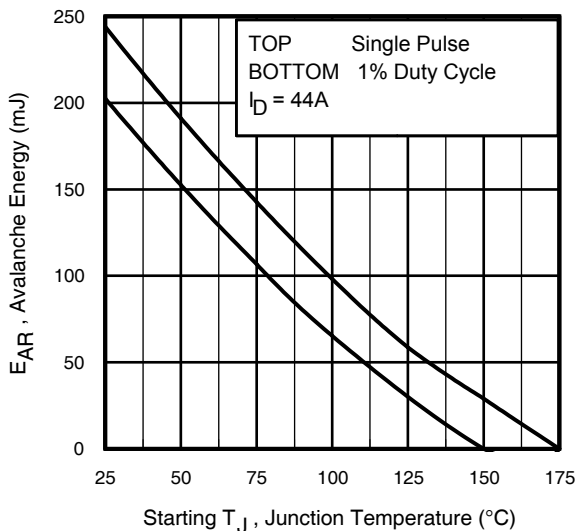
	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode) ①	—	—	75	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	300		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 44A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	136	—	ns	T <sub>J</sub> = 25°C V <sub>DD</sub> = 100V
		—	139	—		T <sub>J</sub> = 125°C I <sub>F</sub> = 44A,
Q <sub>rr</sub>	Reverse Recovery Charge	—	458	—	nC	T <sub>J</sub> = 25°C di/dt = 100A/μs ④
		—	688	—		T <sub>J</sub> = 125°C
I <sub>RRM</sub>	Reverse Recovery Current	—	8.3	—	A	T <sub>J</sub> = 25°C

**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Recommended max EAS limit, starting T<sub>J</sub> = 25°C, L = 0.25mH, R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 44A, V<sub>GS</sub> = 10V.
- ③ I<sub>SD</sub> ≤ 44A, di/dt ≤ 760A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>J</sub> ≤ 175°C.
- ④ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑤ C<sub>oss eff. (TR)</sub> is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- ⑥ C<sub>oss eff. (ER)</sub> is a fixed capacitance that gives the same energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994
- ⑧ R<sub>θ</sub> is measured at T<sub>J</sub> approximately 90°C


**Fig 1. Typical Output Characteristics**

**Fig 2. Typical Output Characteristics**

**Fig 3. Typical Transfer Characteristics**

**Fig 4. Normalized On-Resistance vs. Temperature**

**Fig 5. Typical Capacitance vs. Drain-to-Source Voltage**

**Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage**


**Fig 7.** Typical Source-Drain Diode Forward Voltage

**Fig 8.** Maximum Safe Operating Area

**Fig 9.** Maximum Drain Current vs. Case Temperature

**Fig 10.** Drain-to-Source Breakdown Voltage

**Fig 11.** Typical  $C_{oss}$  Stored Energy

**Fig 12.** Maximum Avalanche Energy vs. Drain Current


**Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case**

**Fig 14. Typical Avalanche Current vs. Pulse Width**

**Notes on Repetitive Avalanche Curves, Figures 14, 15:  
 (For further info, see AN-1005 at www.irf.com)**

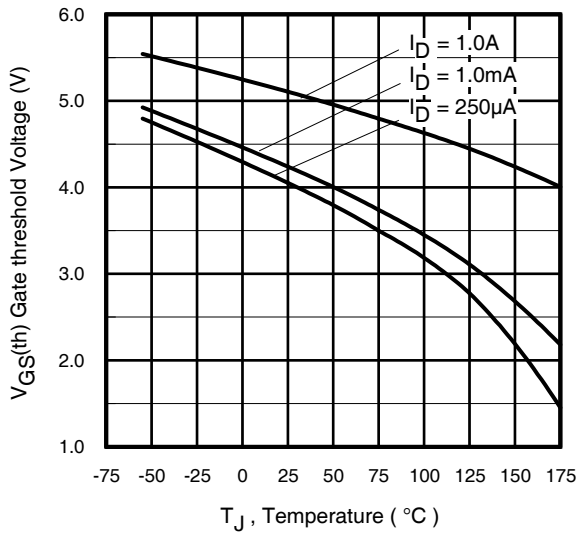
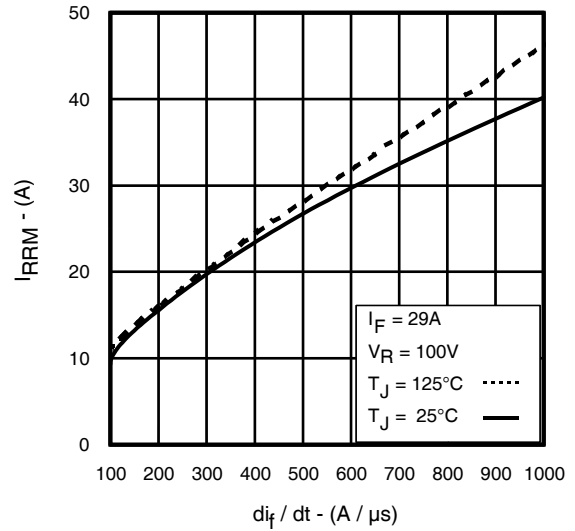
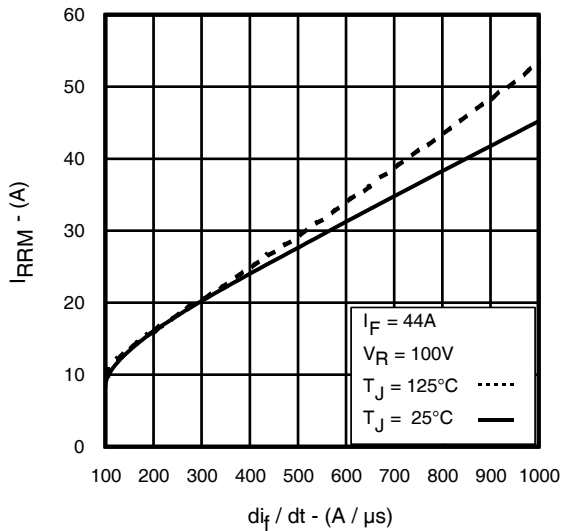
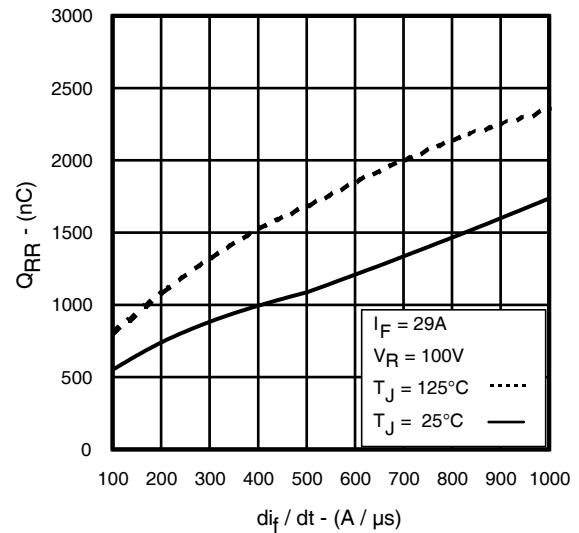
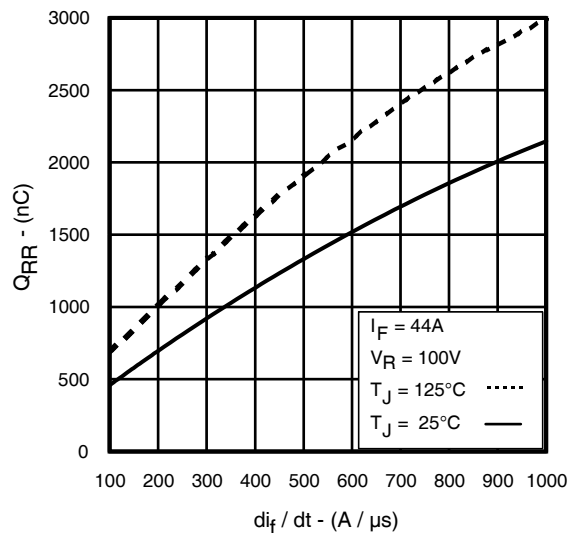
1. Avalanche failures assumption:  
 Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{Imax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{Imax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Fig 22a, 22b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{AV}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{Imax}$  (assumed as 25°C in Fig 14, 15).  
 $t_{AV}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{AV} \cdot f$   
 $Z_{thJC}(D, t_{AV})$  = Transient thermal resistance, see Fig 13.

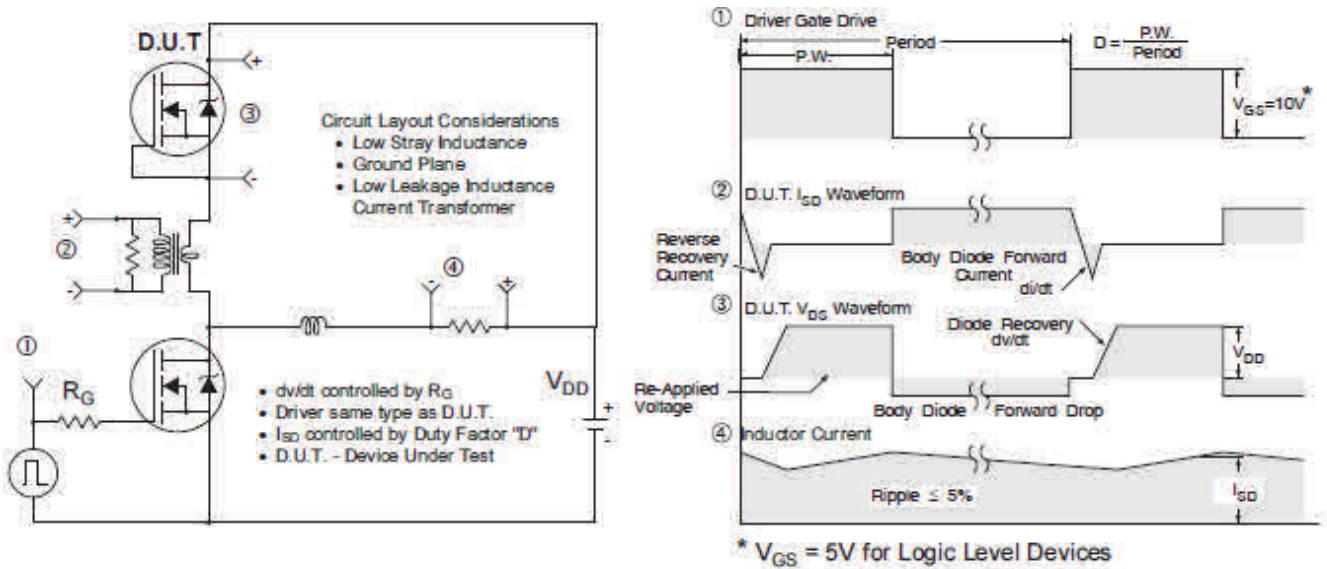
$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{AV}) \cdot \Delta T / Z_{thJC}$$

$$I_{AV} = 2\Delta T / [1.3 \cdot BV \cdot Z_{thJC}]$$

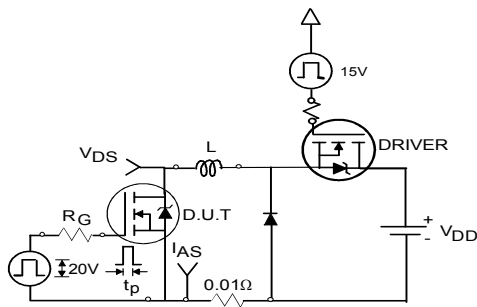
$$E_{AS(AV)} = P_{D(ave)} \cdot t_{AV}$$

**Fig 15. Maximum Avalanche Energy vs. Temperature**

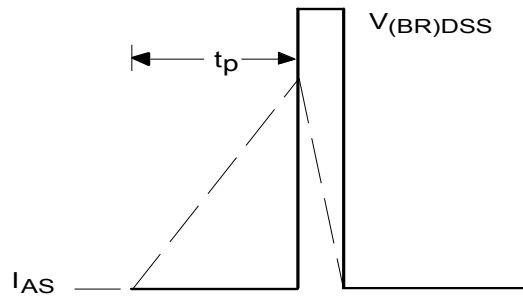

**Fig 16.** Threshold Voltage vs. Temperature

**Fig 17.** Typical Recovery Current vs. dif/dt

**Fig 18.** Typical Recovery Current vs. dif/dt

**Fig 19.** Typical Stored Charge vs. dif/dt

**Fig 20.** Typical Stored Charge vs. dif/dt



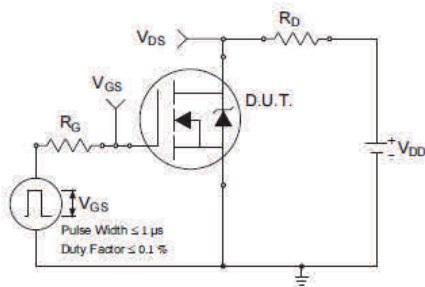
**Fig 21.** Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs



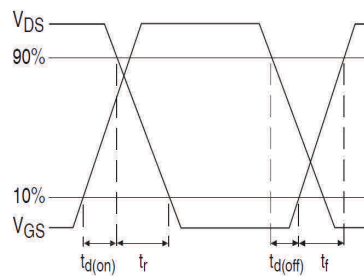
**Fig 22a.** Unclamped Inductive Test Circuit



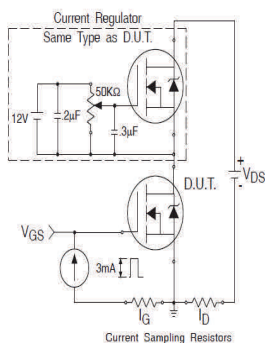
**Fig 22b.** Unclamped Inductive Waveforms



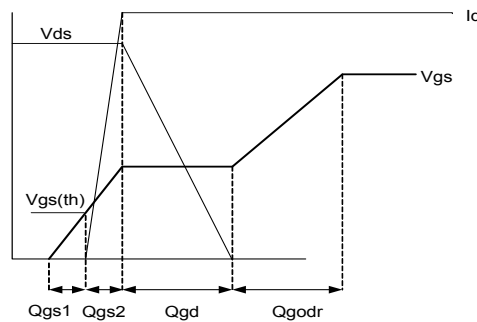
**Fig 23a.** Switching Time Test Circuit



**Fig 23b.** Switching Time Waveforms



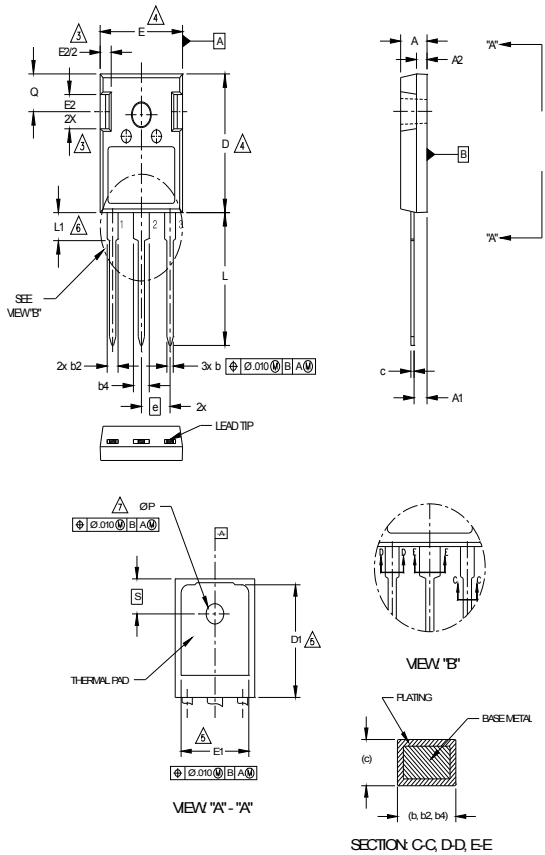
**Fig 24a.** Gate Charge Test Circuit



**Fig 24b.** Gate Charge Waveform

## TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.190	.204	4.83	5.20	4 5 4
A1	.090	.100	2.29	2.54	
A2	.075	.085	1.91	2.16	
b	.042	.052	1.07	1.33	
b2	.075	.094	1.91	2.41	
b4	.113	.133	2.87	3.38	
c	.022	.026	0.55	0.68	
D	.819	.830	20.80	21.10	
D1	.640	.694	16.25	17.65	
E	.620	.635	15.75	16.13	
E1	.512	.570	13.00	14.50	4 5 4
E2	.145	.196	3.68	5.00	
e	.215 Typical		5.45 Typical		
L	.780	.800	19.80	20.32	
L1	.161	.173	4.10	4.40	
ø P	.138	.143	3.51	3.65	
Q	.216	.236	5.49	6.00	
S	.238	.248	6.04	6.30	

**LEAD ASSIGNMENTS**
**HEXFET**

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

**IGBTs, CoPACK**

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

**DIODES**

- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE

**NOTES:**

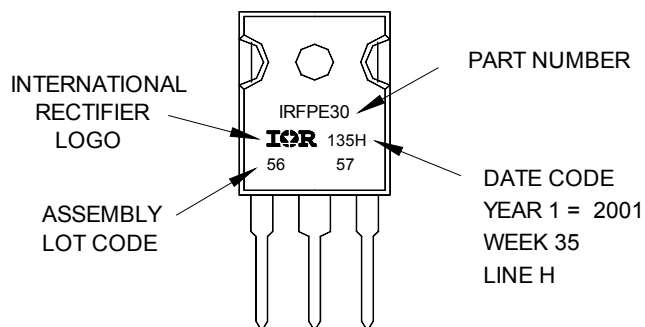
- 1 DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
- 2 DIMENSIONS ARE SHOWN IN INCHES AND MILLIMETERS.
- 3 CONTOUR OF SLOT OPTIONAL.
- 4 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 5 THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
- 6 LEAD FINISH UNCONTROLLED IN L1.
- 7 ø P TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.

## TO-247AC Part Marking Information

Notes: This part marking information applies to devices produced after 02/26/2001

EXAMPLE: THIS IS AN IRFPE30  
WITH ASSEMBLY  
LOT CODE 5657  
ASSEMBLED ON WW 35, 2001  
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position  
indicates "Lead-Free"



TO-247AC package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>



**Qualification Information<sup>†</sup>**

<b>Qualification Level</b>	Industrial (per JEDEC JESD47F) <sup>††</sup>	
<b>Moisture Sensitivity Level</b>	TO-247AC	N/A
<b>RoHS Compliant</b>	Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability/>

†† Applicable version of JEDEC standard at the time of product release.

Data and specifications subject to change without notice.

International  
 Rectifier

**IR WORLD HEADQUARTERS:** 101N Sepulveda., El Segundo, California 90245, USA Tel: (310) 252-7105

TAC Fax: (310) 252-7903

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