

HEF4027B

Dual JK flip-flop

Rev. 11 — 7 December 2021

Product data sheet

1. General description

The HEF4027B is a dual positive-edge triggered JK flip-flop featuring independent set direct (nSD), clear direct (nCD), clock inputs (nCP) and complementary outputs (nQ and n \bar{Q}). Data is accepted when nCP is LOW, and transferred to the output on the positive-going edge of the clock. The asynchronous clear-direct (nCD) and set-direct (nSD) are independent and override the nJ, nK, and nCP inputs. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{DD} .

2. Features and benefits

- Wide supply voltage range from 3.0 V to 15.0 V
- CMOS low power dissipation
- High noise immunity
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Complies with JEDEC standard JESD 13-B
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-B exceeds 200 V
- Specified from -40 °C to +85 °C

3. Applications

- Registers
- Counters
- Control circuits

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
HEF4027BT	-40 °C to +85 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

5. Functional diagram

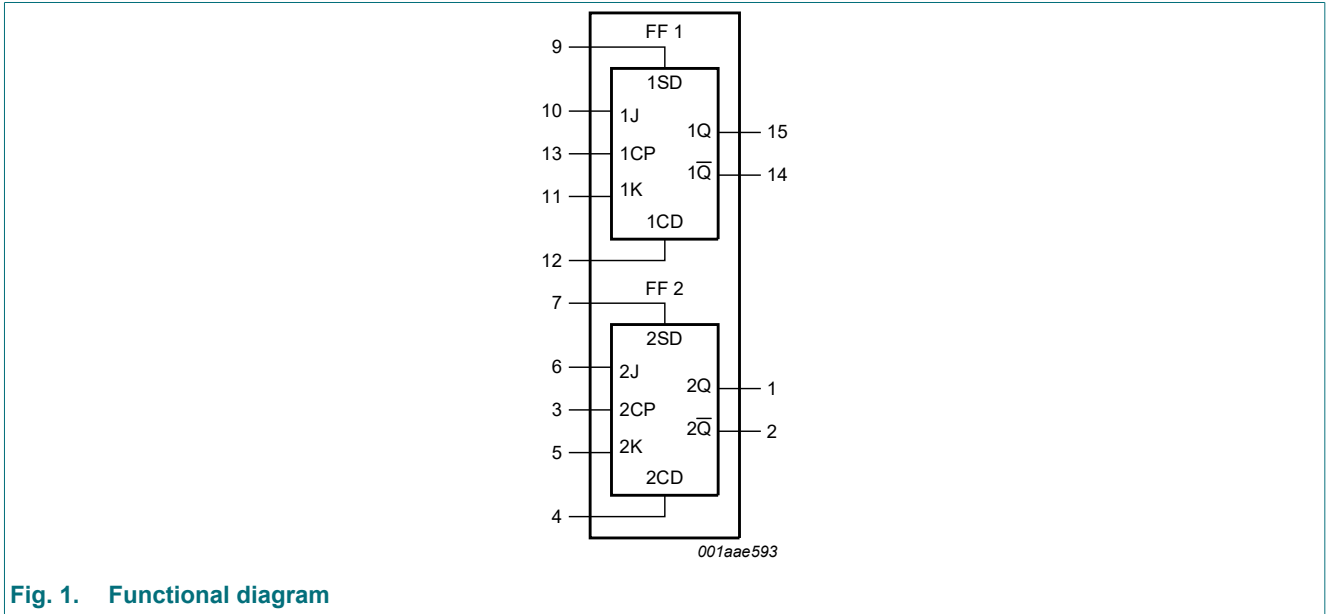


Fig. 1. Functional diagram

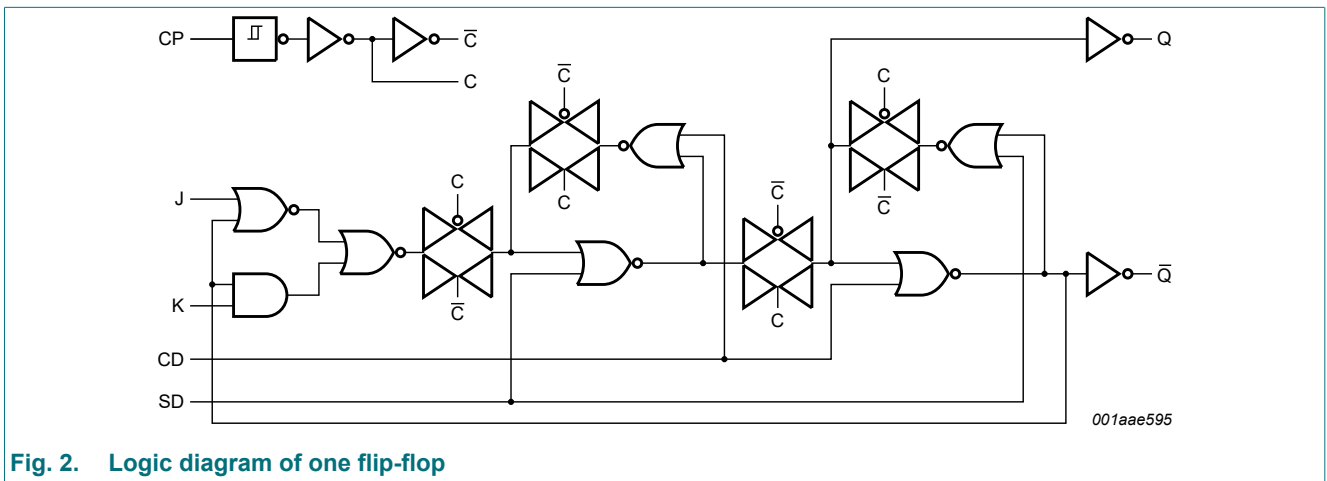


Fig. 2. Logic diagram of one flip-flop

6. Pinning information

6.1. Pinning

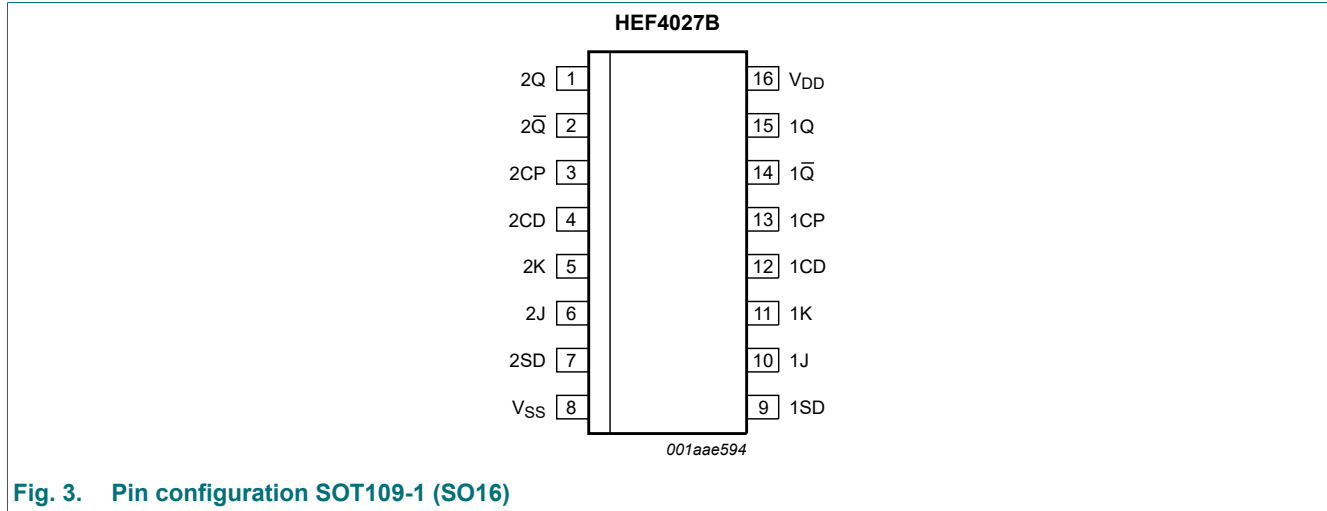


Fig. 3. Pin configuration SOT109-1 (SO16)

6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
V_{SS}	8	ground supply voltage
1SD, 2SD	9, 7	asynchronous set-direct input (active HIGH)
1J, 2J	10, 6	synchronous input
1K, 2K	11, 5	synchronous input
1CD, 2CD	12, 4	asynchronous clear-direct input (active HIGH)
1CP, 2CP	13, 3	clock input (LOW-to-HIGH edge-triggered)
1Q, 2Q	15, 1	true output
1Q, 2Q	14, 2	complement output
V_{DD}	16	supply voltage

7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.; \uparrow = positive-going transition.

Inputs					Outputs	
nSD	nCD	nCP	nJ	nK	nQ	nQ
H	L	X	X	X	H	L
L	H	X	X	X	L	H
H	H	X	X	X	H	H
L	L	\uparrow	L	L	no change	no change
L	L	\uparrow	H	L	H	L
L	L	\uparrow	L	H	L	H
L	L	\uparrow	H	H	nQ	nQ

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+18	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{DD} + 0.5\text{ V}$	-	± 10	mA
V_I	input voltage		-0.5	$V_{DD} + 0.5$	V
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{DD} + 0.5\text{ V}$	-	± 10	mA
$I_{I/O}$	input/output current		-	± 10	mA
I_{DD}	supply current		-	50	mA
T_{stg}	storage temperature		-65	+150	°C
T_{amb}	ambient temperature	in free air	-40	+85	°C
P_{tot}	total power dissipation	$T_{amb} -40\text{ °C}$ to $+85\text{ °C}$	-	500	mW
P	power dissipation	per output	-	100	mW

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		3	15	V
V_I	input voltage		0	V_{DD}	V
T_{amb}	ambient temperature	in free air	-40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5\text{ V}$	-	3.75	$\mu\text{s/V}$
		$V_{DD} = 10\text{ V}$	-	0.5	$\mu\text{s/V}$
		$V_{DD} = 15\text{ V}$	-	0.08	$\mu\text{s/V}$

10. Static characteristics

Table 6. Static characteristics

$V_{SS} = 0\text{ V}$; $V_I = V_{SS}$ or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	$T_{amb} = -40\text{ °C}$		$T_{amb} = +25\text{ °C}$		$T_{amb} = +85\text{ °C}$		Unit
				Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$ I_O < 1\ \mu\text{A}$	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$ I_O < 1\ \mu\text{A}$	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$ I_O < 1\ \mu\text{A}$	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$ I_O < 1\ \mu\text{A}$	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V

Symbol	Parameter	Conditions	V _{DD}	T _{amb} = -40 °C		T _{amb} = +25 °C		T _{amb} = +85 °C		Unit
				Min	Max	Min	Max	Min	Max	
I _{OH}	HIGH-level output current	V _O = 2.5 V	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		V _O = 4.6 V	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		V _O = 9.5 V	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		V _O = 13.5 V	15 V	-	-3.6	-	-3.0	-	-2.4	mA
I _{OL}	LOW-level output current	V _O = 0.4 V	5 V	0.52	-	0.44	-	0.36	-	mA
		V _O = 0.5 V	10 V	1.3	-	1.1	-	0.9	-	mA
		V _O = 1.5 V	15 V	3.6	-	3.0	-	2.4	-	mA
I _I	input leakage current		15 V	-	±0.3	-	±0.3	-	±1.0	µA
I _{DD}	supply current	I _O = 0 A	5 V	-	4.0	-	4.0	-	30	µA
			10 V	-	8.0	-	8.0	-	60	µA
			15 V	-	16.0	-	16.0	-	120	µA
C _I	input capacitance		-	-	-	-	7.5	-	-	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

V_{SS} = 0 V; T_{amb} = 25 °C unless otherwise specified; for test circuit see Fig. 7.

Symbol	Parameter	Conditions	V _{DD}	Extrapolation formula [1]	Min	Typ	Max	Unit
t _{PHL}	HIGH to LOW propagation delay	CP → Q, \bar{Q} ; see Fig. 4	5 V	78 ns + (0.55 ns/pF)C _L	-	105	210	ns
			10 V	29 ns + (0.23 ns/pF)C _L	-	40	80	ns
			15 V	22 ns + (0.16 ns/pF)C _L	-	30	60	ns
		CD → Q; see Fig. 4	5 V	93 ns + (0.55 ns/pF)C _L	-	120	240	ns
			10 V	33 ns + (0.23 ns/pF)C _L	-	45	90	ns
			15 V	27 ns + (0.16 ns/pF)C _L	-	35	70	ns
		SD → \bar{Q} ; see Fig. 4	5 V	113 ns + (0.55 ns/pF)C _L	-	140	280	ns
			10 V	44 ns + (0.23 ns/pF)C _L	-	55	110	ns
			15 V	32 ns + (0.16 ns/pF)C _L	-	40	80	ns
t _{PLH}	LOW to HIGH propagation delay	CP → Q, \bar{Q} ; see Fig. 4	5 V	58 ns + (0.55 ns/pF)C _L	-	85	170	ns
			10 V	27 ns + (0.23 ns/pF)C _L	-	35	70	ns
			15 V	22 ns + (0.16 ns/pF)C _L	-	30	60	ns
		CD → \bar{Q} ; see Fig. 4	5 V	48 ns + (0.55 ns/pF)C _L	-	75	150	ns
			10 V	24 ns + (0.23 ns/pF)C _L	-	35	70	ns
			15 V	17 ns + (0.16 ns/pF)C _L	-	25	50	ns
		SD → Q; see Fig. 4	5 V	43 ns + (0.55 ns/pF)C _L	-	70	140	ns
			10 V	19 ns + (0.23 ns/pF)C _L	-	30	60	ns
			15 V	17 ns + (0.16 ns/pF)C _L	-	25	50	ns
t _t	transition time	see Fig. 4	5 V [2]	10 ns + (1.00 ns/pF)C _L	-	60	120	ns
			10 V	9 ns + (0.42 ns/pF)C _L	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C _L	-	20	40	ns
t _{su}	set-up time	J, K → CP; see Fig. 5	5 V		50	25	-	ns
			10 V		30	10	-	ns
			15 V		20	5	-	ns

Symbol	Parameter	Conditions	V _{DD}	Extrapolation formula [1]	Min	Typ	Max	Unit
t _h	hold time	J, K → CP; see Fig. 5	5 V		25	0	-	ns
			10 V		20	0	-	ns
			15 V		15	5	-	ns
t _w	pulse width	CP LOW; minimum width; see Fig. 5	5 V		80	40	-	ns
			10 V		30	15	-	ns
			15 V		24	12	-	ns
		SD, CD HIGH; minimum width; see Fig. 6	5 V		90	45	-	ns
			10 V		40	20	-	ns
			15 V		30	15	-	ns
t _{rec}	recovery time	SD, CD inputs; see Fig. 6	5 V		+20	-15	-	ns
			10 V		+15	-10	-	ns
			15 V		+10	-5	-	ns
f _{max}	maximum frequency	CP input; J = K = HIGH; see Fig. 5	5 V		4	8	-	MHz
			10 V		12	25	-	MHz
			15 V		15	30	-	MHz

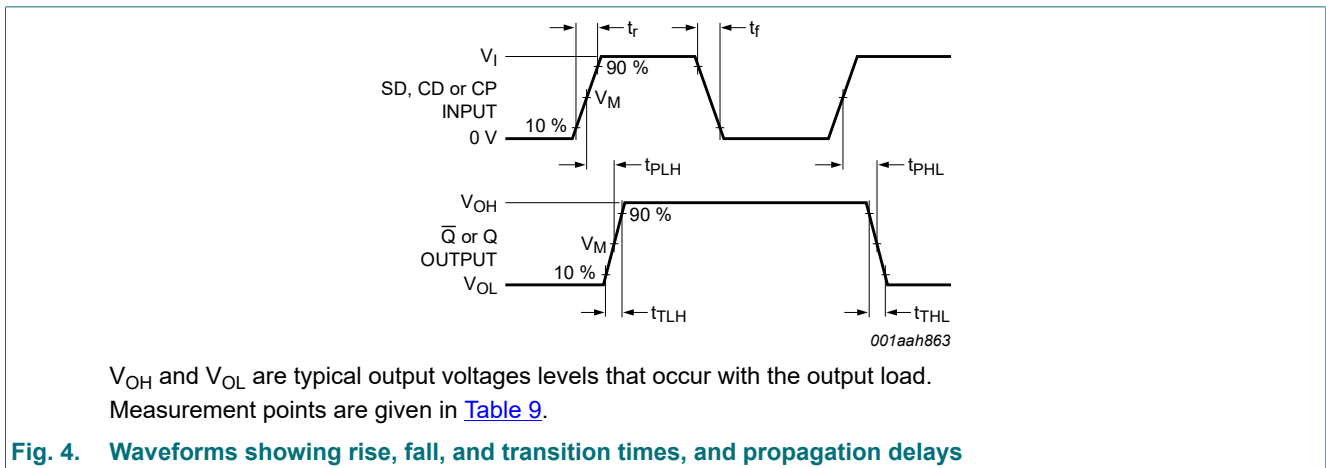
- [1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).
- [2] t_i is the same as t_{TLH} and t_{THL}.

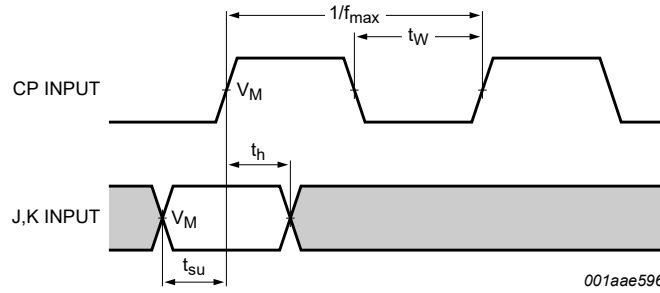
Table 8. Dynamic power dissipation P_D

P_D can be calculated from the formulas shown. V_{SS} = 0 V; t_r = t_f ≤ 20 ns; T_{amb} = 25 °C.

Symbol	Parameter	V _{DD}	Typical formula for P _D (μW)	Where:
P _D	dynamic power dissipation	5 V	$P_D = 900 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f _i = input frequency in MHz f _o = output frequency in MHz C _L = output load capacitance in pF V _{DD} = supply voltage in V Σ(f _o × C _L) = sum of the outputs
		10 V	$P_D = 4500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	
		15 V	$P_D = 13200 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	

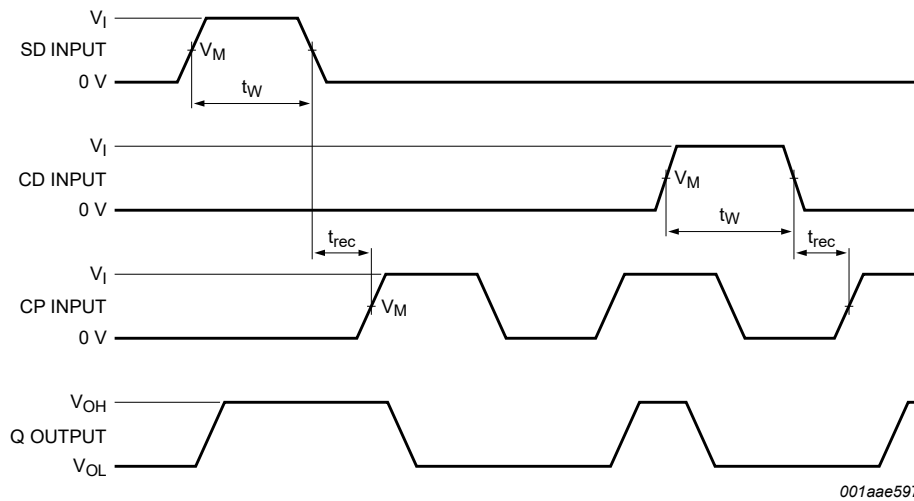
11.1. Waveforms and test circuit





Measurement points are given in [Table 9](#).

Fig. 5. Waveforms showing set-up times, hold times, and minimum clock pulse width

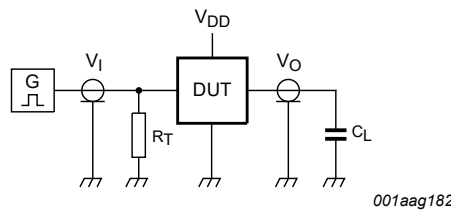


V_{OH} and V_{OL} are typical output voltages levels that occur with the output load.
Measurement points are given in [Table 9](#).

Fig. 6. Waveforms showing pulse widths and recovery times

Table 9. Measurement points

Supply voltage	Input	Output
V_{DD}	V_M	V_M
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$



Test data is given in [Table 10](#).

Definitions for test circuit:

C_L = load capacitance including jig and probe capacitance.

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig. 7. Test circuit

Table 10. Test data

Supply voltage	Input	Load
V_{DD}	V_I	C_L
5 V to 15 V	V_{SS} or V_{DD}	≤ 20 ns
		50 pF

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

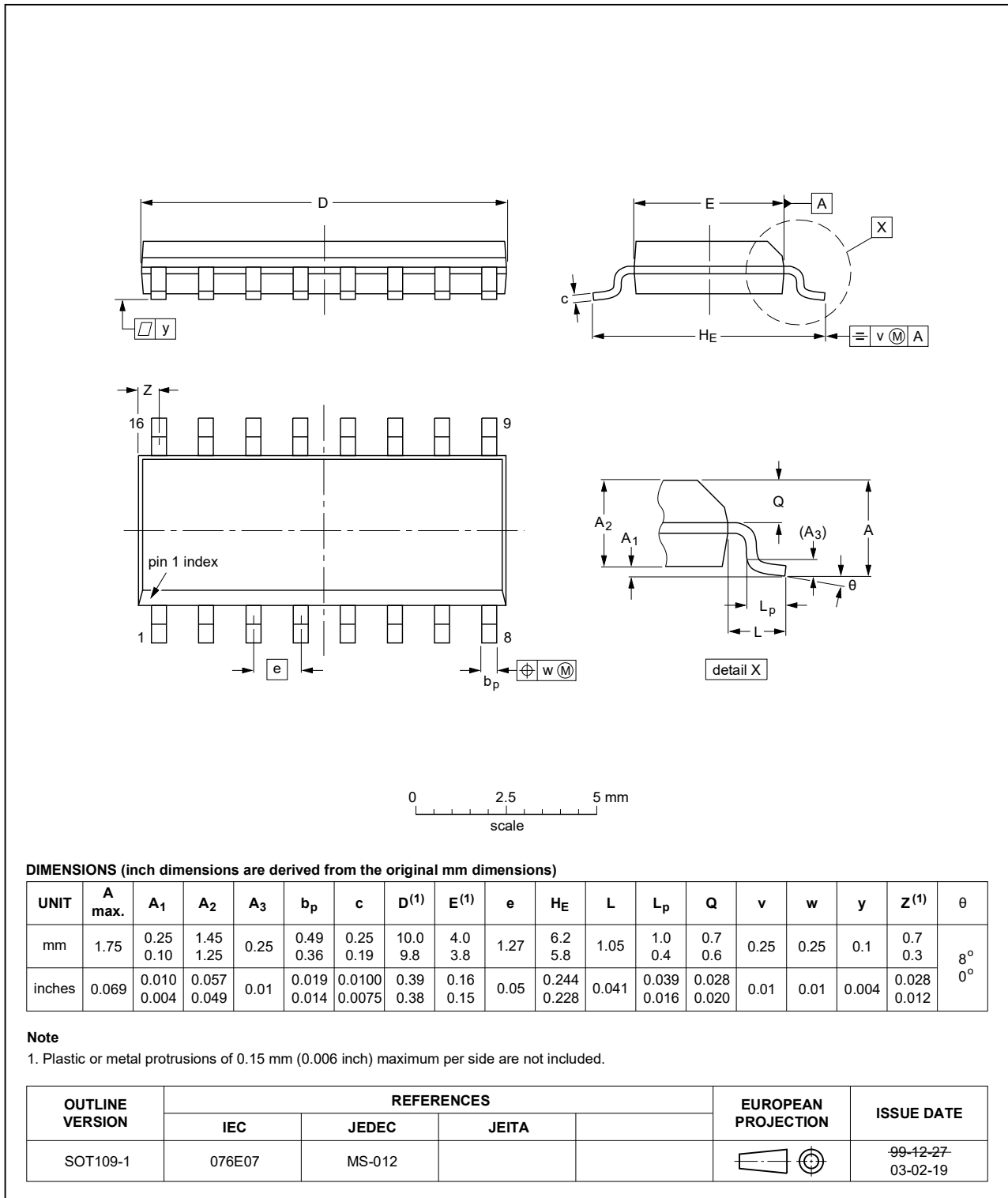


Fig. 8. Package outline SOT109-1 (SO16)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4027B v.11	20211207	Product data sheet	-	HEF4027B v.10
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Section 1 and Section 2 updated. Section 13 added. 			
HEF4027B v.10	20160321	Product data sheet	-	HEF4027B v.9
Modifications:	<ul style="list-style-type: none"> Type number HEF4027BP (SOT38-4) removed. 			
HEF4027B v.9	20111118	Product data sheet	-	HEF4027B v.8
Modifications:	<ul style="list-style-type: none"> Legal pages updated. Changes in Section 1 and Section 2 			
HEF4027B v.8	20111010	Product data sheet	-	HEF4027B v.7
HEF4027B v.7	20091125	Product data sheet	-	HEF4027B v.6
HEF4027B v.6	20090624	Product data sheet	-	HEF4027B v.5
HEF4027B v.5	20081110	Product data sheet	-	HEF4027B v.4
HEF4027B v.4	20080703	Product specification	-	HEF4027B_CNV v.3
HEF4027B_CNV v.3	19950101	Product specification	-	HEF4027B_CNV v.2
HEF4027B_CNV v.2	19950101	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Contents

1. General description	1
2. Features and benefits	1
3. Applications	1
4. Ordering information	1
5. Functional diagram	2
6. Pinning information	3
6.1. Pinning.....	3
6.2. Pin description.....	3
7. Functional description	3
8. Limiting values	4
9. Recommended operating conditions	4
10. Static characteristics	4
11. Dynamic characteristics	5
11.1. Waveforms and test circuit.....	6
12. Package outline	8
13. Abbreviations	9
14. Revision history	9
15. Legal information	10

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