

**40V DUAL P-CHANNEL ENHANCEMENT MODE MOSFET**

**Product Summary**

$V_{(BR)DSS}$	$R_{DS(on) Max}$	$I_D$ $T_A = +25^\circ C$
-40V	50mΩ @ $V_{GS} = -10V$	-5.2A
	79mΩ @ $V_{GS} = -4.5V$	-4.1A

**Description**

This MOSFET has been designed to minimize the on-state resistance and yet maintain superior switching performance, making it ideal for high efficiency power management applications.


**Applications**

- Motor Control
- Backlighting
- DC-DC Converters
- Power Management Functions

**Features and Benefits**

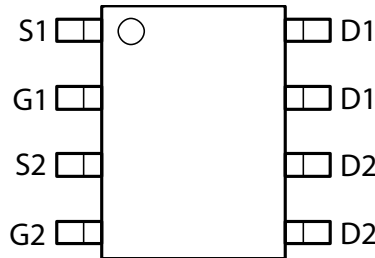
- Low On-Resistance
- Fast Switching Speed
- **Totally Lead-Free & Fully RoHS compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

**Mechanical Data**

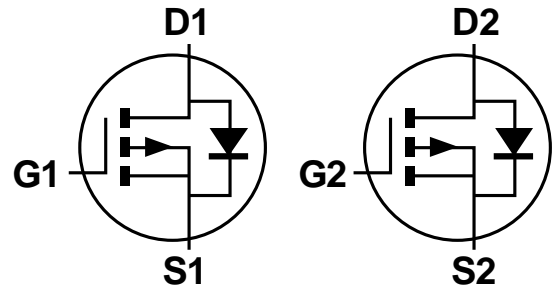
- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0 (Note 1)
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals Connections: See diagram below
- Terminals: Finish - Matte Tin annealed over Copper lead frame. Solderable per MIL-STD-202, Method 208 
- Weight: 0.074 grams (approximate)



Top View



Top View



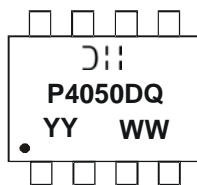
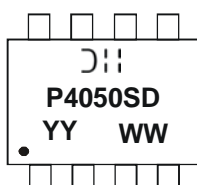
Equivalent Circuit


**Ordering Information** (Note 4)

Part Number	Qualification	Case	Packaging
DMP4050SSD-13	Standard	SO-8	2500 / Tape & Reel
DMP4050SSDQ-13	Automotive	SO-8	2500 / Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
  2. See [http://www.diodes.com/quality/lead\\_free.html](http://www.diodes.com/quality/lead_free.html) for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

**Marking Information**



 = Manufacturer's Marking  
 P4050SD = Product Type Marking Code for DMP4050SSD-13  
 P4050DQ = Product Type Marking Code for DMP4050SSDQ-13  
 YYWW = Date Code Marking  
 YY = Year (ex: 09 = 2009)  
 WW = Week (01-53)

**Maximum Ratings** (@ $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

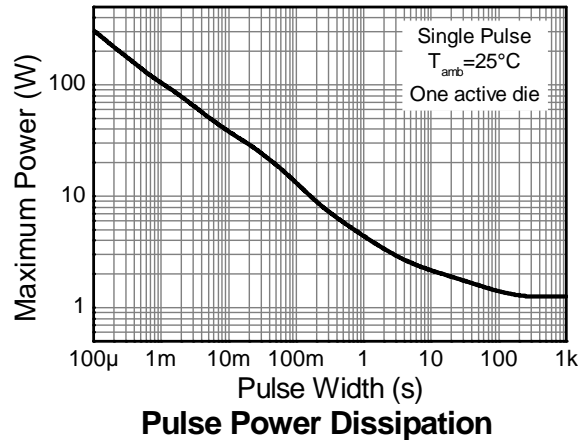
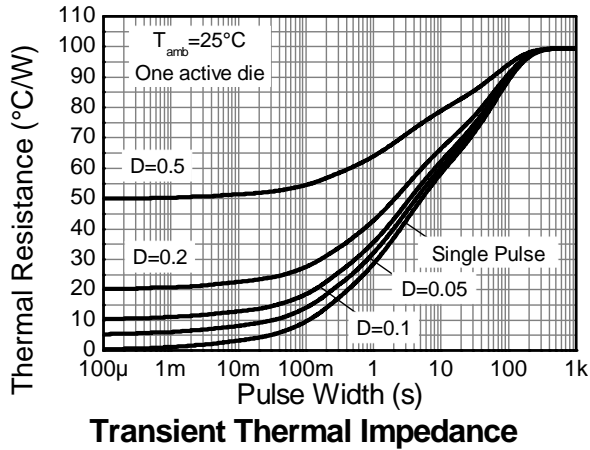
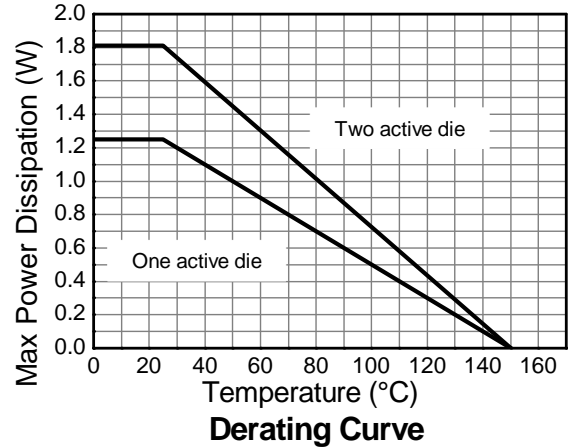
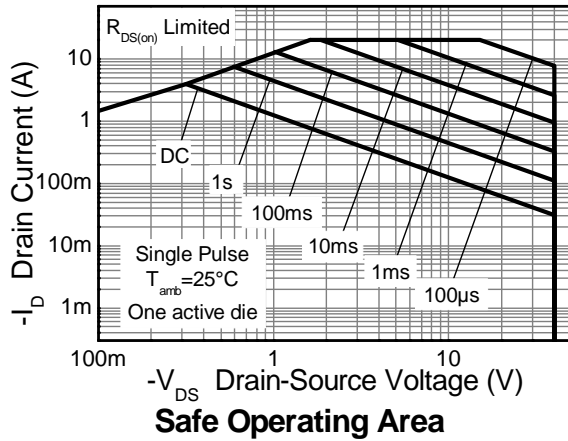
Characteristic			Symbol	Value	Unit
Drain-Source Voltage			$V_{DSS}$	-40	V
Gate-Source Voltage		(Note 5)	$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$V_{GS} = 10\text{V}$	(Notes 9 & 11)	$I_D$	-5.2	A
		$T_A = +70^\circ\text{C}$ (Notes 7 & 9)		-4.2	
		(Notes 6 & 9)		-4.0	
Pulsed Drain Current	$V_{GS} = 10\text{V}$	(Notes 8 & 9)	$I_{DM}$	-20.0	A
Continuous Source Current (Body Diode)			$I_S$	-3.2	A
Pulsed Source Current (Body Diode)			$I_{SM}$	-20.0	A

**Thermal Characteristics** (@ $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Power dissipation Linear derating factor	(Notes 6 & 9)	$P_D$	1.25	W mW/ $^\circ\text{C}$
			10.0	
	(Notes 6 & 10)		1.8	
			14.3	
Thermal Resistance, Junction to Ambient	(Notes 7 & 9)	$R_{\theta JA}$	2.14	$^\circ\text{C/W}$
	(Notes 6 & 9)		100	
	(Notes 6 & 10)		70	
	(Notes 7 & 9)	58		
Thermal Resistance, Junction to Lead	(Notes 9 & 11)	$R_{\theta JL}$	53	
Operating and storage temperature range		$T_J, T_{STG}$	-55 to +150	$^\circ\text{C}$

- Notes:
- AEC-Q101  $V_{GS}$  maximum is  $\pm 16\text{V}$ .
  - For a device surface mounted on 25mm x 25mm x 1.6mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
  - Same as note (3), except the device is measured at  $t \leq 10$  sec.
  - Same as note (3), except the device is pulsed with  $D = 0.02$  and pulse width 300 $\mu\text{s}$ . The pulse current is limited by the maximum junction temperature.
  - For a dual device with one active die.
  - For a device with two active die running at equal power.
  - Thermal resistance from junction to solder-point (at the end of the drain lead).

**Thermal Characteristics**

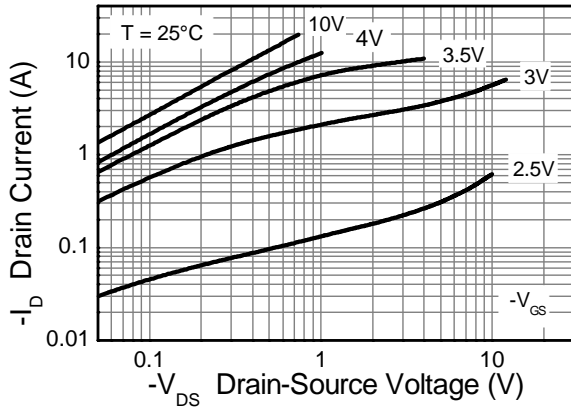


**Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

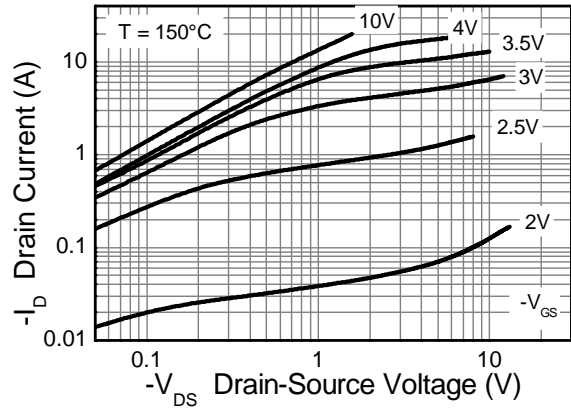
Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	-40	—	—	V	I <sub>D</sub> = -250μA, V <sub>GS</sub> = 0V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	—	—	-0.5	μA	V <sub>DS</sub> = -40V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	—	—	±100	nA	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	-1.0	—	-3.0	V	I <sub>D</sub> = -250μA, V <sub>DS</sub> = V <sub>GS</sub>
Static Drain-Source On-Resistance (Note 12)	R <sub>DS(ON)</sub>	—	0.038	0.050	Ω	V <sub>GS</sub> = -10V, I <sub>D</sub> = -6A
			0.055	0.079		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -5A
Forward Transconductance (Notes 12 & 13)	g <sub>fs</sub>	—	14	—	S	V <sub>DS</sub> = -15V, I <sub>D</sub> = -6A
Diode Forward Voltage (Note 12)	V <sub>SD</sub>	—	-0.86	-1.2	V	I <sub>S</sub> = -6A, V <sub>GS</sub> = 0V
Reverse recovery time (Note 13)	t <sub>rr</sub>	—	18	—	ns	I <sub>S</sub> = -2A, di/dt = 100A/μs
Reverse recovery charge (Note 13)	Q <sub>rr</sub>	—	12.7	—	nC	
<b>DYNAMIC CHARACTERISTICS (Note 13)</b>						
Input Capacitance	C <sub>iSS</sub>	—	674	—	pF	V <sub>DS</sub> = -20V, V <sub>GS</sub> = 0V f = 1MHz
Output Capacitance	C <sub>oSS</sub>	—	115	—	pF	
Reverse Transfer Capacitance	C <sub>rSS</sub>	—	67.7	—	pF	
Total Gate Charge (Note 14)	Q <sub>g</sub>	—	6.9	—	nC	V <sub>GS</sub> = -4.5V
Total Gate Charge (Note 14)	Q <sub>g</sub>	—	13.9	—	nC	V <sub>GS</sub> = -10V
Gate-Source Charge (Note 14)	Q <sub>gs</sub>	—	2	—	nC	
Gate-Drain Charge (Note 14)	Q <sub>gd</sub>	—	3.4	—	nC	
Turn-On Delay Time (Note 14)	t <sub>D(on)</sub>	—	1.9	—	ns	V <sub>DD</sub> = -20V, V <sub>GS</sub> = -10V I <sub>D</sub> = -1A, R <sub>G</sub> ≅ 6.0Ω
Turn-On Rise Time (Note 14)	t <sub>r</sub>	—	3.1	—	ns	
Turn-Off Delay Time (Note 14)	t <sub>D(off)</sub>	—	31.5	—	ns	
Turn-Off Fall Time (Note 14)	t <sub>f</sub>	—	12.6	—	ns	

- Notes:
- 12. Measured under pulsed conditions. Pulse width ≤ 300μs; duty cycle ≤ 2%
  - 13. For design aid only, not subject to production testing.
  - 14. Switching characteristics are independent of operating junction temperatures.

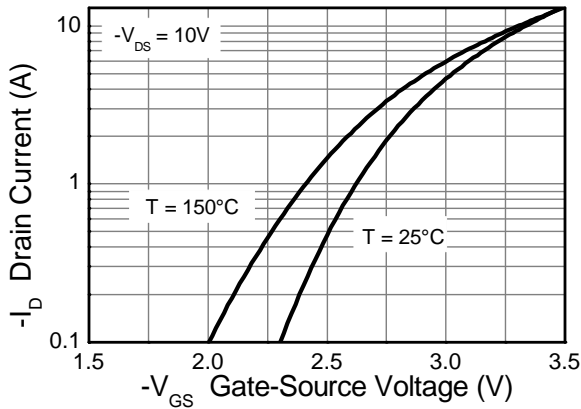
**Typical Characteristics**



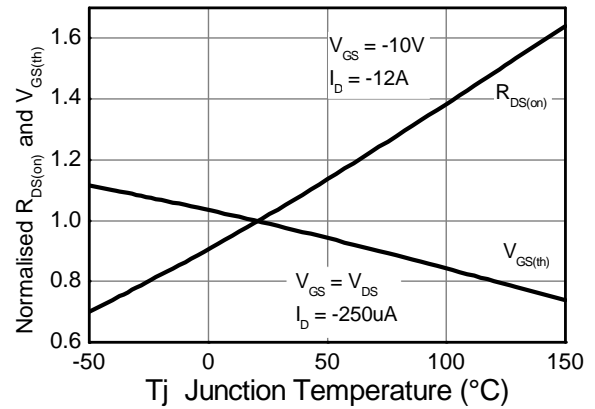
**Output Characteristics**



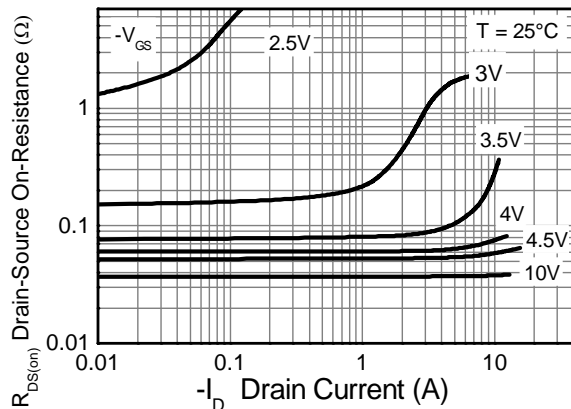
**Output Characteristics**



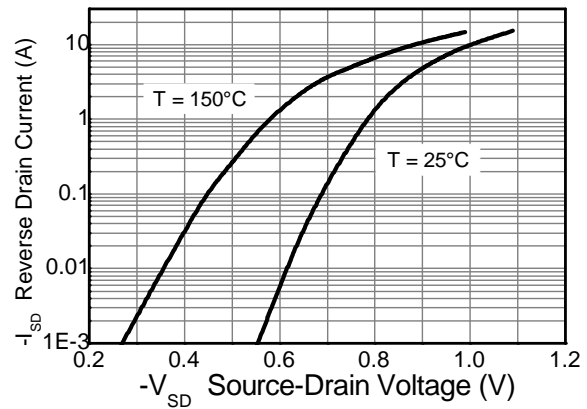
**Typical Transfer Characteristics**



**Normalised Curves v Temperature**

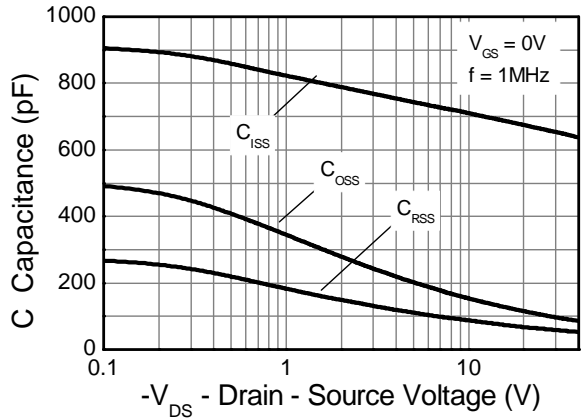


**On-Resistance v Drain Current**

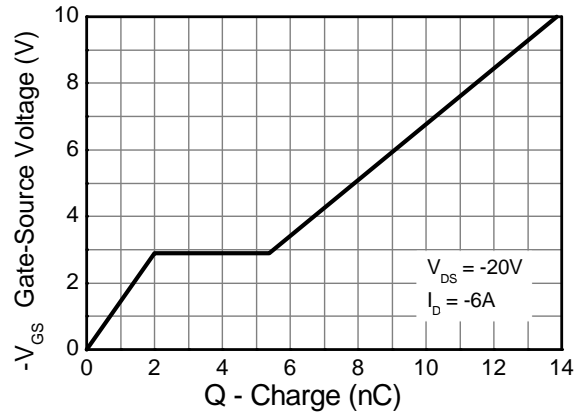


**Source-Drain Diode Forward Voltage**

**Typical Characteristics – (cont.)**

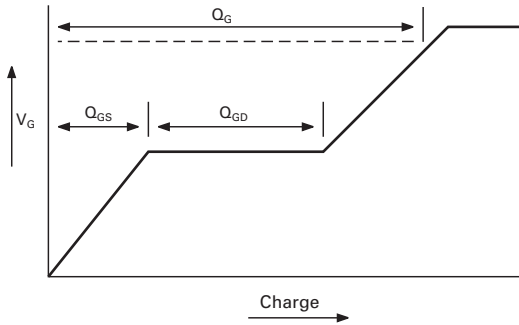


**Capacitance v Drain-Source Voltage**

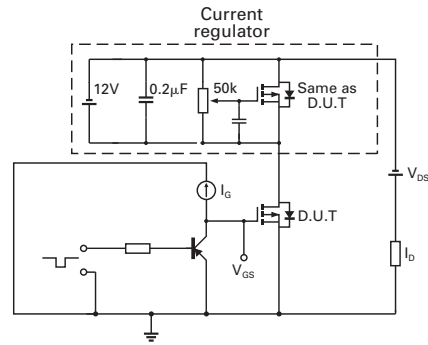


**Gate-Source Voltage v Gate Charge**

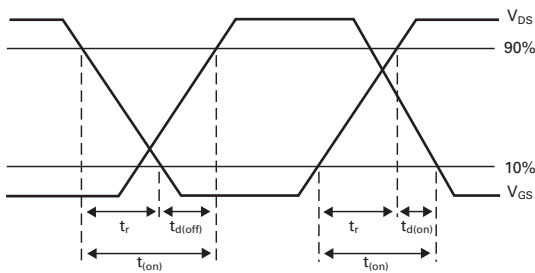
**Test Circuits**



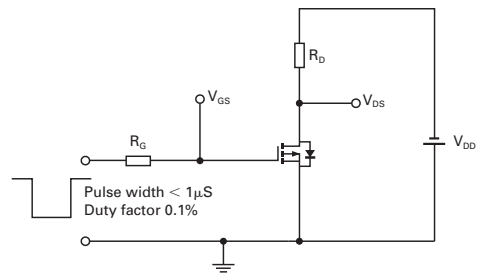
**Basic gate charge waveform**



**Gate charge test circuit**



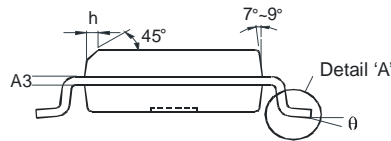
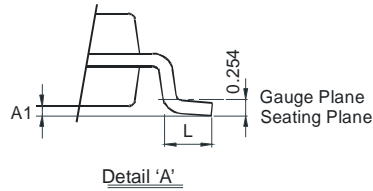
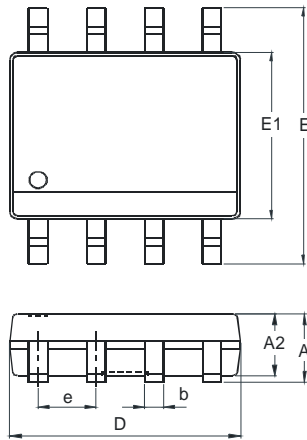
**Switching time waveforms**



**Switching time test circuit**

**Package Outline Dimensions**

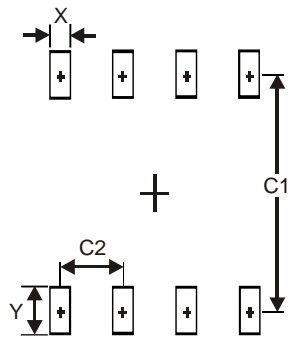
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.



SO-8		
Dim	Min	Max
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

**Suggested Pad Layout**

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27

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