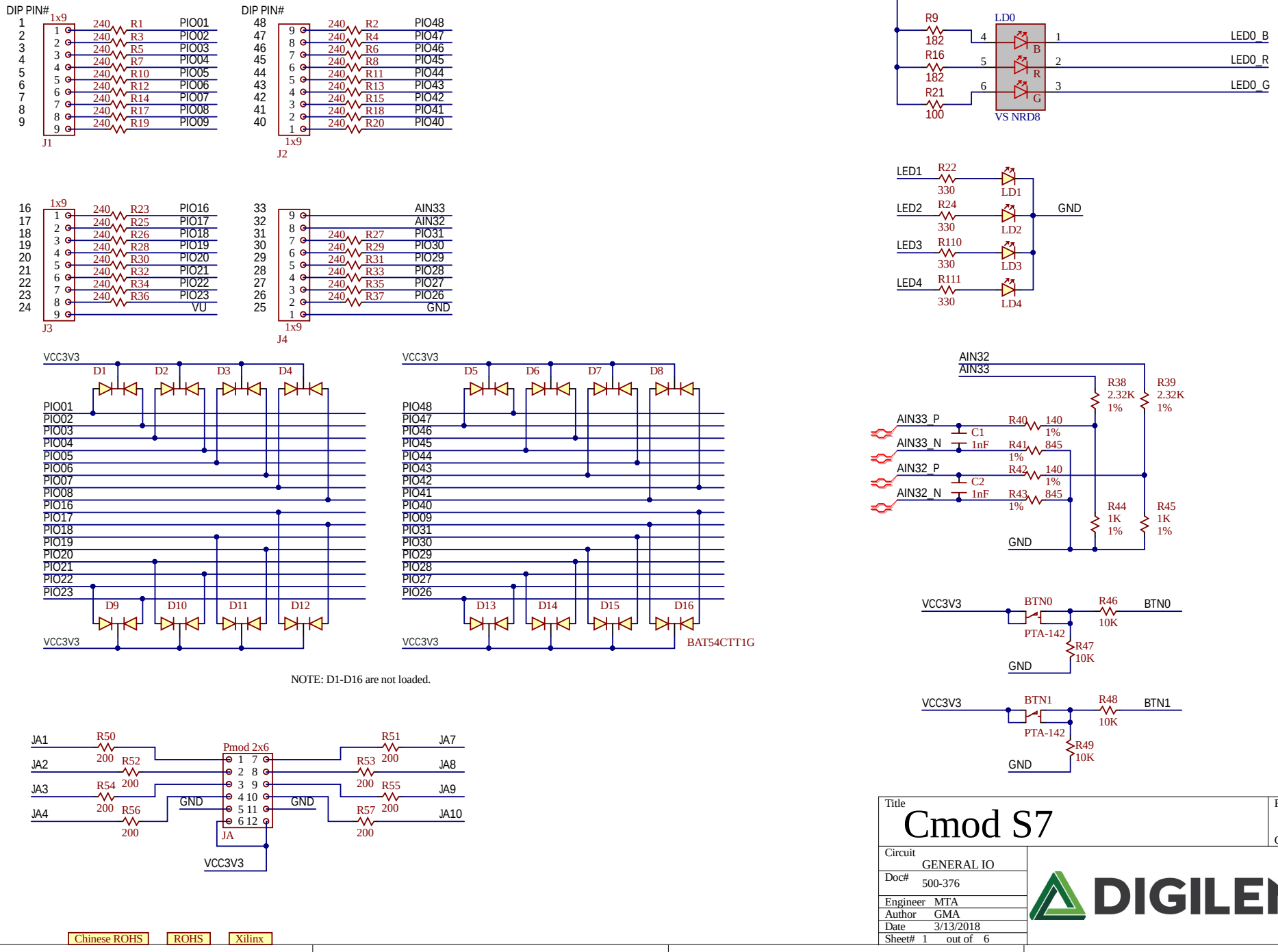

NOTE: D1-D16 are not loaded.

Chinese ROHS ROHS Xilinx

Title	Cmod S7
Rev	B.0
Copyright	2018
Circuit	GENERAL IO
Doc#	500-376
Engineer	MTA
Author	GMA
Date	3/13/2018
Sheet#	1 out of 6

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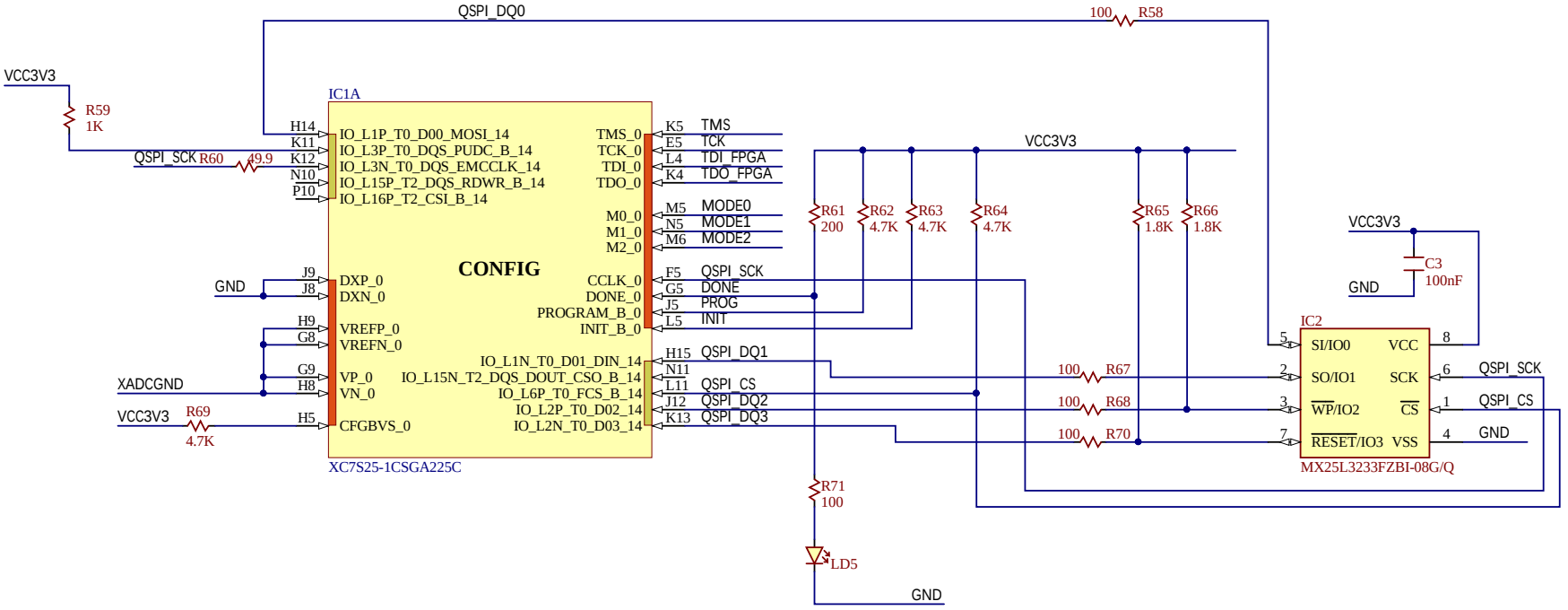

Title	Cmod S7
Rev	B.0
Copyright	2018
Circuit	CONFIG, SPI FLASH
Doc#	500-376
Engineer	MTA
Author	GMA
Date	3/13/2018
Sheet#	2 out of 6

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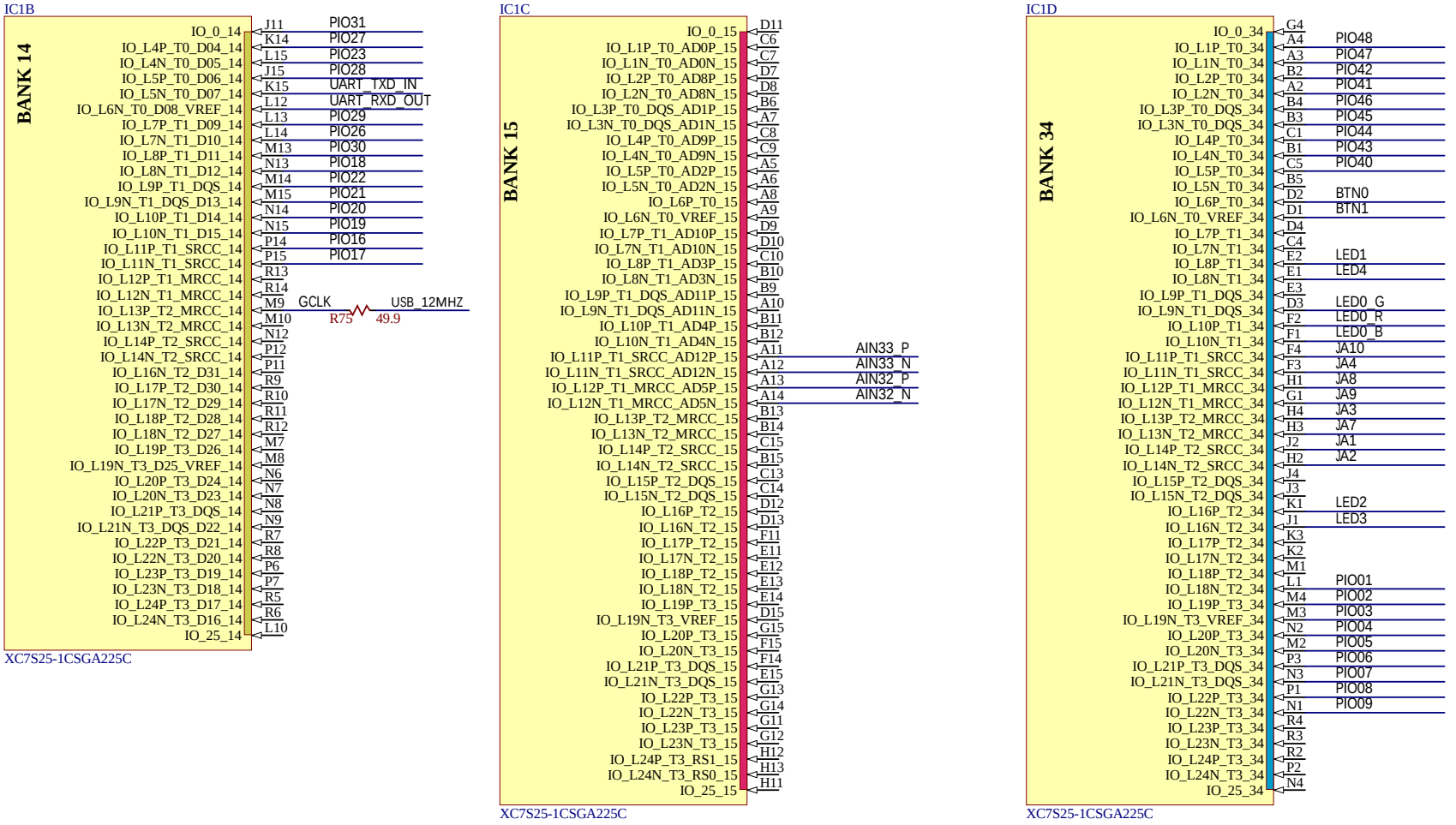
IC1B
BANK 14
IO_0_14
IO_L4P_T0_D04_14
IO_L4N_T0_D05_14
IO_L5P_T0_D06_14
IO_L5N_T0_D07_14
IO_L6N_T0_D08_VREF_14
IO_L7P_T1_D09_14
IO_L7N_T1_D10_14
IO_L8P_T1_D11_14
IO_L8N_T1_D12_14
IO_L9P_T1_DQS_14
IO_L9N_T1_DQS_D13_14
IO_L10P_T1_D14_14
IO_L10N_T1_D15_14
IO_L11P_T1_SRCC_14
IO_L11N_T1_SRCC_14
IO_L12P_T1_MRCC_14
IO_L12N_T1_MRCC_14
IO_L13P_T2_MRCC_14
IO_L13N_T2_MRCC_14
IO_L14P_T2_SRCC_14
IO_L14N_T2_SRCC_14
IO_L16N_T2_D31_14
IO_L17P_T2_D30_14
IO_L17N_T2_D29_14
IO_L18P_T2_D28_14
IO_L18N_T2_D27_14
IO_L19P_T3_D26_14
IO_L19N_T3_D25_VREF_14
IO_L20P_T3_D24_14
IO_L20N_T3_D23_14
IO_L21P_T3_DQS_14
IO_L21N_T3_DQS_D22_14
IO_L22P_T3_D21_14
IO_L22N_T3_D20_14
IO_L23P_T3_D19_14
IO_L23N_T3_D18_14
IO_L24P_T3_D17_14
IO_L24N_T3_D16_14
IO_25_14
J11
K14
L15
J15
K15
L12
L13
L14
M13
N13
M14
M15
N14
N15
P14
P15
R13
R14
M9
M10
N12
P12
P11
R9
R10
R11
R12
M7
M8
N6
N7
N8
N9
R7
R8
P6
P7
R5
R6
L10
PIO31
PIO27
PIO23
PIO28
UART_TXD_IN
UART_RXD_OUT
PIO29
PIO26
PIO30
PIO18
PIO22
PIO21
PIO20
PIO19
PIO16
PIO17
GCLK
R75
49.9
USB_12MHZ
XC7S25-1CSGA225C
IC1C
BANK 15
IO_0_15
IO_L1P_T0_AD0P_15
IO_L1N_T0_AD0N_15
IO_L2P_T0_AD8P_15
IO_L2N_T0_AD8N_15
IO_L3P_T0_DQS_AD1P_15
IO_L3N_T0_DQS_AD1N_15
IO_L4P_T0_AD9P_15
IO_L4N_T0_AD9N_15
IO_L5P_T0_AD2P_15
IO_L5N_T0_AD2N_15
IO_L6P_T0_15
IO_L6N_T0_VREF_15
IO_L7P_T1_AD10P_15
IO_L7N_T1_AD10N_15
IO_L8P_T1_AD3P_15
IO_L8N_T1_AD3N_15
IO_L9P_T1_DQS_AD11P_15
IO_L9N_T1_DQS_AD11N_15
IO_L10P_T1_AD4P_15
IO_L10N_T1_AD4N_15
IO_L11P_T1_SRCC_AD12P_15
IO_L11N_T1_SRCC_AD12N_15
IO_L12P_T1_MRCC_AD5P_15
IO_L12N_T1_MRCC_AD5N_15
IO_L13P_T2_MRCC_15
IO_L13N_T2_MRCC_15
IO_L14P_T2_SRCC_15
IO_L14N_T2_SRCC_15
IO_L15P_T2_DQS_15
IO_L15N_T2_DQS_15
IO_L16P_T2_15
IO_L16N_T2_15
IO_L17P_T2_15
IO_L17N_T2_15
IO_L18P_T2_15
IO_L18N_T2_15
IO_L19P_T3_15
IO_L19N_T3_VREF_15
IO_L20P_T3_15
IO_L20N_T3_15
IO_L21P_T3_DQS_15
IO_L21N_T3_DQS_15
IO_L22P_T3_15
IO_L22N_T3_15
IO_L23P_T3_15
IO_L23N_T3_15
IO_L24P_T3_RS1_15
IO_L24N_T3_RS0_15
IO_25_15
D11
C6
C7
D7
D8
B6
A7
C8
C9
A5
A6
A8
A9
D9
D10
C10
B10
B9
A10
B11
B12
A11
A12
A13
A14
B13
B14
C15
B15
C13
C14
D12
D13
F11
E11
E12
E13
E14
D15
G15
F15
F14
E15
G13
G14
G11
G12
H12
H13
H11
AIN33_P
AIN33_N
AIN32_P
AIN32_N
XC7S25-1CSGA225C
IC1D
BANK 34
IO_0_34
IO_L1P_T0_34
IO_L1N_T0_34
IO_L2P_T0_34
IO_L2N_T0_34
IO_L3P_T0_DQS_34
IO_L3N_T0_DQS_34
IO_L4P_T0_34
IO_L4N_T0_34
IO_L5P_T0_34
IO_L5N_T0_34
IO_L6P_T0_34
IO_L6N_T0_VREF_34
IO_L7P_T1_34
IO_L7N_T1_34
IO_L8P_T1_34
IO_L8N_T1_34
IO_L9P_T1_DQS_34
IO_L9N_T1_DQS_34
IO_L10P_T1_34
IO_L10N_T1_34
IO_L11P_T1_SRCC_34
IO_L11N_T1_SRCC_34
IO_L12P_T1_MRCC_34
IO_L12N_T1_MRCC_34
IO_L13P_T2_MRCC_34
IO_L13N_T2_MRCC_34
IO_L14P_T2_SRCC_34
IO_L14N_T2_SRCC_34
IO_L15P_T2_DQS_34
IO_L15N_T2_DQS_34
IO_L16P_T2_34
IO_L16N_T2_34
IO_L17P_T2_34
IO_L17N_T2_34
IO_L18P_T2_34
IO_L18N_T2_34
IO_L19P_T3_34
IO_L19N_T3_VREF_34
IO_L20P_T3_34
IO_L20N_T3_34
IO_L21P_T3_DQS_34
IO_L21N_T3_DQS_34
IO_L22P_T3_34
IO_L22N_T3_34
IO_L23P_T3_34
IO_L23N_T3_34
IO_L24P_T3_34
IO_L24N_T3_34
IO_25_34
G4
A4
A3
B2
A2
B4
B3
C1
B1
C5
B5
D2
D1
D4
C4
E2
E1
E3
D3
F2
F1
F4
F3
H1
G1
H4
H3
J2
H2
J4
J3
K1
J1
K3
K2
M1
L1
M4
M3
N2
M2
P3
N3
P1
N1
R4
R3
R2
P2
N4
PIO48
PIO47
PIO42
PIO41
PIO46
PIO45
PIO44
PIO43
PIO40
BTN0
BTN1
LED1
LED4
LED0_G
LED0_R
LED0_B
JA10
JA4
JA8
JA9
JA3
JA7
JA1
JA2
LED2
LED3
PIO01
PIO02
PIO03
PIO04
PIO05
PIO06
PIO07
PIO08
PIO09
XC7S25-1CSGA225C
Title
Cmod S7
Rev
B.0
Copyright 2018
Circuit
FPGA BANKS
Doc#
500-376
Engineer MTA
Author GMA
Date 3/13/2018
Sheet# 3 out of 6
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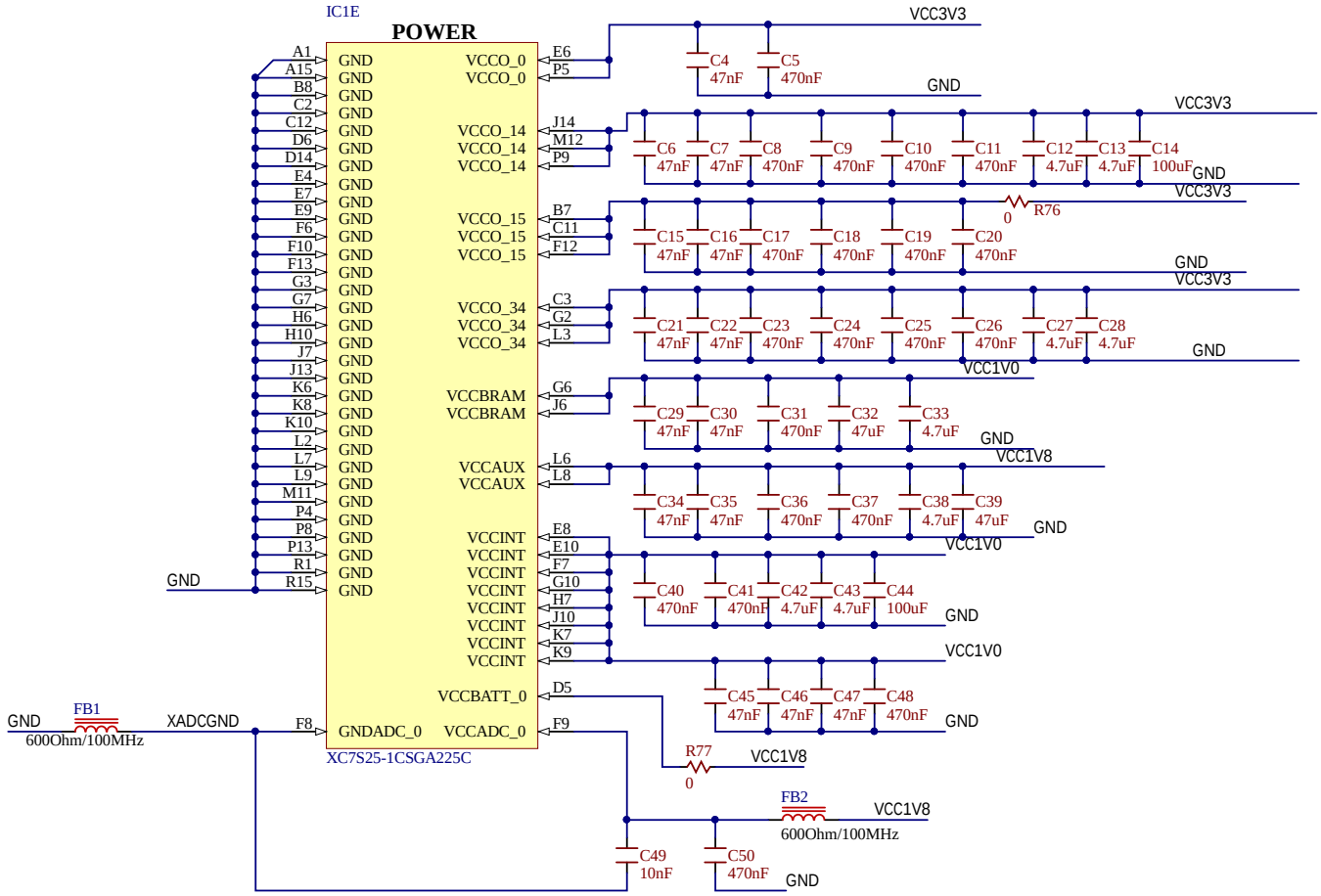

Title	Cmod S7
Rev	B.0
Copyright	2018
Circuit	FPGA POWER
Doc#	500-376
Engineer	MTA
Author	GMA
Date	3/13/2018
Sheet#	4 out of 6

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Title	Cmod S7
Rev	B.0
Circuit	USB PROG/UART
Doc#	500-376
Engineer	MTA
Author	GMA
Date	3/13/2018
Sheet#	5 out of 6

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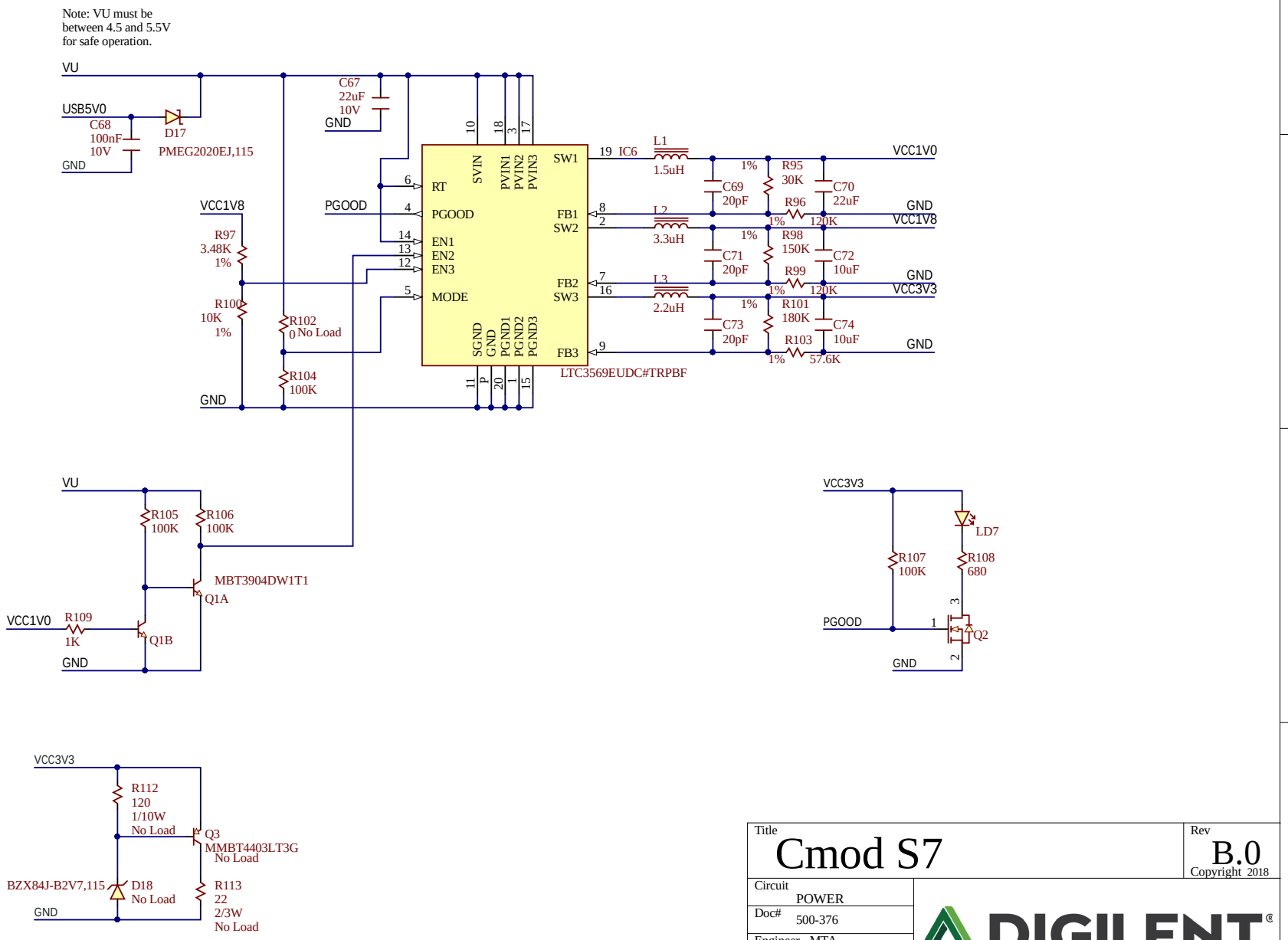
Note: VU must be between 4.5 and 5.5V for safe operation.
VU
USB5V0
C68 100nF 10V
GND
D17 PMEG2020EJ,115
C67 22uF 10V
GND
VCC1V8
R97 3.48K 1%
R100 10K 1%
R102 0 No Load
R104 100K
GND
PGOOD
RT
PGOOD
EN1
EN2
EN3
MODE
SVIN
PVIN1
PVIN2
PVIN3
SW1
FB1
SW2
FB2
SW3
FB3
SGND
GND
PGND1
PGND2
PGND3
LTC3569EUDC#TRPBF
IC6
L1 1.5uH
L2 3.3uH
L3 2.2uH
C69 20pF
C71 20pF
C73 20pF
R95 30K 1%
R96 120K 1%
R98 150K 1%
R99 120K 1%
R101 180K 1%
R103 57.6K 1%
C70 22uF
C72 10uF
C74 10uF
VCC1V0
GND
VCC1V8
GND
VCC3V3
GND
VU
R105 100K
R106 100K
MBT3904DW1T1
Q1A
VCC1V0
R109 1K
Q1B
GND
VCC3V3
LD7
R107 100K
R108 680
PGOOD
Q2
GND
VCC3V3
R112 120 1/10W No Load
Q3 MMBT4403LT3G No Load
BZX84J-B2V7,115
D18 No Load
R113 22 2/3W No Load
GND
Title
Cmod S7
Rev
B.0
Copyright 2018
Circuit
POWER
Doc#
500-376
Engineer MTA
Author GMA
Date 3/13/2018
Sheet# 6 out of 6
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