CAS300M17BM2

1.7kV, 8.0 mΩ All-Silicon Carbide Half-Bridge Module

C2M MOSFET and Z-Rec® Diode

V_{DS}	1.7 kV
$E_{sw, Total @ 300A, 150 °C}$	23.7 mJ
$R_{DS(on)}$	8.0 mΩ

Features

- Ultra Low Loss
- High-Frequency Operation
- Zero Reverse Recovery Current from Diode
- Zero Turn-off Tail Current from MOSFET
- Normally-off, Fail-safe Device Operation
- Ease of Paralleling
- Copper Baseplate and Aluminum Nitride Insulator

System Benefits

- Enables Compact and Lightweight Systems
- High Efficiency Operation
- Mitigates Over-voltage Protection
- Reduced Thermal Requirements
- Reduced System Cost

Applications

- HF Resonant Converters/Inverters
- Solar and Wind Inverters
- UPS and SMPS
- Motor Drive
- Traction

Package 62mm x 106mm x 30mm

Part Number	Package	Marking
CAS300M17BM2	Half-Bridge Module	CAS300M17BM2

Maximum Ratings (T_c = 25˚C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Notes
V_{DSmax}	Drain - Source Voltage	1.7	kV		
V_{GSmax}	Gate - Source Voltage	-10/+25	V	Absolute maximum values	
V_{GSop}	Gate - Source Voltage	-5/20	V	Recommended operational values	
I_D	Continuous MOSFET Drain Current	325	A	V_{GS} = 20 V, T_C = 25 ˚C	Fig. 26
		225		V_{GS} = 20 V, T_C = 90 ˚C	
$I_{D(pulse)}$	Pulsed Drain Current	900	A	Pulse width tp limited by $T_{J(max)}$	
I_F	Continuous Diode Forward Current	556	A	V_{GS} = -5 V, T_C = 25 ˚C	Fig. 27
		353		V_{GS} = -5 V, T_C = 90 ˚C	
T_{Jmax}	Junction Temperature	-40 to +150	˚C		
T_C ,T_{STG}	Case and Storage Temperature Range	-40 to +125	˚C		
V_{isol}	Case Isolation Voltage	4.5	kV	AC, 50 Hz , 1 min	
L_{Stray}	Stray Inductance	15	nH	Measured between terminals 2 and 3	
P_D	Power Dissipation	1760	W	T_C = 25 ˚C, T_J = 150 ˚C	Fig. 25

Electrical Characteristics (T_C = 25˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain - Source Breakdown Voltage	1.7			kV	V_{GS} = 0 V, I_D = 1 mA	
$V_{GS(th)}$	Gate Threshold Voltage	1.8	2.3		V	V_{DS} = 10 V, I_D = 15 mA	Fig. 7
I_{DSS}	Zero Gate Voltage Drain Current		500	1000	μA	V_{DS} = 1.7 kV, V_{GS} = 0V	
			1500	3000	μA	V_{DS} = 1.7 kV,V_{GS} = 0V, T_J = 150 ˚C	
I_{GSS}	Gate-Source Leakage Current		1	600	nA	V_{GS} = 20 V, V_{DS} = 0V	
$R_{DS(on)}$	On State Resistance		8.0	10	mΩ	V_{GS} = 20 V, I_{DS} = 225 A	Fig. 4, 5, 6
			16.2	20		V_{GS} = 20V, I_{DS} = 225 A,T_J = 150 ˚C	
g_{fs}	Transconductance		95		S	V_{DS} = 20 V, I_{DS} = 225 A	Fig. 8
			82			V_{DS} = 20 V, I_D = 225 A, T_J = 150 ˚C	
C_{iss}	Input Capacitance		20		nF	V_{DS} = 1 kV, f = 200 kHz, V_{AC} = 25 mV	Fig. 16, 17
C_{oss}	Output Capacitance		2.5				
C_{rss}	Reverse Transfer Capacitance		0.08				
E_{on}	Turn-On Switching Energy		13.0		mJ	V_{DD} = 900 V, V_{GS} = -5V/+20V I_D = 300 A, $R_{G(ext)}$ = 2.5 Ω Load = 77 μH, T_J = 150 ˚C Note: IEC 60747-8-4 Definitions	Fig. 19
E_{Off}	Turn-Off Switching Energy		10.0		mJ		
$R_{G\ (int)}$	Internal Gate Resistance		3.7		Ω	f = 1 MHz, V_{AC} = 25 mV	
Q_{GS}	Gate-Source Charge		273		nC	V_{DD}= 900 V, V_{GS} = -5V/+20V, I_D= 300 A, Per JEDEC24 pg 27	Fig. 15
Q_{GD}	Gate-Drain Charge		324				
Q_G	Total Gate Charge		1076				
$t_{d(on)}$	Turn-on delay time		105		ns	V_{DD} = 900V, V_{GS} = -5/+20V, I_D = 300 A, $R_{G(ext)}$ = 2.5 Ω, Timing relative to V_{DS} Note: IEC 60747-8-4, pg 83 Inductive load	Fig. 24
t_r	Rise Time		72		ns		
$t_{d(off)}$	Turn-off delay time		211		ns		
t_f	Fall Time		56		ns		
V_{SD}	Diode Forward Voltage		1.7	2.0	V	I_F = 300 A, V_{GS} = 0	Fig. 10
			2.2	2.5		I_F = 300 A, V_{GS} = 0 , T_J = 150 ˚C	Fig. 11
Q_C	Total Capacitive Charge		4.4		μC	I_{SD} = 300 A, V_{DS} = 900 V, T_J = 25°C, di_{SD}/dt = 9 kA/μs, V_{GS} = -5 V	

Thermal Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
R_{thJCM}	Thermal Resistance Juction-to-Case for MOSFET		0.067	0.071	˚C/W		Fig. 27
R_{thJCD}	Thermal Resistance Juction-to-Case for Diode		0.060	0.065			Fig. 28

Additional Module Data

Symbol	Parameter	Max.	Unit	Test Condtion
W	Weight	300	g	
M	Mounting Torque	5	Nm	To heatsink and terminals
	Clearance Distance	9	mm	Terminal to terminal
	Creepage Distance	30	mm	Terminal to terminal
		40	mm	Terminal to baseplate

CREE

Typical Performance

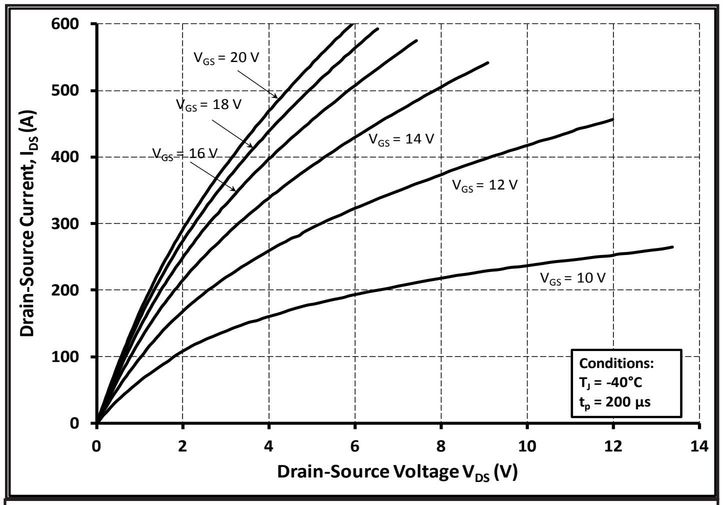


Figure 1. Output Characteristics T_J = -40 °C

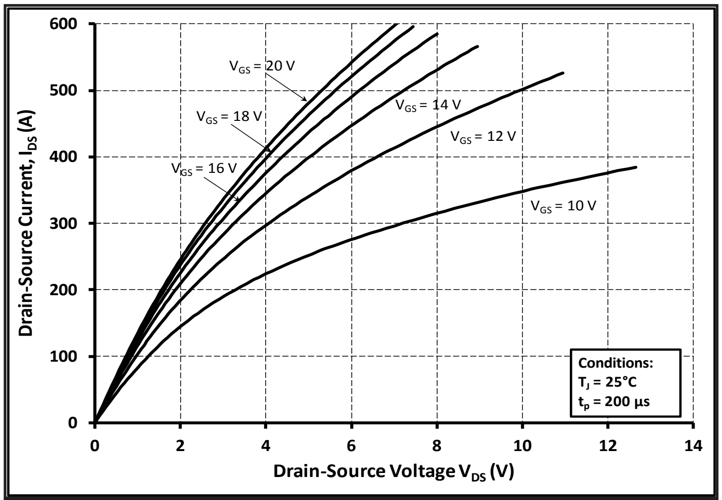


Figure 2. Output Characteristics T_J = 25 °C

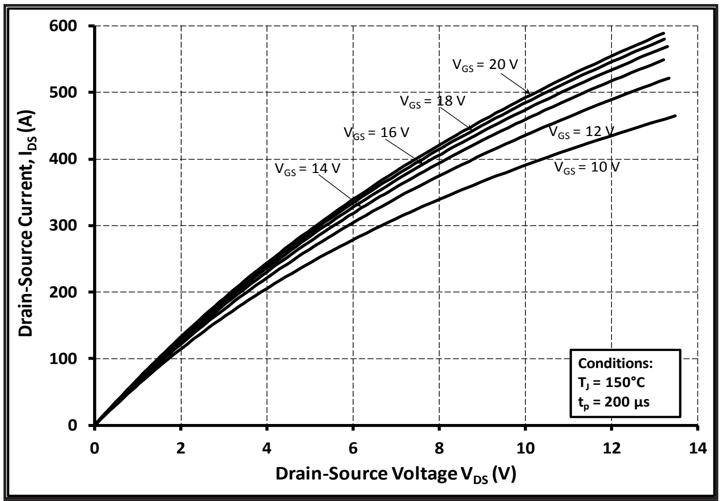


Figure 3. Output Characteristics T_J = 150 °C

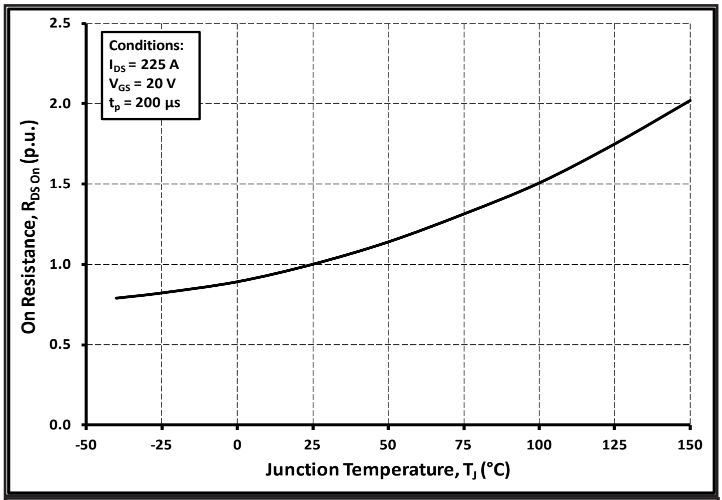


Figure 4. Normalized On-Resistance vs. Temperature

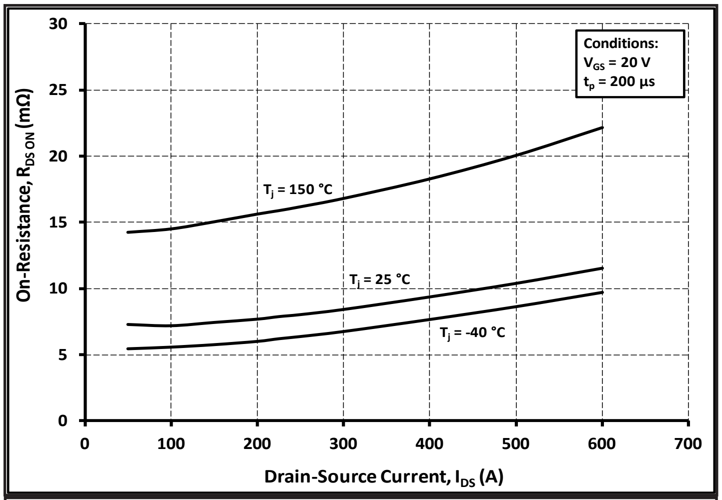


Figure 5. On-Resistance vs. Drain Current For Various Temperatures

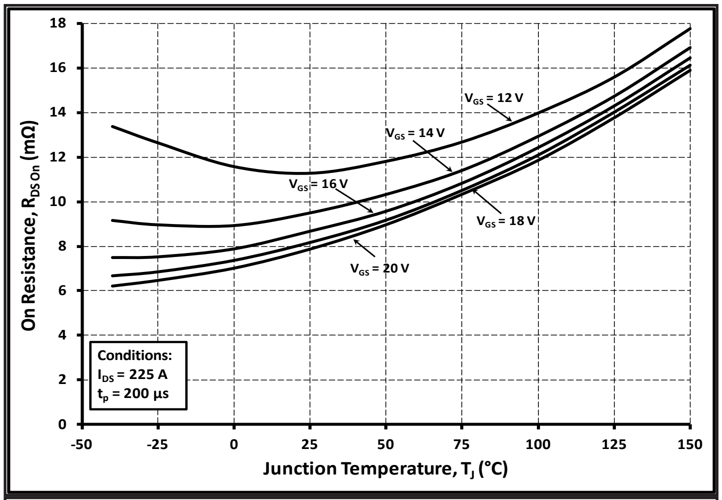


Figure 6. On-Resistance vs. Temperature for Various Gate-Source Voltage

Typical Performance

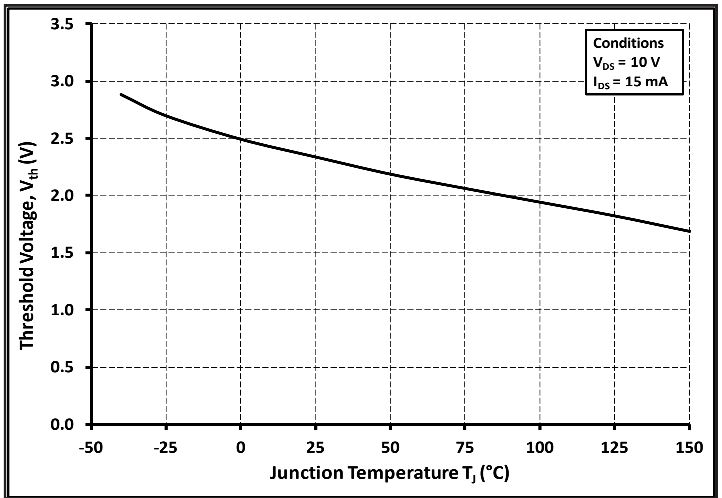


Figure 7. Threshold Voltage vs. Temperature

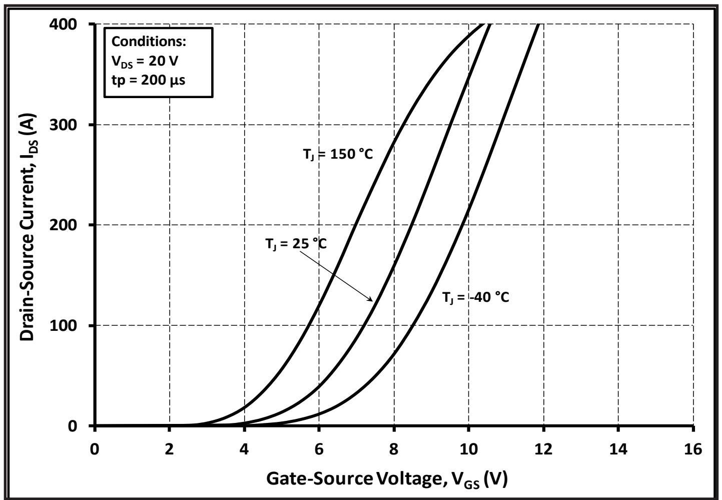


Figure 8. Transfer Characteristic for Various Junction Temperatures

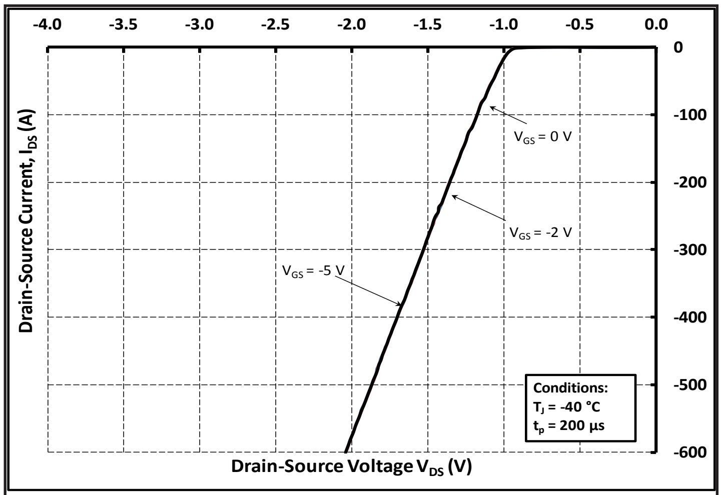


Figure 9. Diode Characteristic at -40 °C

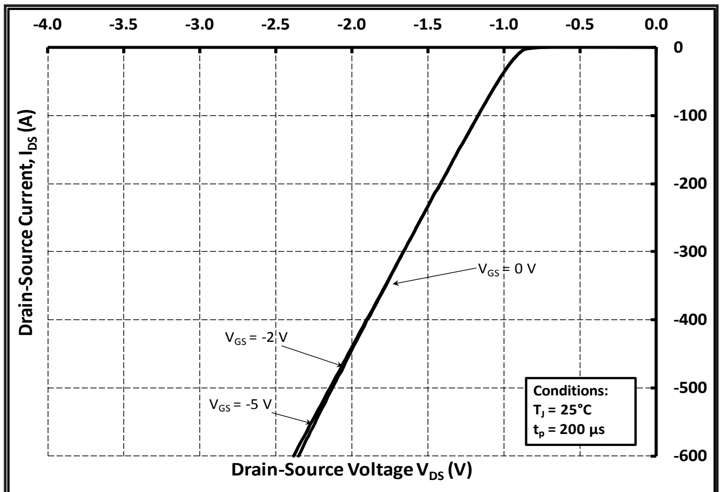


Figure 10. Diode Characteristic at 25 °C

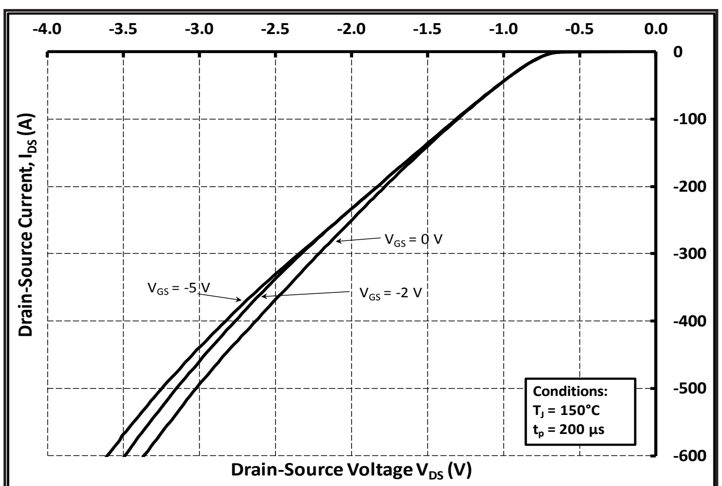


Figure 11. Diode Characteristic at 150 °C

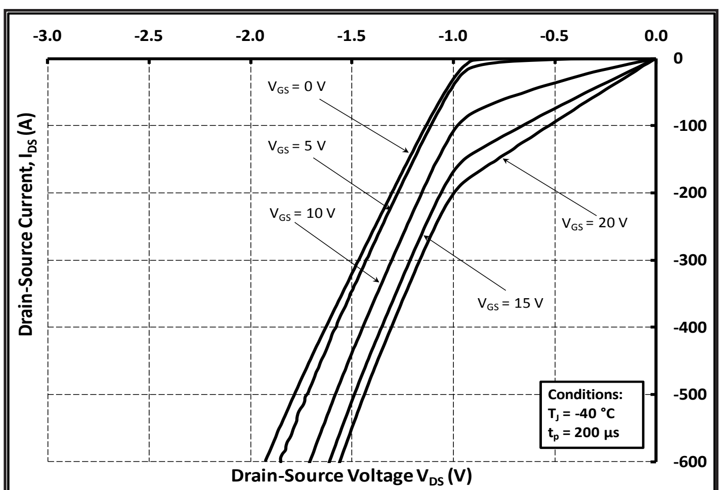


Figure 12. 3rd Quadrant Characteristic at -40 °C

Typical Performance

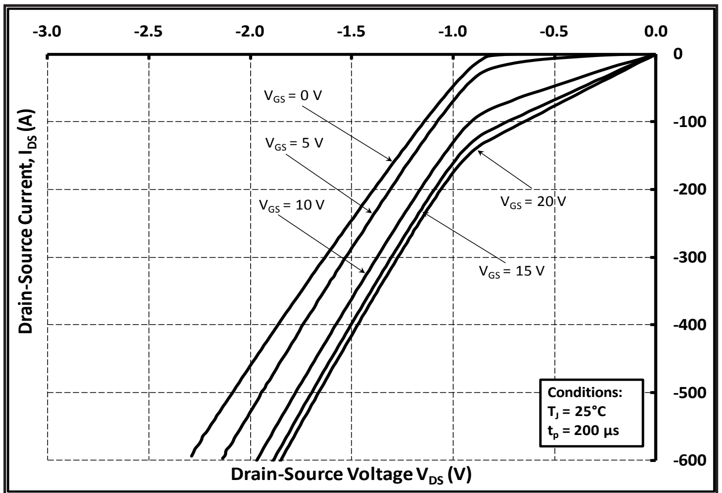


Figure 13. 3rd Quadrant Characteristic at 25 °C

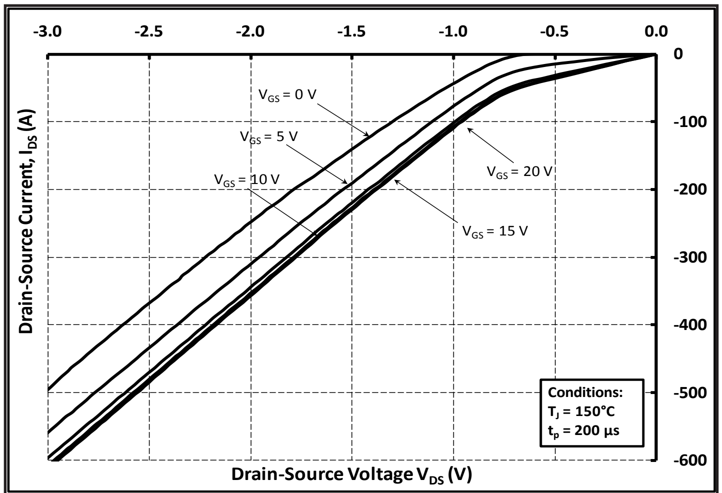


Figure 14. 3rd Quadrant Characteristic at 150 °C

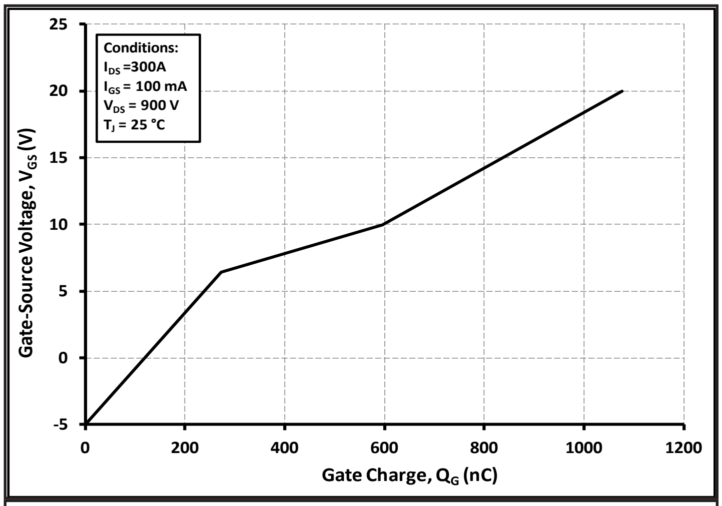


Figure 15. Gate Charge Characteristics

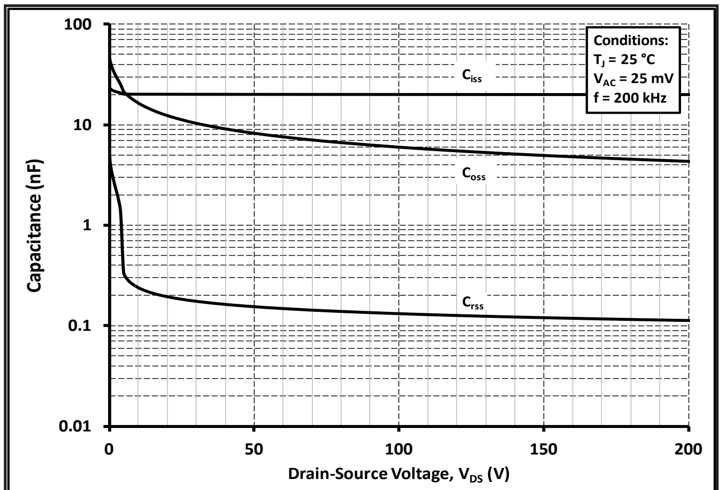


Figure 16. Capacitances vs. Drain-Source Voltage (0 - 200 V)

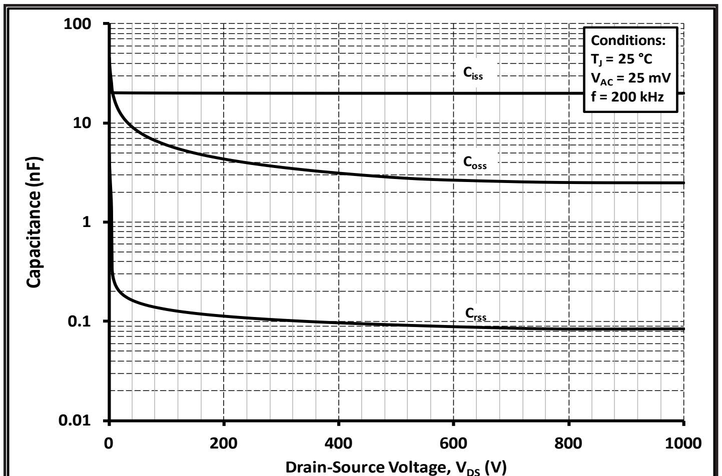


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 1 kV)

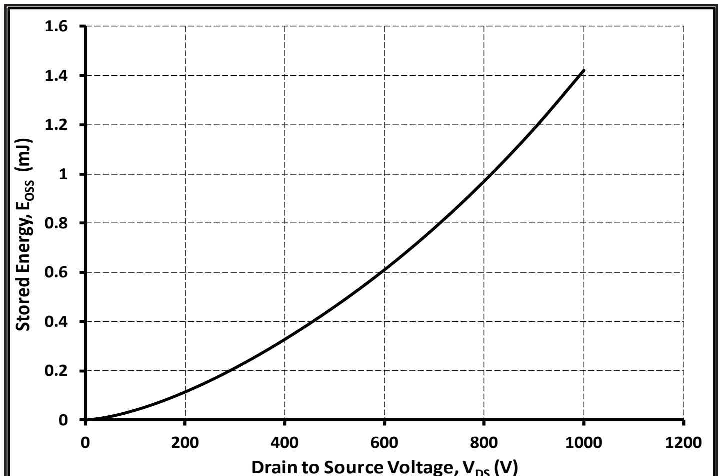


Figure 18. Output Capacitor Stored Energy

Typical Performance

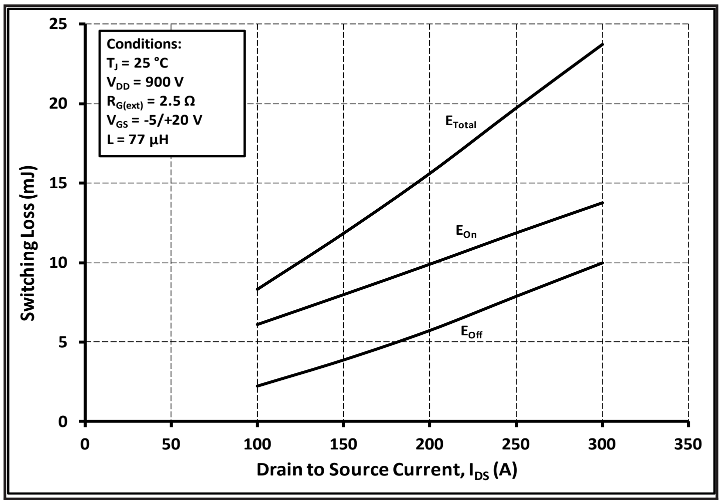


Figure 19. Inductive Switching Energy vs. Drain Current For V_{DS} = 900V, R_G = 2.5 Ω

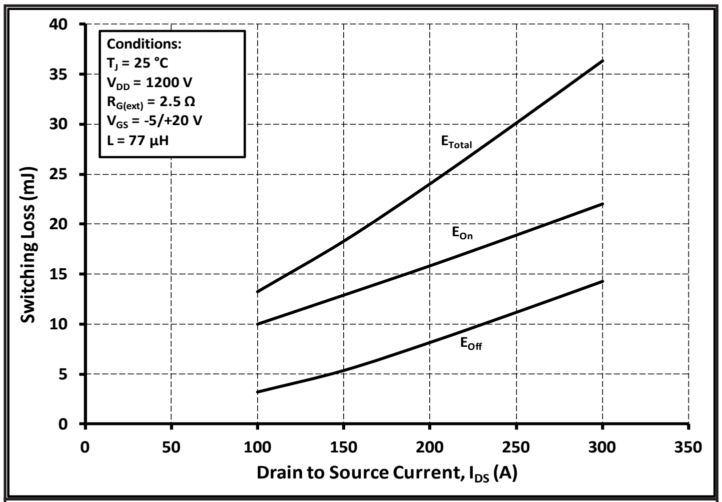


Figure 20. Inductive Switching Energy vs. Drain Current For V_{DS} = 1200 V, R_G = 2.5 Ω

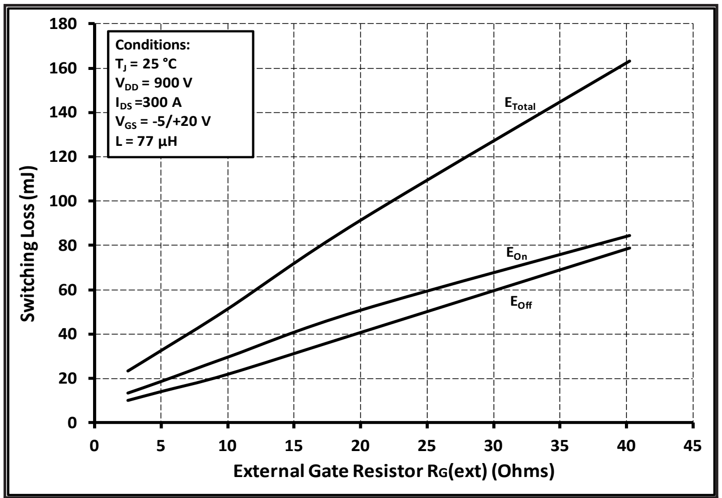


Figure 21. Inductive Switching Energy vs. $R_{G(ext)}$

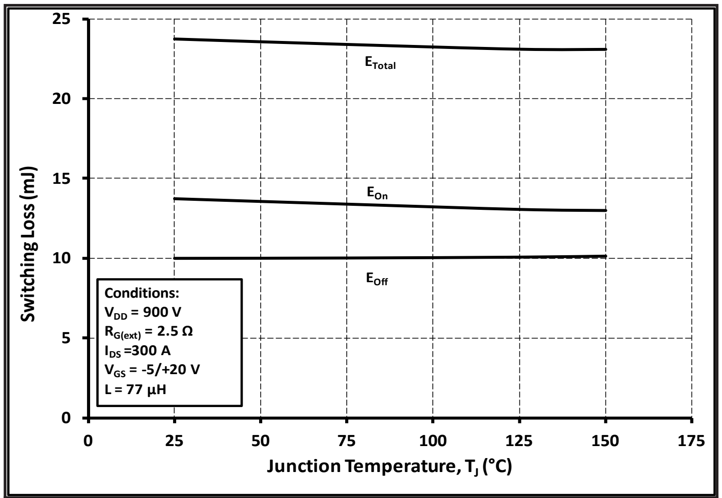


Figure 22. Inductive Switching Energy vs. Temperature

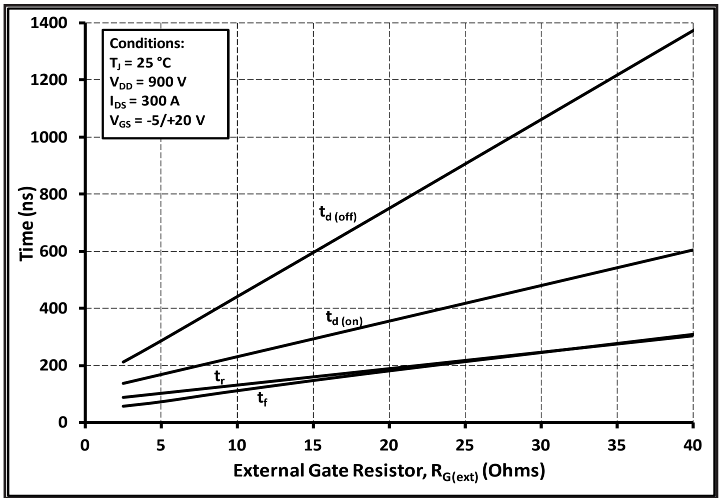


Figure 23. Timing vs. $R_{G(ext)}$

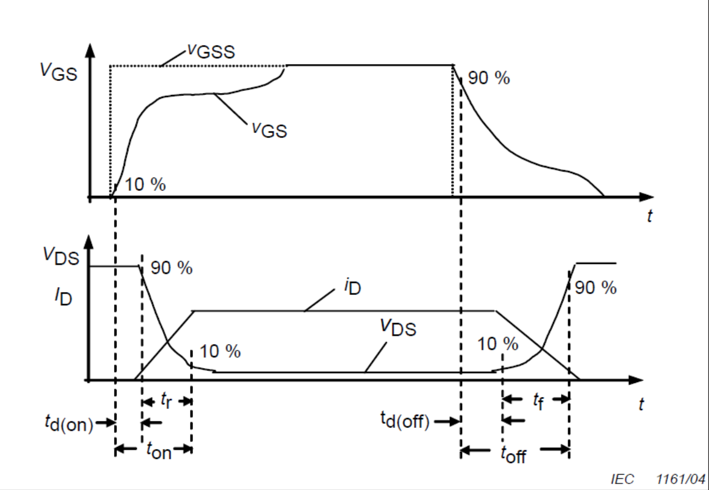


Figure 24. Resistive Switching Time Description

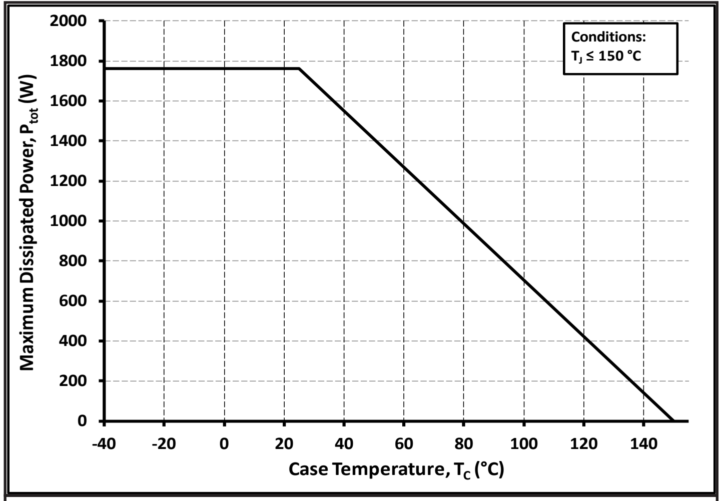


Figure 25. Maximum Power Dissipation (MOSFET) Derating vs. Case Temperature

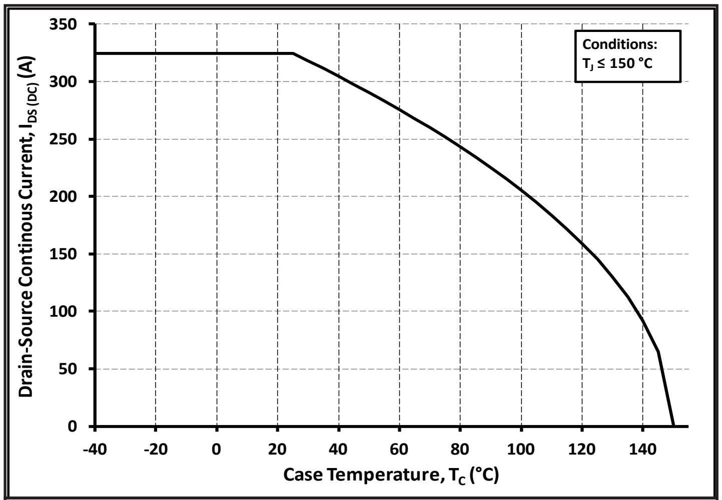


Figure 26. Continous Drain Current Derating vs Case Temperature

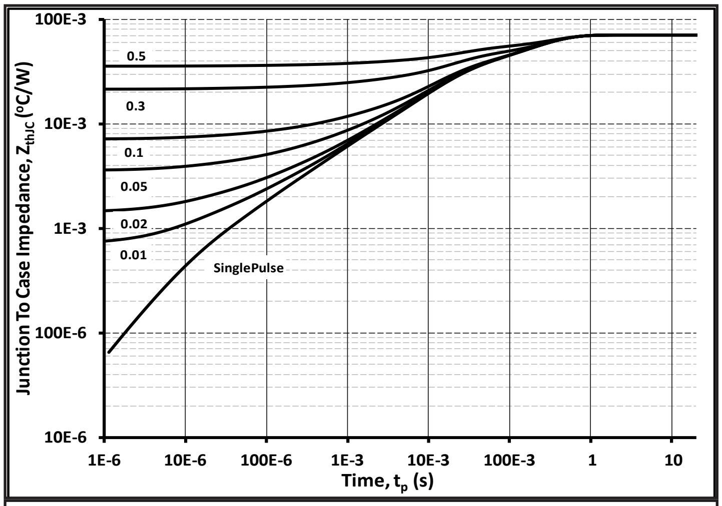


Figure 27. MOSFET Junction to Case Thermal Impedance

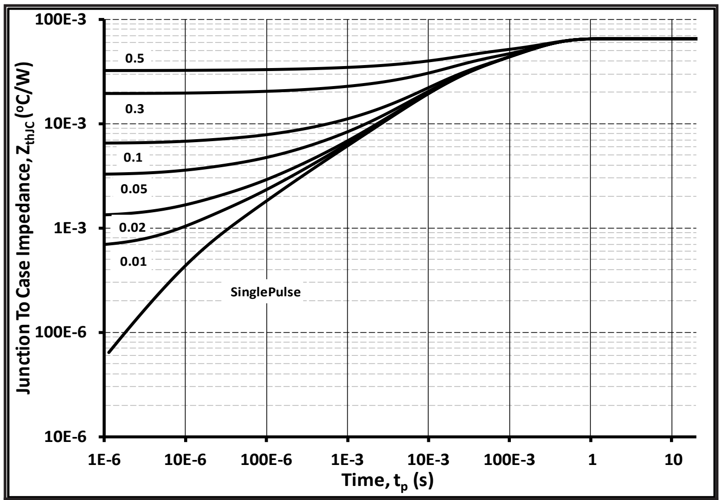


Figure 28. Diode Junction to Case Thermal Impedance

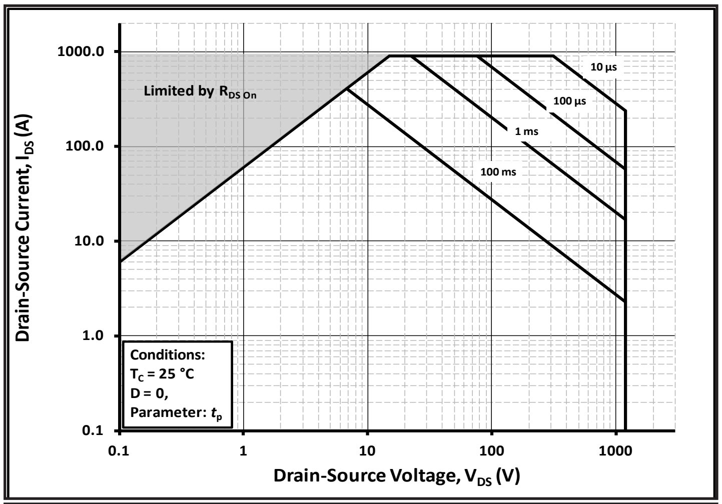
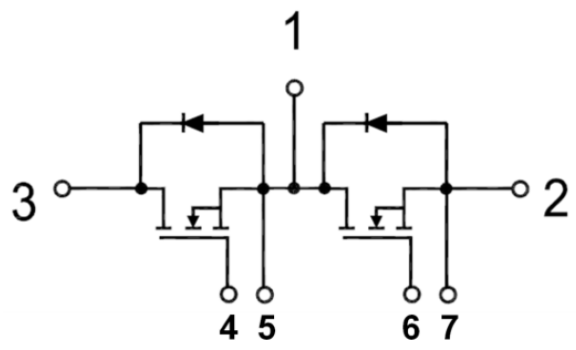
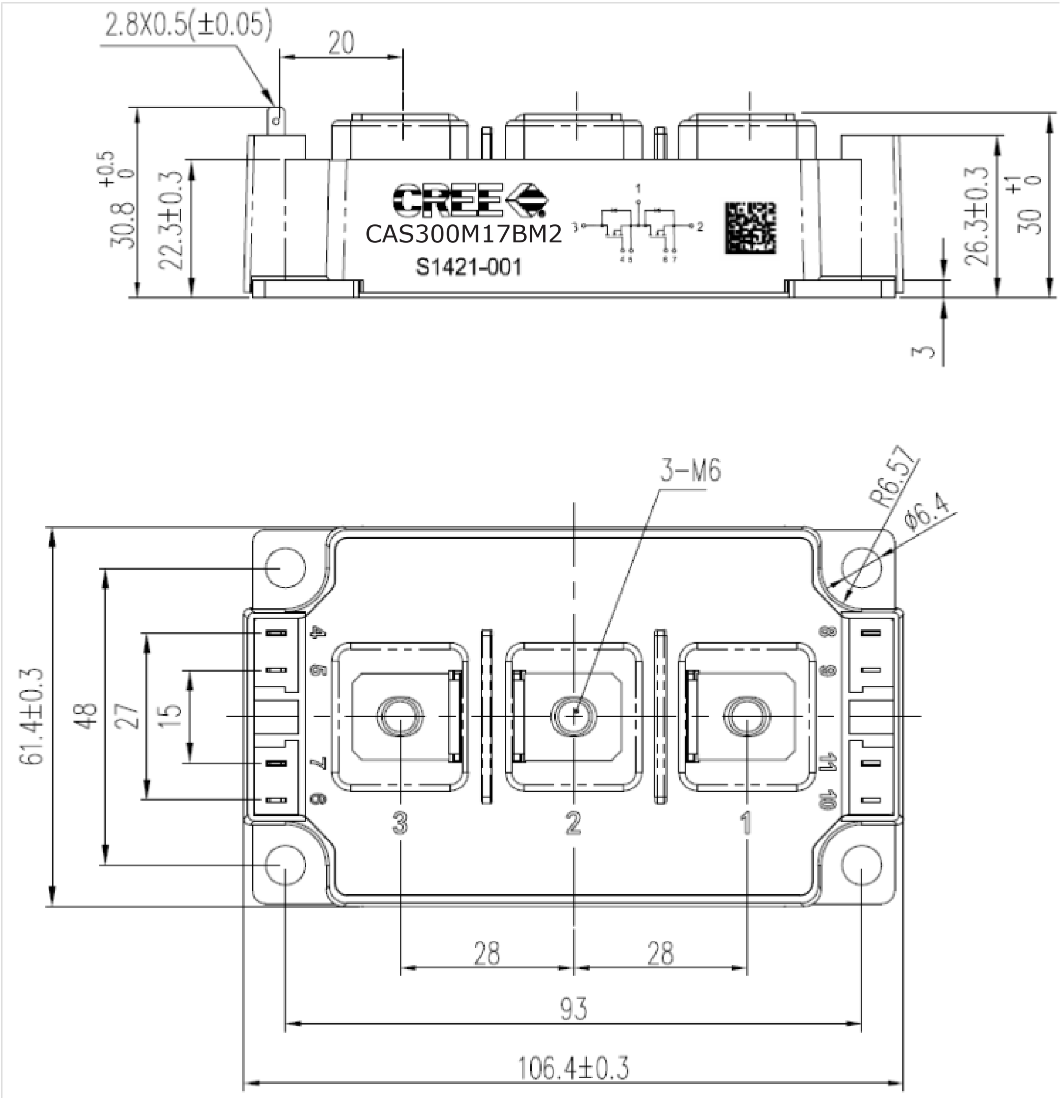


Figure 29. Maximum Power Dissipation (MOSFET) Derating vs. Case Temperature

Schematic



Package Dimensions (mm)



Notes

- **RoHS Compliance**
  The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS2), as implemented January 2, 2013. RoHS Declarations for this product can be obtained from your Cree representative or from the Product Documentation sections of www.cree.com.

- **REACh Compliance**
  REACh substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future,please contact a Cree representative to insure you get the most up-to-date REACh SVHC Declaration. REACh banned substance information (REACh Article 67) is also available upon request.

- This product has not been designed or tested for use in, and is not intended for use in, applications implanted into the human body nor in applications in which failure of the product could lead to death, personal injury or property damage, including but not limited to equipment used in the operation of nuclear facilities, life-support machines, cardiac defibrillators or similar emergency medical equipment, aircraft navigation or communication or control systems, air traffic control systems.

Module Application Note:

The SiC MOSFET module switches at speeds beyond what is customarily associated with IGBT based modules. Therefore, special precautions are required to realize the best performance. The interconnection between the gate driver and module housing needs to be as short as possible. This will afford the best switching time and avoid the potential for device oscillation. Also, great care is required to insure minimum inductance between the module and link capacitors to avoid excessive V_{DS} overshoots.

Please Refer to application note: Design Considerations when using Cree SiC Modules Part 1 and Part 2. [CPWR-AN12, CPWR-AN13]

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