

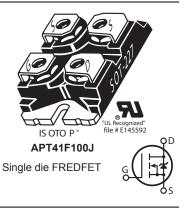


APT41F100J

1000V, 42A, 0.20Ω Max, t_{rr} ≤400ns

N-Channel FREDFET

Power MOS 8TM is a high speed, high voltage N-channel switch-mode power MOSFET. This 'FREDFET' version has a drain-source (body) diode that has been optimized for high reliability in ZVS phase shifted bridge and other circuits through reduced t_{rr} , soft recovery, and high recovery dv/dt capability. Low gate charge, high gain, and a greatly reduced ratio of C_{rss}/C_{iss} result in excellent noise immunity and low switching loss. The intrinsic gate resistance and capacitance of the poly-silicon gate structure help control di/dt during switching, resulting in low EMI and reliable paralleling, even when switching at very high frequency.



FEATURES

- Fast switching with low EMI
- Low t_{rr} for high reliability
- Ultra low C_{rss} for improved noise immunity
- Low gate charge
- Avalanche energy rated
- RoHS compliant

TYPICAL APPLICATIONS

- ZVS phase shifted and other full bridge
- Half bridge
- PFC and other boost converter
- Buck converter
- Single and two switch forward
- Flyback

Absolute Maximum Ratings Symbol Parameter Ratings Unit Continuous Drain Current @ T $_{C}$ = 25°C 42 I_D Continuous Drain Current @ T_C = 100°C 27 A I_{DM} Pulsed Drain Current^① 260 V_{GS} V Gate-Source Voltage ±30 E_{AS} 4075 Single Pulse Avalanche Energy ² mJ I_{AR} Avalanche Current, Repetitive or Non-Repetitive 33 A

Thermal and Mechanical Characteristics

Symbol	Characteristic	Min	Тур	Max	Unit	
P _D	Total Power Dissipation @ $T_{C} = 25^{\circ}C$			960	W	
R _{θJC}	Junction to Case Thermal Resistance			0.13 °C/W		
R _{ecs}	Case to Sink Thermal Resistance, Flat, Greased Surface		0.15		0/00	
T _J ,T _{STG}	Operating and Storage Junction Temperature Range	-55		150	°C	
V _{Isolation}	RMS Voltage (50-60hHz Sinusoidal Waveform from Terminals to Mounting Base for 1 Min.)	2500			V	
W _T	Package Weight		1.03		oz	
			29.2		g	
Torque	Terminele and Mounting Corours			10	in∙lbf	
	Terminals and Mounting Screws.			1.1	N∙m	

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Static Characteristics

T_J = 25°C unless otherwise specified

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Symbol	Parameter	Test Conditions		Min	Тур	Max	Unit
V _{BR(DSS)}	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_{D} = 250 \mu A$		1000			V
$\Delta V_{BR(DSS)} / \Delta T_{J}$	Breakdown Voltage Temperature Coefficient	Reference to 25°C, $I_D = 250\mu A$			1.15		V/°C
R _{DS(on)}	Drain-Source On Resistance ^③	V _{GS} = 10V, I _D = 33A			0.18	0.20	Ω
V _{GS(th)}	Gate-Source Threshold Voltage	- V _{GS} = V _{DS} , I _D = 5mA		2.5	4	5	V
$\Delta V_{GS(th)} / \Delta T_J$	Threshold Voltage Temperature Coefficient				-10		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 1000V	T _J = 25°C			250	μA
		$V_{GS} = 0V$	T _J = 125°C			1000	
I _{GSS}	Gate-Source Leakage Current	$V_{GS} = \pm 30V$				±100	nA

Dynamic Characteristics

T_J = 25°C unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Тур	Мах	Unit
9 _{fs}	Forward Transconductance	V _{DS} = 50V, I _D = 33A		75		S
C _{iss}	Input Capacitance			18500		
C _{rss}	Reverse Transfer Capacitance	$V_{GS} = 0V, V_{DS} = 25V$ f = 1MHz		245		
C _{oss}	Output Capacitance			1555		
C _{o(cr)} ④	Effective Output Capacitance, Charge Related			635		pF
C _{o(er)} ⑤	Effective Output Capacitance, Energy Related	$V_{GS} = 0V, V_{DS} = 0V \text{ to } 667V$		325		
Q _g	Total Gate Charge			570		
Q _{gs}	Gate-Source Charge	$V_{GS} = 0 \text{ to } 10V, I_{D} = 33A,$ $V_{DS} = 500V$		100		nC
Q _{gd}	Gate-Drain Charge	$v_{\rm DS} = 500v$		270		
t _{d(on)}	Turn-On Delay Time	Resistive Switching		55		
t _r	Current Rise Time	V _{DD} = 667V, I _D = 33A		55		
t _{d(off)}	Turn-Off Delay Time	$R_{G}^{}$ = 2.2Ω [®] , V _{GG} = 15V		235		ns
t _f	Current Fall Time	1		55		1

Source-Drain Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
۱ _s	Continuous Source Current (Body Diode)	showing the			42	A
I _{SM}	Pulsed Source Current (Body Diode) ^①	integral reverse p-n junction diode (body diode)	s		260	
V _{SD}	Diode Forward Voltage	I _{SD} = 33A, T _J = 25°C, V _{GS} = 0V			1.0	V
t _{rr}	Reverse Recovery Time	$T_{J} = 25^{\circ}C$			400 n 800 n	20
٢r		T _J = 125°C				115
Q _{rr}	Reverse Recovery Charge	$I_{SD} = 33A^{(3)}$ $T_{J} = 25^{\circ}C$		3.3		
<u> </u>		$V_{DD} = 100V$ $T_{J} = 125^{\circ}C$		8.0		μC
I _{rrm}	Reverse Recovery Current	$di_{SD}/dt = 100A/\mu s$ $T_J = 25^{\circ}C$		17.2	A	^
		T _J = 125°C		24.6		A
dv/dt	Peak Recovery dv/dt	$I_{SD} \le 33A$, di/dt $\le 1000A/\mu s$, $V_{DD} = 667V$, $T_{J} = 125^{\circ}C$			25	V/ns

(1) Repetitive Rating: Pulse width and case temperature limited by maximum junction temperature.

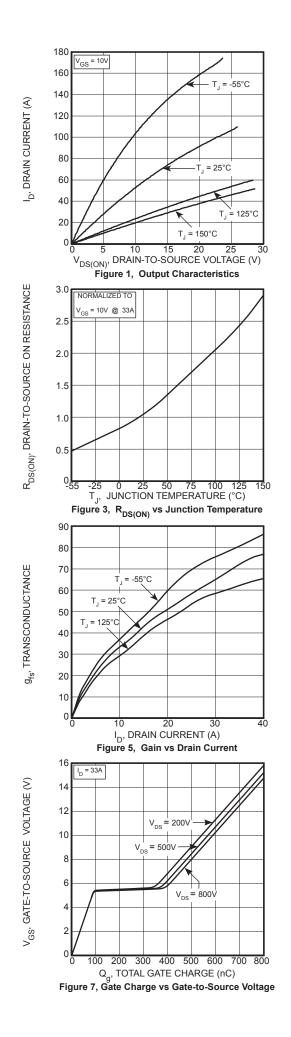
(2) Starting at $T_J = 25^{\circ}$ C, L = 7.48mH, $R_G = 25\Omega$, $I_{AS} = 33$ A.

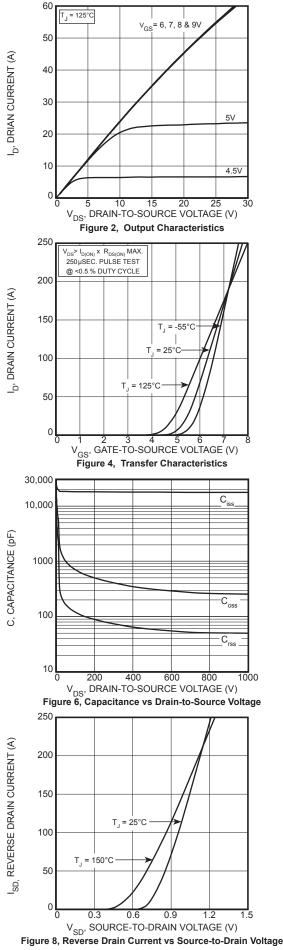
(3) Pulse test: Pulse Width < 380μ s, duty cycle < 2%.

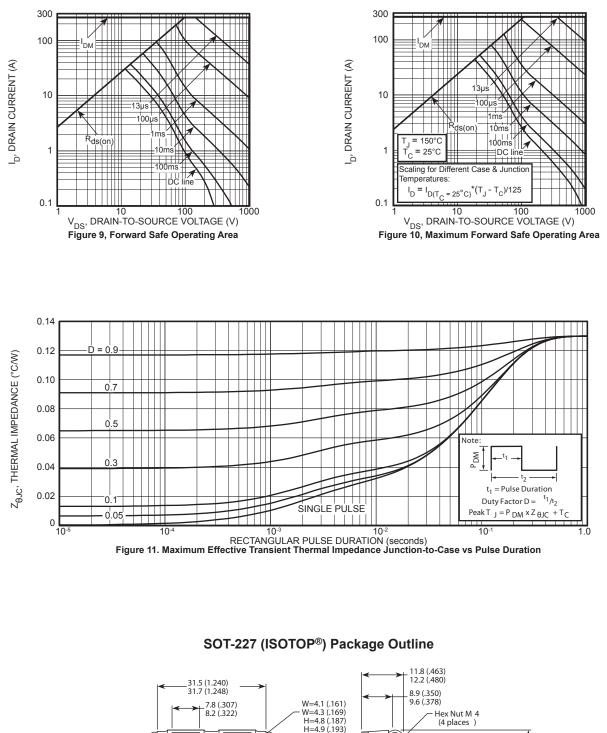
(4) C_{o(cr)} is defined as a fixed capacitance with the same stored charge as C_{OSS} with V_{DS} = 67% of V_{(BR)DSS}.
(5) C_{o(er)} is defined as a fixed capacitance with the same stored energy as C_{OSS} with V_{DS} = 67% of V_{(BR)DSS}. To calculate C_{o(er)} for any value of V_{DS} less than V_{(BR)DSS}, use this equation: C_{o(er)} = -5.37E-7/V_{DS}² + 9.48E-8/V_{DS} + 1.83E-10.

(6) R_G is external gate resistance, not including internal gate resistance or gate driver impedance. (MIC4452)

Microsemi reserves the right to change, without notice, the specifications and information contained herein.







r = 4.0 (.157)

(2 places)

-> 14.9 (.587)

15.1 (.594) 30.1 (1.185)

30.3 (1.193)

38.0 (1.496)

38.2 (1.504)



(4 places)

4.0 (.157) 4.2 (.165)

* Source

* Source

♠ (2 places)

3.3 (.129) 3.6 (.143)

25.2 (0.992) 25.4 (1.000)

1

12.6 (.496) 12.8 (.504)

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⁴ Emitter terminals are shorted internally. Current handling capability is equal for either Source terminal.

0.75 (.030)
0.85 (.033)

Drai n

Gate

F

1.95 (.077) 2.14 (.084)

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