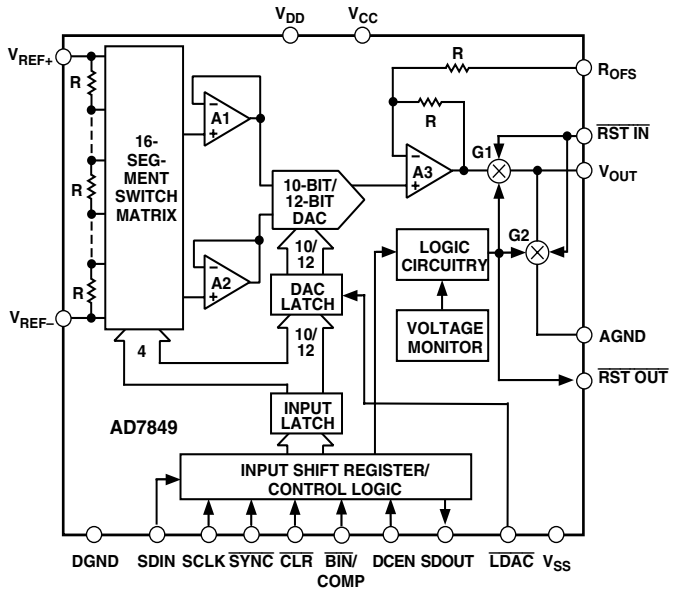
Serial Input, 14-Bit/16-Bit DAC

AD7849*

FEATURES
14-Bit/16-Bit Multiplying DAC
Guaranteed Monotonicity
Output Control on Power-Up and Power-Down
Internal or External Control
Versatile Serial Interface
DAC Clears to 0 V in Both Unipolar and Bipolar Output Ranges

APPLICATIONS
Industrial Process Control
PC Analog I/O Boards
Instrumentation

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7849 is a 14-bit/16-bit serial input multiplying DAC. The DAC architecture ensures excellent differential linearity performance, and monotonicity is guaranteed to 14 bits for the A grade and to 16 bits for all other grades over the specified temperature ranges.

During power-up and power-down sequences (when the supply voltages are changing), the V_{OUT} pin is clamped to 0 V via a low impedance path. To prevent the output of A3 being shorted to 0 V during this time, transmission gate G1 is also opened. These conditions are maintained until the power supplies stabilize and a valid word is written to the DAC register. At this time, G2 opens and G1 closes. Both transmission gates are also externally controllable via the Reset In ($\overline{RST\ IN}$) control input. For instance, if the $\overline{RST\ IN}$ input is driven from a battery supervisor chip, then on power-off or during a brown out, the $\overline{RST\ IN}$ input will be driven low to open G1 and close G2. The DAC must be reloaded, with $\overline{RST\ IN}$ high, to re-enable the output. Conversely, the on-chip voltage detector output ($\overline{RST\ OUT}$) is also available to the user to control other parts of the system.

The AD7849 has a versatile serial interface structure and can be controlled over three lines to facilitate opto-isolator applications.

SDOUT is the output of the on-chip shift register and can be used in a daisy-chain fashion to program devices in the multi-channel system. The DCEN (Daisy Chain Enable) input controls this function.

The $\overline{BIN}$/COMP pin sets the DAC coding; with $\overline{BIN}$/COMP set to 0, the coding is straight binary; and with it set to 1, the coding is 2s complement. This allows the user to reset the DAC to 0 V in both the unipolar and bipolar output ranges.

The part is available in a 20-lead DIP and 20-lead SOIC package.

*Protected by U.S. Patent No. 5,319,371.

REV. B

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AD7849–SPECIFICATIONS[1]

(V_{DD} = +14.25 V to +15.75 V; V_{SS} = –14.25 V to –15.75 V; V_{CC} = +4.75 V to +5.25 V; V_{OUT} loaded with 2 kΩ,[2] 200 pF to 0 V; V_{REF+} = +5 V; R_{OFS} connected to 0 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

Parameter	A Versions	B, T Versions	C Versions	Units	Test Conditions/Comments
RESOLUTION	14	16	16	Bits	A Versions: 1 LSB = 2 (V_{REF+}–V_{REF-})/2^{14} B, C, T Versions: 1 LSB = 2 (V_{REF+}–V_{REF-})/2^{16}
UNIPOLAR OUTPUT					V_{REF-} = 0 V, V_{OUT} = 0 V to +10 V
Relative Accuracy @ +25°C	±4	±6	±4	LSBs typ	
T_{MIN} to T_{MAX}	±5	±16	±8	LSBs max	
Differential Nonlinearity	±0.25	±0.9	±0.5	LSBs max	All Grades Guaranteed Monotonic Over Temperature
Gain Error @ +25°C	±1	±4	±4	LSBs typ	V_{OUT} Load = 10 MΩ
T_{MIN} to T_{MAX}	±4	±16	±16	LSBs max	
Offset Error @ +25°C	±1	±4	±4	LSBs typ	
T_{MIN} to T_{MAX}	±6	±24	±16	LSBs max	
Gain TC[3]	±2	±2	±2	ppm FSR/°C typ	
Offset TC[3]	±2	±2	±2	ppm FSR/°C typ	
BIPOLAR OUTPUT					V_{REF-} = –5 V, V_{OUT} = –10 V to +10 V
Relative Accuracy @ +25°C	±2	±3	±2	LSBs typ	
T_{MIN} to T_{MAX}	±3	±8	±4	LSBs max	
Differential Nonlinearity	±0.25	±0.9	±0.5	LSBs max	All Grades Guaranteed Monotonic Over Temperature
Gain Error @ +25°C	±1	±4	±4	LSBs typ	V_{OUT} Load = 10 MΩ
T_{MIN} to T_{MAX}	±4	±16	±16	LSBs max	
Offset Error @ +25°C	±0.5	±2	±2	LSBs typ	
T_{MIN} to T_{MAX}	±3	±12	±8	LSBs max	
Bipolar Zero Error @ +25°C	±0.5	±2	±2	LSBs typ	
T_{MIN} to T_{MAX}	±4	±12	±8	LSBs max	
Gain TC[3]	±2	±2	±2	ppm FSR/°C typ	
Offset TC[3]	±2	±2	±2	ppm FSR/°C typ	
Bipolar Zero TC[3]	±2	±2	±2	ppm FSR/°C typ	
REFERENCE INPUT					
Input Resistance	25	25	25	kΩ min	Resistance from V_{REF+} to V_{REF-}
	43	43	43	kΩ max	Typically 34 kΩ
V_{REF+} Range	V_{SS} + 6 to V_{DD} – 6	V_{SS} + 6 to V_{DD} – 6	V_{SS} + 6 to V_{DD} – 6	Volts	
V_{REF-} Range	V_{SS} + 6 to V_{DD} – 6	V_{SS} + 6 to V_{DD} – 6	V_{SS} + 6 to V_{DD} – 6	Volts	
OUTPUT CHARACTERISTICS					
Output Voltage Swing	V_{SS} + 4 to V_{DD} – 4	V_{SS} + 4 to V_{DD} – 4	V_{SS} + 4 to V_{DD} – 4	V max	
Resistive Load	2	2	2	kΩ min	To 0 V
Capacitive Load	200	200	200	pF max	To 0 V
Output Resistance	0.3	0.3	0.3	Ω typ	
Short Circuit Current	±25	±25	±25	mA typ	Voltage Range: –10 V to +10 V
DIGITAL INPUTS					
V_{INH}, Input High Voltage	2.4	2.4	2.4	V min	
V_{INL}, Input Low Voltage	0.8	0.8	0.8	V max	
I_{INH}, Input Current	±10	±10	±10	µA max	
C_{IN}, Input Capacitance	10	10	10	pF max	
DIGITAL OUTPUTS					
V_{OL} (Output Low Voltage)	0.4	0.4	0.4	Volts max	I_{SINK} = 1.6 mA
V_{OH} (Output High Voltage)	4.0	4.0	4.0	Volts min	I_{SOURCE} = 400 µA
Floating State Leakage Current	±10	±10	±10	µA max	
Floating State Output Capacitance	10	10	10	pF max	
POWER REQUIREMENTS[4]					
V_{DD}	+14.25/+15.75	+14.25/+15.75	+14.25/+15.75	V min/V max	
V_{SS}	–14.25/–15.75	–14.25/–15.75	–14.25/–15.75	V min/V max	
V_{CC}	+4.75/+5.25	+4.75/+5.25	+4.75/+5.25	V min/V max	
I_{DD}	5	5	5	mA max	V_{OUT} Unloaded, V_{INH} = V_{DD} – 0.1 V, V_{INL} = 0.1 V
I_{SS}	5	5	5	mA max	V_{OUT} Unloaded, V_{INH} = V_{DD} – 0.1 V, V_{INL} = 0.1 V
I_{CC}	2.5	2.5	2.5	mA max	V_{INH} = V_{DD} – 0.1 V, V_{INL} = 0.1 V
Power Supply Sensitivity[5]	0.4	1.5	1.5	LSB/V max	
Power Dissipation	100	100	100	mW typ	V_{OUT} Unloaded

NOTES
[1]Temperature ranges: A, B, C Versions: –40°C to +85°C; T Version: –55°C to +125°C.
[2]Minimum load for T Version is 3 kΩ.
[3]Guaranteed by design and characterization, not production tested.
[4]The AD7849 is functional with power supplies of ±12 V. See Typical Performance Curves.
[5]Sensitivity of Gain Error, Offset Error and Bipolar Zero Error to V_{DD}, V_{SS} variations.
Specifications subject to change without notice.

RESET SPECIFICATIONS (These specifications apply when the device goes into the Reset mode during a power-up or power-down sequence.) V_{OUT} unloaded.

Parameter	All Versions	Units	Test Conditions/Comments
V_A[1], Low Threshold Voltage for V_{DD}, V_{SS}	1.2	Volt max	This is the lower V_{DD}/V_{SS} threshold voltage for the reset
	0	Volts typ	function. Above this, the reset is activated.
V_B, High Threshold Voltage for V_{DD}, V_{SS}	9.5	Volts max	This is the higher V_{DD}/V_{SS} threshold voltage for the reset
	6.4	Volts min	function. Below this, the reset is activated. Typically 8 volts.
V_C, Low Threshold Voltage for V_{CC}	1	Volt max	This is the lower threshold voltage for the reset function.
	0	Volts typ	Above this, the reset is activated.
V_D, High Threshold Voltage for V_{CC}	4	Volts max	This is the higher V_{CC} threshold voltage for the reset function.
	2.5	Volts min	Below this, the reset is activated. Typically 3 volts.
G2 R_{ON}	1	kΩ typ	On Resistance of G2; V_{DD} = 2 V; V_{SS} = –2 V; I_{G2} = 1 mA.

NOTES
[1]A pull-down resistor (65 kΩ) on V_{OUT} maintains 0 V output when V_{DD}/V_{SS} is below V_A.
Specifications subject to change without notice.

AC PERFORMANCE CHARACTERISTICS (These characteristics are included for Design Guidance and are not subject to test. (V_{REF+} = +5 V; V_{DD} = +14.25 V to +15.75 V; V_{SS} = –14.25 V to –15.75 V; V_{CC} = +4.75 V to +5.25 V; R_{OFS} connected to 0 V.)

Parameter	T Version	A, B, C Versions	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE				
Output Settling Time[1]	7	7	µs typ	To 0.006% FSR. V_{OUT} Loaded. V_{REF-} = 0 V.
	10	10	µs typ	To 0.003% FSR. V_{OUT} Loaded. V_{REF-} = –5 V.
Slew Rate	4	4	V/µs typ	
Digital-to-Analog Glitch Impulse	250	250	nV-s typ	DAC Alternately Loaded with 00 . . . 00 and 111 . . . 11. V_{OUT} Unloaded. $\overline{LDAC}$ Permanently Low. $\overline{BIN}$/COMP Set to 1. V_{REF-} = –5 V.
	150	150	nV-s typ	$\overline{LDAC}$ Frequency = 100 kHz
AC Feedthrough	1	1	mV pk-pk typ	V_{REF-} = 0 V, V_{REF+} = 1 V rms, 10 kHz Sine Wave. DAC Loaded with All 0s. $\overline{BIN}$/COMP Set to 0.
Digital Feedthrough	5	5	nV-s typ	DAC Alternately Loaded with All 1s and All 0s. $\overline{SYNC}$ High.
Output Noise Voltage Density 1 kHz–100 kHz	80	80	nV/√Hz typ	Measured at V_{OUT}. V_{REF+} = V_{REF-} = 0 V. $\overline{BIN}$/COMP Set to 0.

NOTES
[1]$\overline{LDAC}$ = 0. Settling time does not include deglitching time of 5 µs (typ).
Specification subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +14.25 V to +15.75 V; V_{SS} = –14.25 V to –15.75 V; V_{CC} = +4.75 V to +5.25 V; R_L = 2 kΩ, C_L = 200 pF. All Specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Limit at +25°C (All Versions)	Limit at T_{MIN}, T_{MAX} (All Versions)	Units	Conditions/Comments
t_1[3]	200	200	ns min	SCLK Cycle Time
t_2	50	50	ns min	$\overline{SYNC}$ to SCLK Setup Time
t_3	70	70	ns min	$\overline{SYNC}$ to SCLK Hold Time
t_4	10	10	ns min	Data Setup Time
t_5	40	40	ns min	Data Hold Time
t_6[4]	80	80	ns max	SCLK Falling Edge to SDO Valid
t_7	80	80	ns min	$\overline{LDAC}$, $\overline{CLR}$ Pulsewidth
t_r	30	30	µs max	Digital Input Rise Time
t_f	30	30	µs max	Digital Input Fall Time

NOTES
[1]Guaranteed by characterization.
[2]All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[3]SCLK mark/space ratio range is 40/60 to 60/40.
[4]SDO load capacitance is 50 pF.
Specification subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

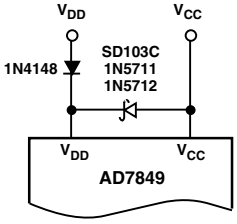
(T_A = +25°C unless otherwise noted)

V_{DD} to DGND . . . . . –0.4 V to +17 V
V_{CC} to DGND[2] . . . . . –0.4 V, V_{DD} + 0.4 V or +7 V (Whichever Is Lower)
V_{SS} to DGND . . . . . –0.4 V to –17 V
V_{REF+} to DGND . . . . . V_{DD} + 0.4 V, V_{SS} – 0.4 V
$V_{REF–}$ to DGND . . . . . V_{DD} + 0.4 V, V_{SS} – 0.4 V
V_{OUT} to DGND[3] . . . . . V_{DD} + 0.4 V, V_{SS} – 0.4 V or ±10 V (Whichever Is Lower)
R_{OFS} to DGND . . . . . V_{DD} + 0.4 V, V_{SS} – 0.4 V
Digital Input Voltage to DGND . . . . . –0.4 V to V_{CC} + 0.4 V
Input Current to any Pin Except Supplies[4] . . . . . ±10 mA
Operating Temperature Range
  Commercial/Industrial (A, B, C Versions). . . . –40°C to +85°C
  Extended (T Version) . . . . . –55°C to +125°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . +150°C
Plastic DIP Package, Power Dissipation . . . . . 875 mW
  θ_{JA} Thermal Impedance . . . . . 102°C/W
  Lead Temperature (Soldering, 10 secs) . . . . . +260°C
SOP Package, Power Dissipation . . . . . 875 mW
  θ_{JA} Thermal Impedance . . . . . 74°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 secs) . . . . . +215°C
    Infrared (15 secs) . . . . . +220°C
Cerdip Package, Power Dissipation . . . . . 875 mW
  θ_{JA} Thermal Impedance . . . . . 71°C/W
  Lead Temperature, Soldering (Soldering 10 secs) . . . 260°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]V_{CC} must not exceed V_{DD} by more than 0.4 V. If it is possible for this to happen during power-up or power-down (for example, if V_{CC} is greater than +0.4 V while V_{DD} is still 0 V), the following diode protection scheme will ensure protection.



[3]V_{OUT} may be shorted to DGND, +10 V, –10 V, provided that the power dissipation of the package is not exceeded.

[4]Transient currents of up to 100 mA will not cause SCR latch-up.

CAUTION

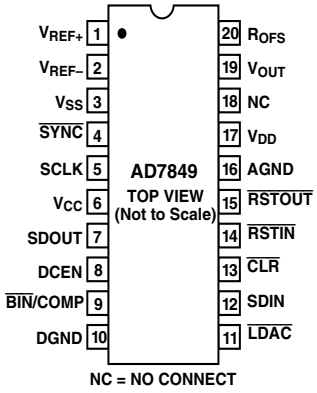
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7849 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Model	Temperature Range	Resolution (Bits)	Bipolar INL (LSBs)	Package Option*
AD7849AN	–40°C to +85°C	14	±3	N-20
AD7849BN	–40°C to +85°C	16	±8	N-20
AD7849CN	–40°C to +85°C	16	±4	N-20
AD7849AR	–40°C to +85°C	14	±3	R-20
AD7849BR	–40°C to +85°C	16	±8	R-20
AD7849CR	–40°C to +85°C	16	±4	R-20
AD7849TQ	–55°C to +125°C	16	±8	Q-20

*N = Plastic DIP; R = SOP (Small Outline Package); Q = Cerdip.

PIN CONFIGURATION



NC = NO CONNECT

TERMINOLOGY

Least Significant Bit
This is the analog weighting of 1 bit of the digital word in a DAC. For the AD7849, B, C and T versions, 1 LSB = $(V_{REF+} - V_{REF-})/2^{16}$. For the AD7849, A version, 1 LSB = $(V_{REF+} - V_{REF-})/2^{14}$.

Relative Accuracy
Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for both endpoints (i.e., offset and gain errors are adjusted out) and is normally expressed in least significant bits or as a percentage of full-scale range.

Differential Nonlinearity
Differential nonlinearity is the difference between the measured change and the ideal change between any two adjacent codes. A specified differential nonlinearity of less than ±1 LSB over the operating temperature range ensures monotonicity.

Gain Error
Gain error is a measure of the output error between an ideal DAC and the actual device output with all 1s loaded after offset error has been adjusted out. Gain error is adjustable to zero with an external potentiometer.

Offset Error
This is the error present at the device output with all 0s loaded in the DAC. It is due to op amp input offset voltage and bias current and the DAC leakage current.

Bipolar Zero Error
When the AD7849 is connected for bipolar output and (100 . . . 000) is loaded to the DAC, the deviation of the analog output from the ideal midscale of 0 V, is called the bipolar zero error.

Digital-to-Analog Glitch Impulse
This is the amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in nV-secs.

Multiplying Feedthrough Error
This is an ac error due to capacitive feedthrough from either of the V_{REF} terminals to V_{OUT} when the DAC is loaded with all 0s.

Digital Feedthrough
When the DAC is not selected ($\overline{SYNC}$ is held high), high frequency logic activity on the digital inputs is capacitively coupled through the device to show up as noise on the V_{OUT} pin. This noise is digital feedthrough.

PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	V_{REF+}	V_{REF+} Input. The DAC is specified for V_{REF+} of +5 V. The DAC is fully multiplying so that the V_{REF+} range is +5 V to –5 V.
2	V_{REF-}	V_{REF-} Input. The DAC is specified for V_{REF-} of –5 V. Since the DAC is fully multiplying the V_{REF-} range is –5 V to +5 V.
3	V_{SS}	Negative supply for the analog circuitry. This is nominally –15 V.
4	$\overline{SYNC}$	Data Synchronization Logic Input. When it goes low, the internal logic is initialized in readiness for a new data word.
5	SCLK	Serial Clock Logic Input. Data is clocked into the input register on each SCLK falling edge.
6	V_{CC}	Positive supply for the digital circuitry. This is nominally +5 V.
7	SDOUT	Serial Data Output. With DCEN at Logic "1," this output is enabled and the serial data in the input shift register is clocked out on each rising edge of SCLK.
8	DCEN	Daisy-Chain Enable Logic Input. Connect this pin high if a daisy-chain interface is being used, otherwise this pin must be connect low.
9	$\overline{BIN}$/COMP	Logic Input. This input selects the data format to be either binary or 2s complement. In the unipolar output range, natural binary format is selected by connecting the input to a Logic "0." In the bipolar output range, offset binary is selected by connecting this input to a Logic "0" and 2s complement is selected by connecting it to a Logic "1."
10	DGND	Digital Ground. Ground reference point for the on-chip digital circuitry.
11	$\overline{LDAC}$	Load DAC Logic Input. This input updates the DAC output. The DAC output is updated on the falling edge of this signal or alternatively, if this input is permanently low, an automatic update mode is selected whereby the DAC is updated on the 16th falling SCLK edge.
12	SDIN	Serial Data Input. The 16-bit serial data word is applied to this input.
13	$\overline{CLR}$	Clear Logic Input. Taking this input low sets V_{OUT} to 0 V in both the unipolar output range and the bipolar 2s complement output range. It sets V_{OUT} to V_{REF-} in the offset binary bipolar output range.
14	$\overline{RSTIN}$	Reset Logic Input. This input allows external access to the internal reset logic. Applying a Logic "0" to this input, resets the DAC output to 0 V. In normal operation it should be tied to Logic "1."
15	$\overline{RSTOUT}$	Reset Logic Output. This is the output from the on-chip voltage monitor used in the reset circuit. It may used to control other system components if desired.
16	AGND	This is the analog ground for the device. It is the point to which the output gets shorted in the reset mode.
17	V_{DD}	Positive supply for the analog circuitry. This is +15 V nominal.
18	NC	No Connect. Leave unconnected.
19	V_{OUT}	DAC Output Voltage Pin.
20	R_{OFS}	Input to summing resistor of DAC output amplifier. This is used to select output voltage ranges. See Figures 16 to 19 in "APPLYING THE AD7849."

Typical Performance Curves

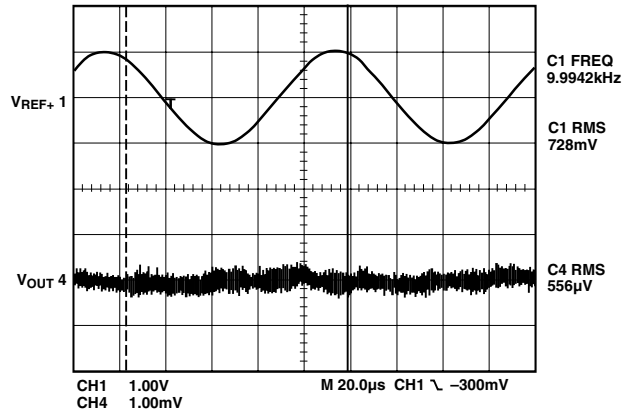


Figure 1a. AC Feedthrough

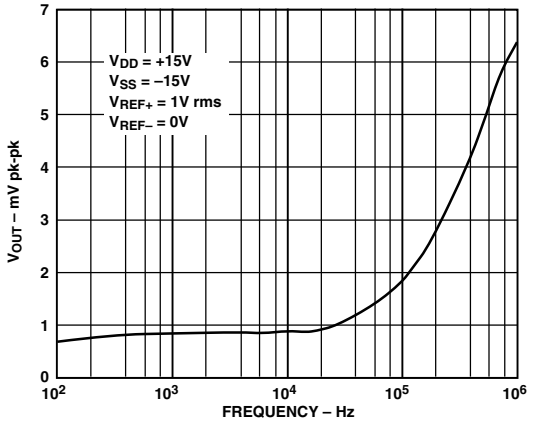


Figure 1b. AC Feedthrough vs. Frequency

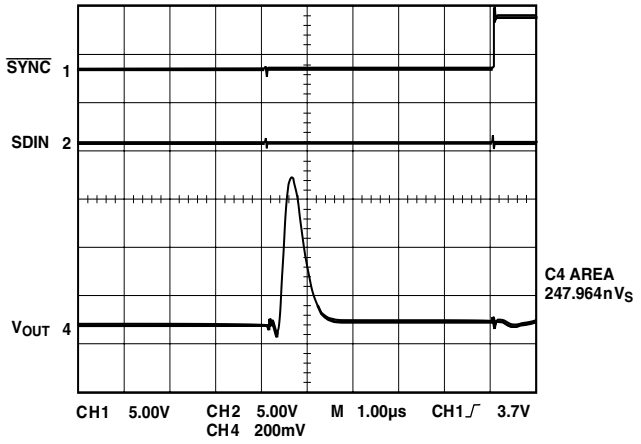


Figure 2a. Digital-to-Analog Glitch Impulse Without Internal Deglitcher

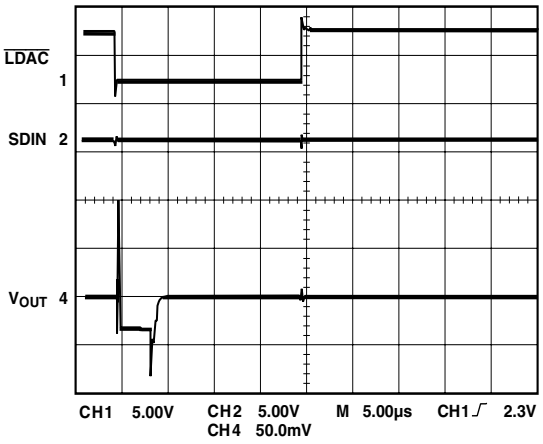


Figure 2b. Digital-to-Analog Glitch Impulse with Internal Deglitcher

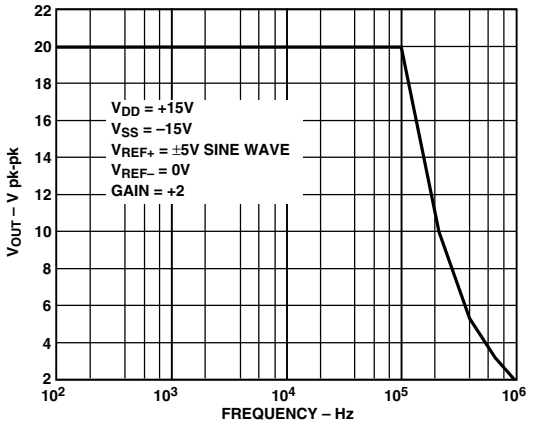


Figure 3. Large Signal Frequency Response

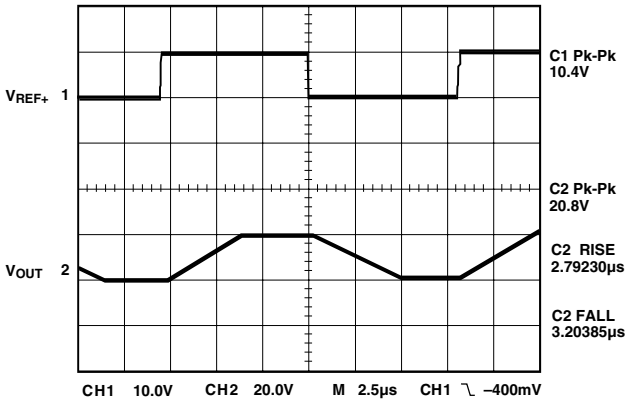


Figure 4. Pulse Response (Large Signal)

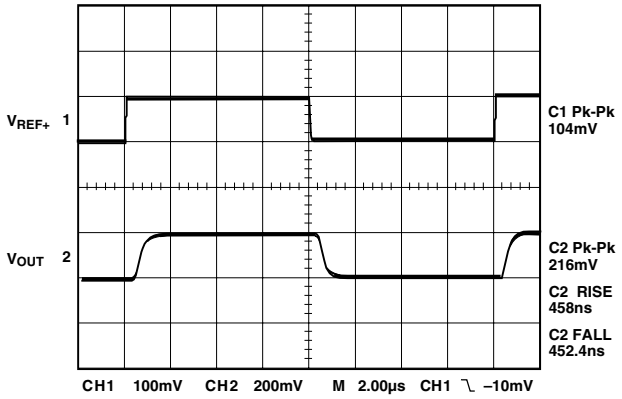


Figure 5. Pulse Response (Small Signal)

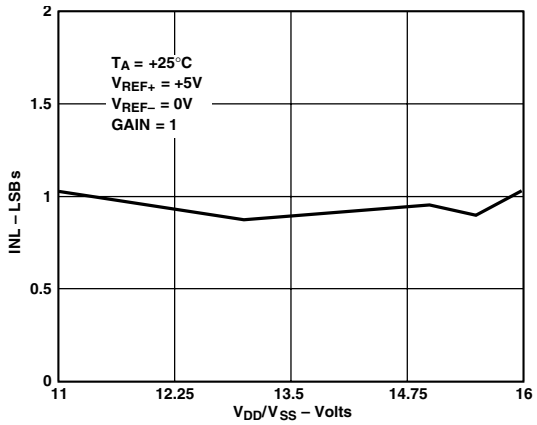


Figure 6. Typical Integral Nonlinearity vs. Supplies

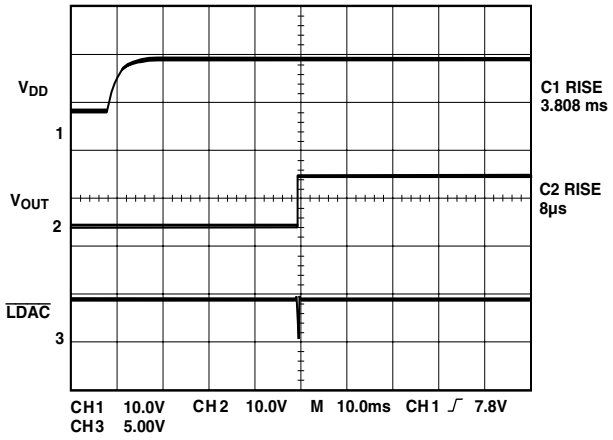


Figure 8. Turn-On Characteristics

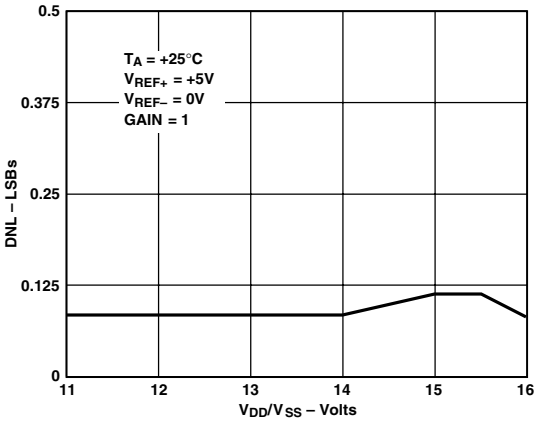


Figure 7. Typical Differential Nonlinearity vs. Supplies

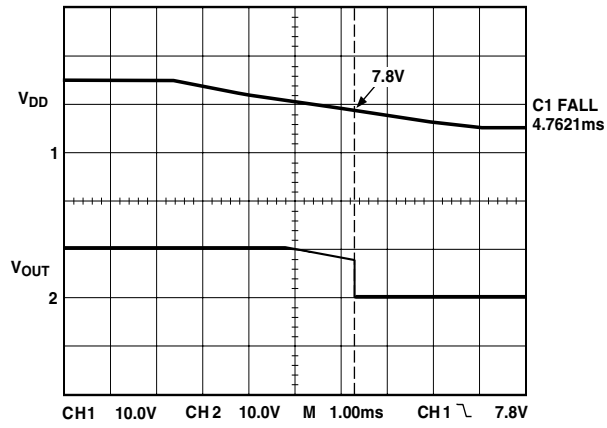


Figure 9. Turn-Off Characteristics

CIRCUIT DESCRIPTION

D/A CONVERSION

Figure 10 shows the D/A section of the AD7849. There are three on-chip DACs each of which has its own buffer amplifier. DAC1 and DAC2 are 4-bit DACs. They share a 16-resistor string but have their own analog multiplexers. The voltage reference is applied to the resistor string. DAC3 is a 12-bit voltage mode DAC with its own output stage.

The 4 MSBs of the 16-bit digital input code drive DAC1 and DAC2 while the 12 LSBs control DAC3. Using DAC1 and DAC2, the MSBs select a pair of adjacent nodes on the resistor string and present that voltage to the positive and negative inputs of DAC3. This DAC interpolates between these two voltages to produce the analog output voltage.

To prevent nonmonotonicity in the DAC due to amplifier offset voltages, DAC1 and DAC2 "leap-frog" along the resistor string. For example, when switching from Segment 1 to Segment 2, DAC1 switches from the bottom of Segment 1 to the top of Segment 2 while DAC 2 remains connected to the top of Segment 1. The code driving DAC3 is automatically complemented to compensate for the inversion of its inputs. This means that any linearity effects due to amplifier offset voltages remain unchanged when switching from one segment to the next and 16-bit monotonicity is ensured if DAC3 is monotonic. So, 12-bit resistor matching in DAC3 guarantees overall 16-bit monotonicity. This is much more achievable than the 16-bit matching which a conventional R-2R structure would have needed.

Output Stage

The output stage of the AD7849 is shown in Figure 11. It is capable of driving a load of 2 kΩ in parallel with 200 pF. The feedback and offset resistors allow the output stage to be configured for gains of 1 or 2. Additionally, the offset resistor may be used to shift the output range.

The AD7849 has a special feature to ensure output stability during power-up and power-down sequences. This is specifically available for control applications where actuators must not be allowed to move in an uncontrolled fashion.

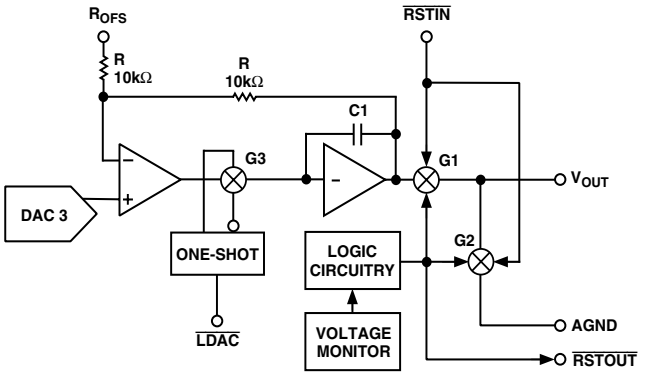


Figure 11. AD7849 Output Stage

When the supply voltages are changing, the V_{OUT} pin is clamped to 0 V via a low impedance path . To prevent the output of A3 being shorted to 0 V during this time, transmission gate G1 is also opened. These conditions are maintained until the power supplies stabilize and a valid word is written to the DAC register. At this time, G2 opens and G1 closes. Both transmission gates are also externally controllable via the Reset In ($\overline{RST\ IN}$) control input. For instance, if the $\overline{RST\ IN}$ input is driven from a battery supervisor chip, then on power-off or during a brown-out, the $\overline{RST\ IN}$ input will be driven low to open G1 and close G2. The DAC has to be reloaded, with $\overline{RST\ IN}$ high, to re-enable the output. Conversely, the on-chip voltage detector output ($\overline{RST\ OUT}$) is also available to the user to control other parts of the system.

The AD7849 output buffer is configured as a track-and-hold amplifier. Although normally tracking its input, this amplifier is placed in a hold mode for approximately 5 µs after the leading edge of $\overline{LDAC}$. This short state keeps the DAC output at its previous voltage while the AD7849 is internally changing to its new value. So, any glitches that occur in the transition are not seen at the output. In systems where the $\overline{LDAC}$ is permanently low, the deglitching will not be in operation.

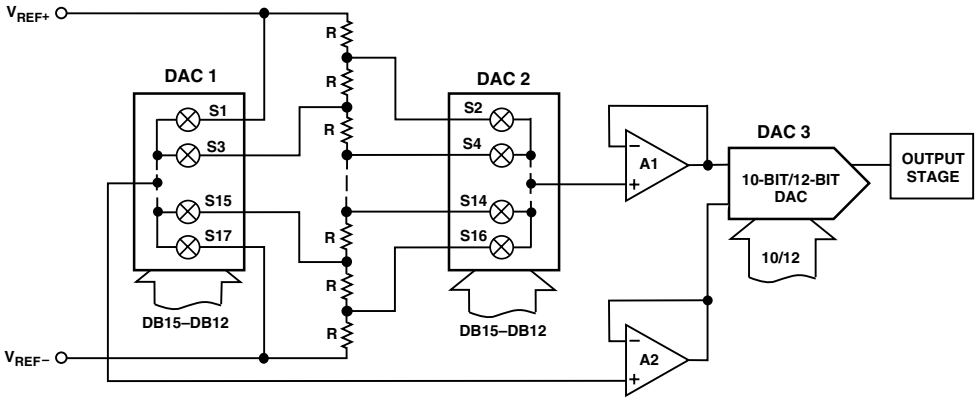


Figure 10. AD7849 D/A Conversion

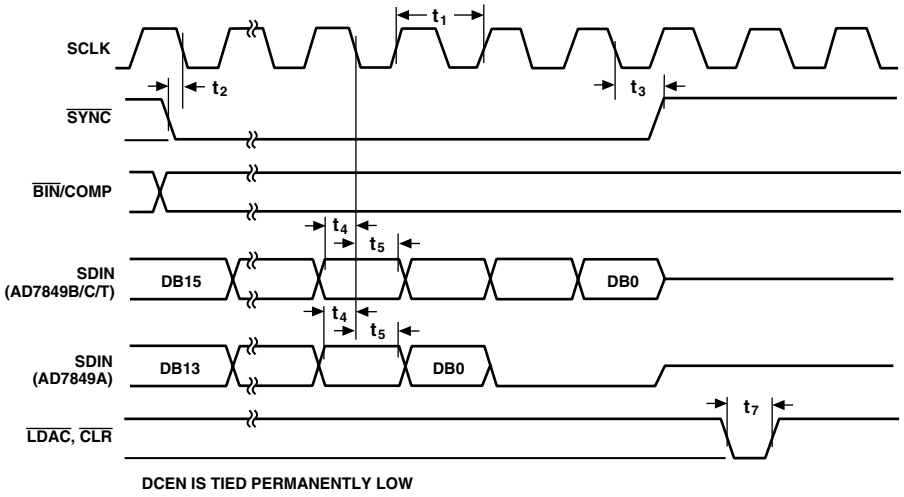


Figure 12. Timing Diagram (Stand-Alone Mode)

DIGITAL INTERFACE

The AD7849 contains an input serial to parallel shift register and a DAC latch. A simplified diagram of the input loading circuitry is shown in Figure 12. Serial data on the SDIN input is loaded to the input register under control of DCEN, $\overline{SYNC}$ and SCLK. When a complete word is held in the shift register it may then be loaded into the DAC latch under control of $\overline{LDAC}$. Only the data in the DAC latch determines the analog output on the AD7849.

The DCEN (daisy-chain enable) input is used to select either a stand-alone mode or a daisy-chain mode. The loading format is slightly different depending on which mode is selected.

Serial Data Loading Format (Stand-Alone Mode)

With DCEN at Logic 0 the stand-alone mode is selected. In this mode a low $\overline{SYNC}$ input provides the frame synchronization signal which tells the AD7849 that valid serial data on the SDIN input will be available for the next 16 falling edges of SCLK. An internal counter/decoder circuit provides a low gating signal so that only 16 data bits are clocked into the input shift register. After 16 SCLK pulses the internal gating signal goes inactive (high) thus locking out any further clock pulses. Therefore either a continuous clock or a burst clock source may be used to clock in the data.

The $\overline{SYNC}$ input is taken high after the complete 16-bit word is loaded in.

The AD7849B, AD7849C and AD7849T versions are 16-bit resolution DACS and have a straight 16-bit load format, with the MSB (DB15) being loaded first. The AD7849A is a 14-bit DAC but the loading structure is still 16-bit. The MSB (DB13) is loaded first and the final two bits of the 16-bit stream must be 0s.

There are two ways in which the DAC latch and hence the analog output may be updated. The status of the $\overline{LDAC}$ input is examined after $\overline{SYNC}$ is taken low. Depending on its status, one of two update modes is selected.

If $\overline{LDAC}$ = 0 then the automatic update mode is selected. In this mode the DAC latch and analog output are updated automatically when the last bit in the serial data stream is clocked in. The update thus takes place on the sixteenth falling SCLK edge.

If $\overline{LDAC}$ = 1 then the automatic update is disabled. The DAC latch update and output update are now separate. The DAC latch is updated on the falling edge of $\overline{LDAC}$. However, the output update is delayed for a further 5 μs by means of an internal track-and-hold amplifier in the output stage. This function results in lower digital-to-analog glitch impulse at the DAC output. Note that the $\overline{LDAC}$ input must be taken back high again before the next data transfer is initiated.

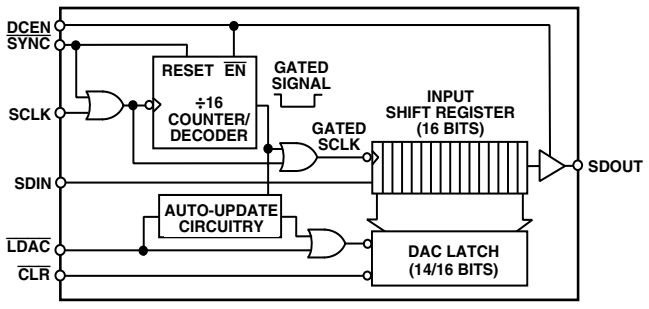


Figure 13. Simplified Loading Structure

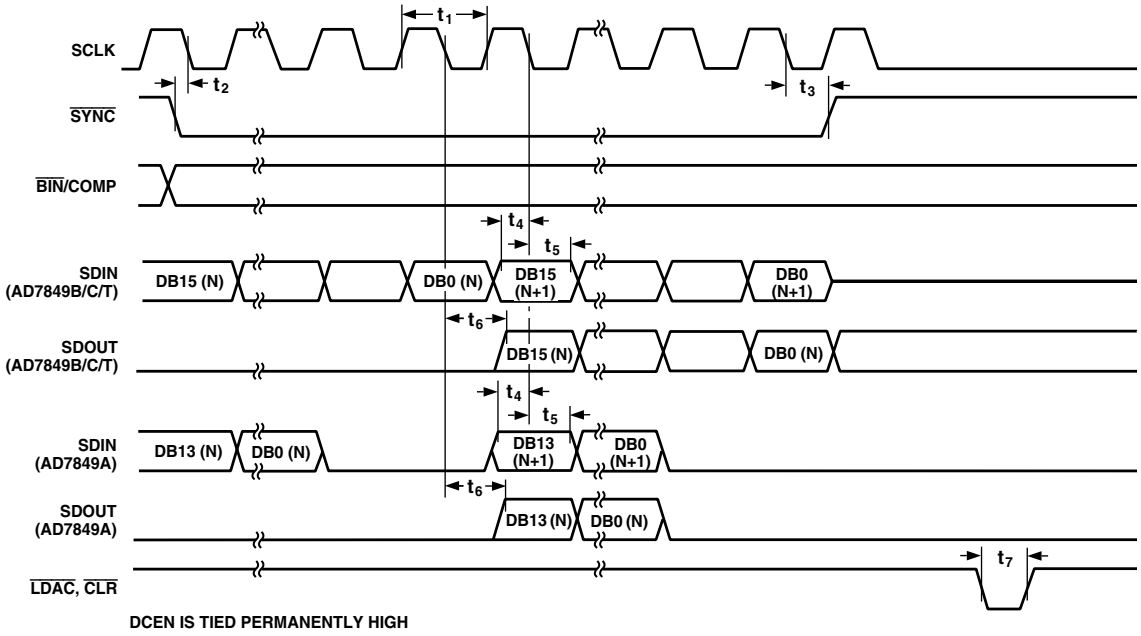


Figure 14. Timing Diagram (Daisy-Chain Mode)

Serial Data Loading Format (Daisy Chain Mode)

By connecting DCEN high, the daisy-chain mode is enabled. This mode of operation is designed for multi-DAC systems where several AD7849s may be connected in cascade. In this mode, the internal gating circuitry on SCLK is disabled and a serial data output facility is enabled. The internal gating signal is permanently active (low) so that the SCLK signal is continuously applied to the input shift register when $\overline{SYNC}$ is low. The data is clocked into the register on each falling SCLK edge after $\overline{SYNC}$ going low. If more than 16 clock pulses are applied, the data ripples out of the shift register and appears on the SDOUT line. By connecting this line to the SDIN input on the next AD7849 in the chain, a multi-DAC interface may be constructed. Sixteen SCLK pulses are required for each DAC in the system. Therefore the total number of clock cycles must equal $16 \times N$ where N is the total number of devices in the chain. When the serial transfer to all devices is complete, $\overline{SYNC}$ is taken high. This prevents any further data being clocked into the input register.

A continuous SCLK source may be used if it can be arranged that $\overline{SYNC}$ is held low for the correct number of clock cycles. Alternatively, a burst clock containing the exact number of clock cycles may be used and $\overline{SYNC}$ taken high some time later.

When the transfer to all input registers is complete, a common $\overline{LDAC}$ signal updates all DAC latches with the data in each input register. All analog outputs are therefore updated simultaneously, 5 µs after the falling edge of $\overline{LDAC}$.

Clear Function ($\overline{CLR}$)

The clear function bypasses the input shift register and loads the DAC Latch with all 0s. It is activated by taking $\overline{CLR}$ low. In all ranges except the Offset Binary bipolar range (–5 V to +5 V) the output voltage is reset to 0 V. In the offset binary bipolar range the output is set to V_{REF-}. This clear function is distinct and separate from the automatic power-on reset feature of the device.

APPLYING THE AD7849

Power Supply Sequencing and Decoupling

In the AD7849, V_{CC} should not exceed V_{DD} by more than 0.4 V. If this does happen then an internal diode can be turned on and produce latch-up in the device. Care should be taken to employ the following power supply sequence: V_{DD}; V_{SS}; V_{CC}. In systems where it is possible to have an incorrect power sequence (for example, if V_{CC} is greater than 0.4 V while V_{DD} is still 0 V), the circuit of Figure 15 may be used to ensure that the Absolute Maximum Ratings are not exceeded.

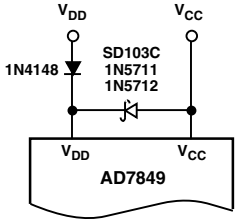


Figure 15. Power Supply Protection

Unipolar Configuration

Figure 16 shows the AD7849 in the unipolar binary circuit configuration. The DAC is driven by the AD586, +5 V reference. Since R_{OFS} is tied to 0 V, the output amplifier has a gain of ×2 and the output range is 0 V to +10 V. If a 0 V to +5 V range is required, R_{OFS} should be tied to V_{OUT}, configuring the output stage for a gain of ×1. Table I gives the code table for the circuit of Figure 16.

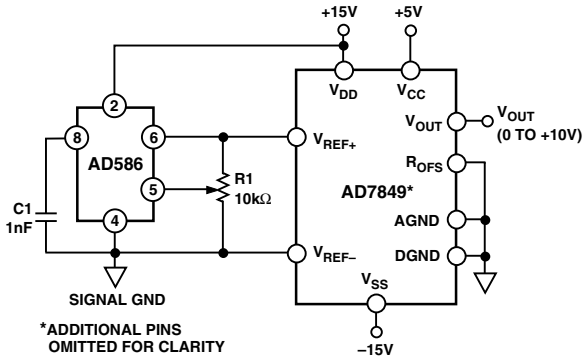


Figure 16. Unipolar Binary Operation

Table I. Code Table for Figure 16

Binary Number in DAC Latch MSB LSB	Analog Output (V_{OUT})
1111 1111 1111 1111	+10 (65535/65536) V
1000 0000 0000 0000	+10 (32768/65536) V
0000 0000 0000 0001	+10 (1/65536) V
0000 0000 0000 0000	0 V

NOTE: Assumes 16-bit resolution; 1 LSB = 10 V/2^{16} = 10 V/65536 = 152 μV.

Offset and gain may be adjusted in Figure 16 as follows: To adjust offset, disconnect the V_{REF-} input from 0 V, load the DAC with all 0s and adjust the V_{REF-} voltage until V_{OUT} = 0 V. For gain adjustment, the AD7849 should be loaded with all 1s and R1 adjusted until V_{OUT} = 10 (65535)/65536 = 9.9998474 V, (B, T and C, 16-bit versions). For the 14-bit A version, V_{OUT} should be 10 (16383/16384) = 9.9993896 V.

If a simple resistor divider is used to vary the V_{REF-} voltage, it is important that the temperature coefficients of these resistors match that of the DAC input resistance (–300 ppm/°C). Otherwise, extra offset errors will be introduced over temperature. Many circuits will not require these offset and gain adjustments. In these circuits, R1, can be omitted. Pin 5 of the AD586 may be left open circuit and Pin 2 (V_{REF-}) of the AD7849 tied to 0 V.

Bipolar Configuration

Figure 17 shows the AD7849 set up for ±10 V bipolar operation. The AD588 provides precision ±5 V tracking outputs which are fed to the V_{REF+} and V_{REF-} inputs of the AD7849. The code table for Figure 17 is shown in Table II.

Full-scale and bipolar-zero adjustment are provided by varying the gain and balance on the AD588. R2 varies the gain on the AD588 while R3 adjusts the +5 V and –5 V outputs together with respect to ground.

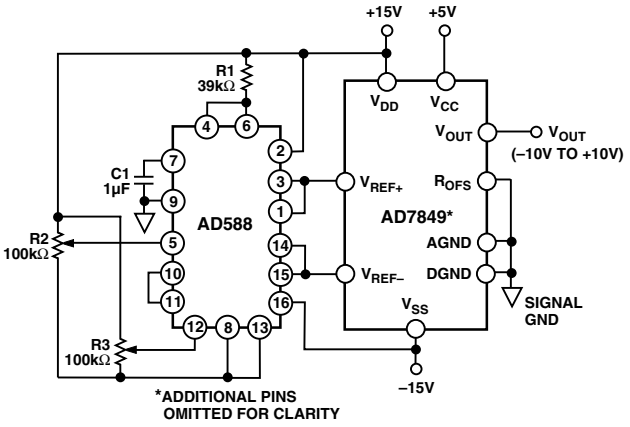


Figure 17. Bipolar ±10 V Operation

Table II. Offset Binary Code Table for Figure 17

Binary Number in DAC Latch MSB LSB	Analog Output (V_{OUT})
1111 1111 1111 1111	+10 (32767/32768) V
1000 0000 0000 0001	+10 (1/32768) V
1000 0000 0000 0000	0 V
0111 1111 1111 1111	–10 (1/32768) V
0000 0000 0000 0000	–10 (32768/32768) V

NOTE: Assumes 16-bit resolution; 1 LSB = 20 V/2^{16} = 305 μV.

For bipolar-zero adjustment on the AD7849, load the DAC with 100 . . . 000 and adjust R3 until V_{OUT} = 0 V. Full scale is adjusted by loading the DAC with all 1s and adjusting R2 until V_{OUT} = 9.999694 V.

When bipolar-zero and full-scale adjustment are not needed, R2 and R3 can be omitted, Pin 12 on the AD588 should be connected to Pin 11 and Pin 5 should be left floating.

If a user wants a ±5 V output range with the circuit of Figure 17, simply tie Pin 20 (R_{OFS}) to Pin 19 (V_{OUT}), thus reducing the output gain stage to unity and giving an output range of ±5 V.

Other Output Voltage Ranges

In some cases, users may require output voltage ranges other than those already mentioned. One example is systems which need the output voltage to be a whole number of millivolts (i.e., 1 mV, 2 mV, etc.,). If Figure 18 is used, then the LSB size is 125 µV. This makes it possible to program whole millivolt values at the output. Table III shows the code table for Figure 18.

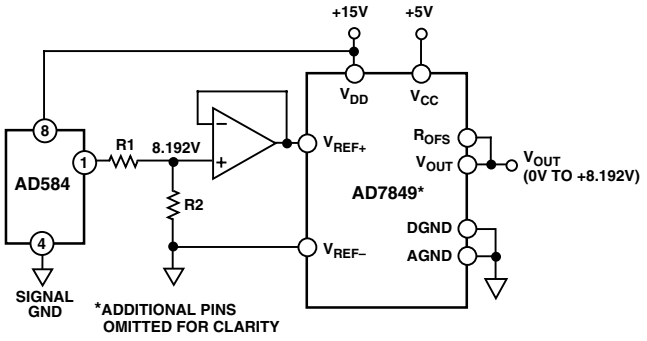


Figure 18. 0 V to 8.192 V Output Range

Table III. Code Table for Figure 18

Binary Number in DAC Latch MSB LSB	Analog Output (V_{OUT})
1111 1111 1111 1111	8.192 V (65535/65536) = 8.1919 V
1000 0000 0000 0000	8.192 V (32768/65536) = 4.096 V
0000 0000 0000 1000	8.192 V (8/65536) = 0.001 V
0000 0000 0000 0100	8.192 V (4/65536) = 0.0005 V
0000 0000 0000 0010	8.192 V (2/65536) = 0.00025 V
0000 0000 0000 0001	8.192 V (1/65536) = 0.000125 V

NOTE: Assumes 16-bit resolution; 1 LSB = 8.192 V/2^{16} = 125 µV.

Generating ±5 V Output Range From Single +5 V Reference

The diagram below shows how to generate a ±5 V output range when using a single +5 V reference. V_{REF-} is connected to 0 V and R_{OFS} is connected to V_{REF+}. The +5 V reference input is applied to these pins. With all 0s loaded to the DAC, the noninverting terminal of the output stage amplifier is at 0 V and V_{OUT} is simply the inverse of V_{REF+}. With all 1s loaded to the DAC, the noninverting terminal of the output stage amplifier is at 5 V and so V_{OUT} is also at 5 V.

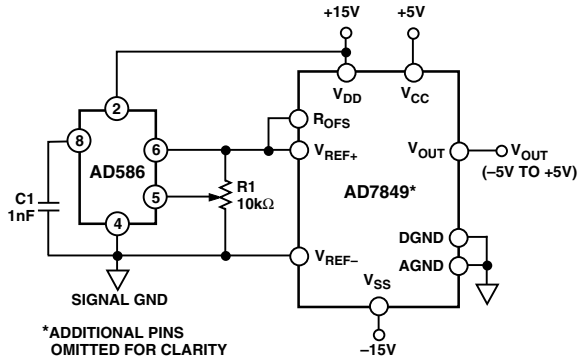


Figure 19. Generating ±5 V Output Range From Single +5 V

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD7849 is via a serial bus which uses standard protocol compatible with DSP processors and microcontrollers. The communications channel requires a three-wire interface consisting of a clock signal, a data signal and a synchronization signal. The AD7849 requires a 16-bit data word with data valid on the falling edge of SCLK. For all the interfaces, the DAC update may be done automatically when all the data is clocked in or it may be done under control of $\overline{\text{LDAC}}$.

Figures 20 to 24 show the AD7849 configured for interfacing to a number of popular DSP processors and microcontrollers.

AD7849-ADSP-2101/ADSP-2102 Interface

Figure 20 shows a serial interface between the AD7849 and the ADSP-2101/ADSP-2102 DSP processor. The ADSP-2101/ ADSP-2102 contains two serial ports and either port may be used in the interface. The data transfer is initiated by $\overline{\text{TFS}}$ going low. Data from the ADSP-2101/ ADSP-2102 is clocked into the AD7849 on the falling edge of SCLK. The DAC can be updated by holding $\overline{\text{LDAC}}$ high while performing the write cycle. $\overline{\text{TFS}}$ must be taken high after the 16-bit write cycle. $\overline{\text{LDAC}}$ is brought low at the end of the cycle and the DAC output is updated. In the interface shown the DAC is updated using an external timer which generates an $\overline{\text{LDAC}}$ pulse. This could also be done using a control or decoded address line from the processor. Alternatively, if the $\overline{\text{LDAC}}$ input is hardwired low the output update takes place automatically on the 16th falling edge of SCLK.

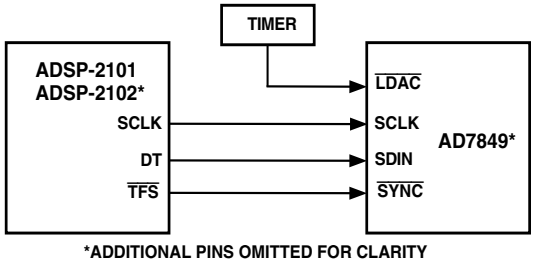


Figure 20. AD7849 to ADSP-2101/ADSP-2102 Interface

AD7849-DSP56000 Interface

A serial interface between the AD7849 and the DSP56000 is shown in Figure 21. The DSP56000 is configured for Normal Mode Asynchronous operation with Gated Clock. It is also set up for a 16-bit word with SCK and SC2 as outputs and the FSL control bit set to a "0". SCK is internally generated on the DSP56000 and applied to the AD7849 SCLK input. Data from the DSP56000 is valid on the falling edge of SCK. The SC2 output provides the framing pulse for valid data. This line must be inverted before being applied to the $\overline{\text{SYNC}}$ input of the AD7849.

In this interface an $\overline{\text{LDAC}}$ pulse generated from an external timer is used to update the outputs of the DACs. This update can also be produced using a bit programmable control line from the DSP56000.

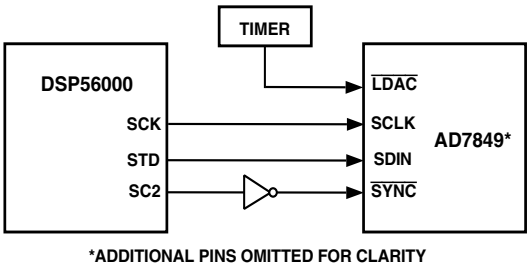


Figure 21. AD7849 to DSP56000 Interface

AD7849-TMS320C2x Interface

Figure 22 shows a serial interface between the AD7849 and the TMS320C2x DSP processor. In this interface, the CLKX and FSX signals for the TMS320C2x should be generated using external clock/timer circuitry. The FSX pin of the TMS320C2x must be configured as an input. Data from the TMS320C2x is valid on the falling edge of CLKX.

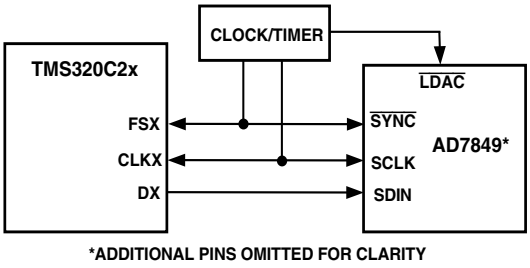


Figure 22. AD7849 to TMS320C2x Interface

The clock/timer circuitry generates the $\overline{\text{LDAC}}$ signal for the AD7849 to synchronize the update of the output with the serial transmission. Alternatively, the automatic update mode may be selected by connecting $\overline{\text{LDAC}}$ to DGND.

AD7849-68HC11 Interface

Figure 23 shows a serial interface between the AD7849 and the 68HC11 microcontroller. SCK of the 68HC11 drives SCLK of the AD7849 while the MOSI output drives the serial data line of the AD7849. The $\overline{\text{SYNC}}$ signal is derived from a port line (PC0 shown).

For correct operation of this interface, the 68HC11 should be configured such that its CPOL bit is a 0 and its CPHA bit is a 1. When data is to be transmitted to the part, PC0 is taken low. When the 68HC11 is configured like this, data on MOSI is valid on the falling edge of SCK. The 68HC11 transmits its serial data in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. To load data to the AD7849, PC0 is left low after the first eight bits are transferred and a second byte of data is then transferred serially to the AD7849. When the second serial transfer is complete, the PC0 line is taken high.

Figure 23 shows the $\overline{\text{LDAC}}$ input of the AD7849 being driven from another bit programmable port line (PC1). As a result, the DAC can be updated by taking $\overline{\text{LDAC}}$ low after the DAC input register has been loaded.

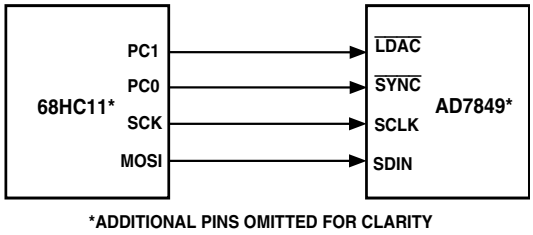


Figure 23. AD7849 to 68HC11 Interface

AD7849-87C51 Interface

A serial interface between the AD7849 and the 87C51 microcontroller is shown in Figure 24. TXD of the 87C51 drives SCLK of the AD7849 while RXD drives the serial data line of the part. The $\overline{\text{SYNC}}$ signal is derived from the port line P3.3 and the $\overline{\text{LDAC}}$ line is driven port line P3.2.

The 87C51 provides the LSB of its SBUF register as the first bit in the serial data stream. Therefore, the user will have to ensure that the data in the SBUF register is arranged correctly so that the most significant bits are the first to be transmitted to the AD7849 and the last bit to be sent is the LSB of the word to be loaded to the AD7849. When data is to be transmitted to the part, P3.3 is taken low. Data on RXD is valid on the falling edge of TXD. The 87C51 transmits its serial data in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. To load data to the AD7849, P3.3 is left low after the first eight bits are transferred and a second byte of data is then transferred serially to the AD7849. When the second serial transfer is complete, the P3.3 line is taken high.

Figure 24 shows the $\overline{\text{LDAC}}$ input of the AD7849 driven from the bit programmable port line P3.2. As a result, the DAC output can be updated by taking the $\overline{\text{LDAC}}$ line low following the completion of the write cycle. Alternatively $\overline{\text{LDAC}}$ could be hardwired low and the analog output will be updated on the sixteenth falling edge of TXD after the $\overline{\text{SYNC}}$ signal for the DAC has gone low.

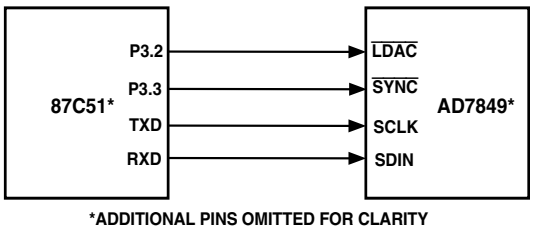


Figure 24. AD7849 to 87C51 Interface

APPLICATIONS

Opto-Isolated Interface

In many process control type applications it is necessary to provide an isolation barrier between the controller and the unit being controlled. Opto isolators can provide voltage isolation in excess of 3 kV. The serial loading structure of the AD7849 makes it ideal for opto-isolated interfaces as the number of interface lines is kept to a minimum.

Figure 25 shows a 4-channel isolated interface using the AD7849. The DCEN pin must be connected high to enable the daisy-chain facility. Four channels with 14-bit or 16-bit resolution are provided in the circuit shown, but this may be expanded to accommodate any number of DAC channels without any extra isolation circuitry. The only limitation is the output update rate. For example, if an output update rate of 10 kHz is required, then all the DACs must be loaded and updated in a time period of 100 µs. Operating at the maximum clock rate of 5 MHz means that it takes 3.2 µs to load a DAC. This means that the total number of channels for this update rate would be 31. This leaves 800 ns for the $\overline{\text{LDAC}}$ pulse. Of course, as the update rate requirement decreases, the number of possible channels increases.

The sequence of events to program the output channels in Figure 25 is as follows.

1. Take the $\overline{\text{SYNC}}$ line low.
2. Transmit the data as four 16-bit words. A total of 64 clock pulses is required to clock the data through the chain.
3. Take the $\overline{\text{SYNC}}$ line high.
4. Pulse the $\overline{\text{LDAC}}$ line low. This updates all output channels simultaneously on the falling edge of $\overline{\text{LDAC}}$.

To reduce the number of opto-couplers, the $\overline{\text{LDAC}}$ line could be driven from a one-shot which is triggered by the rising edge on the $\overline{\text{SYNC}}$ line. A low level pulse of 100 ns duration or greater is all that is required to update the outputs.

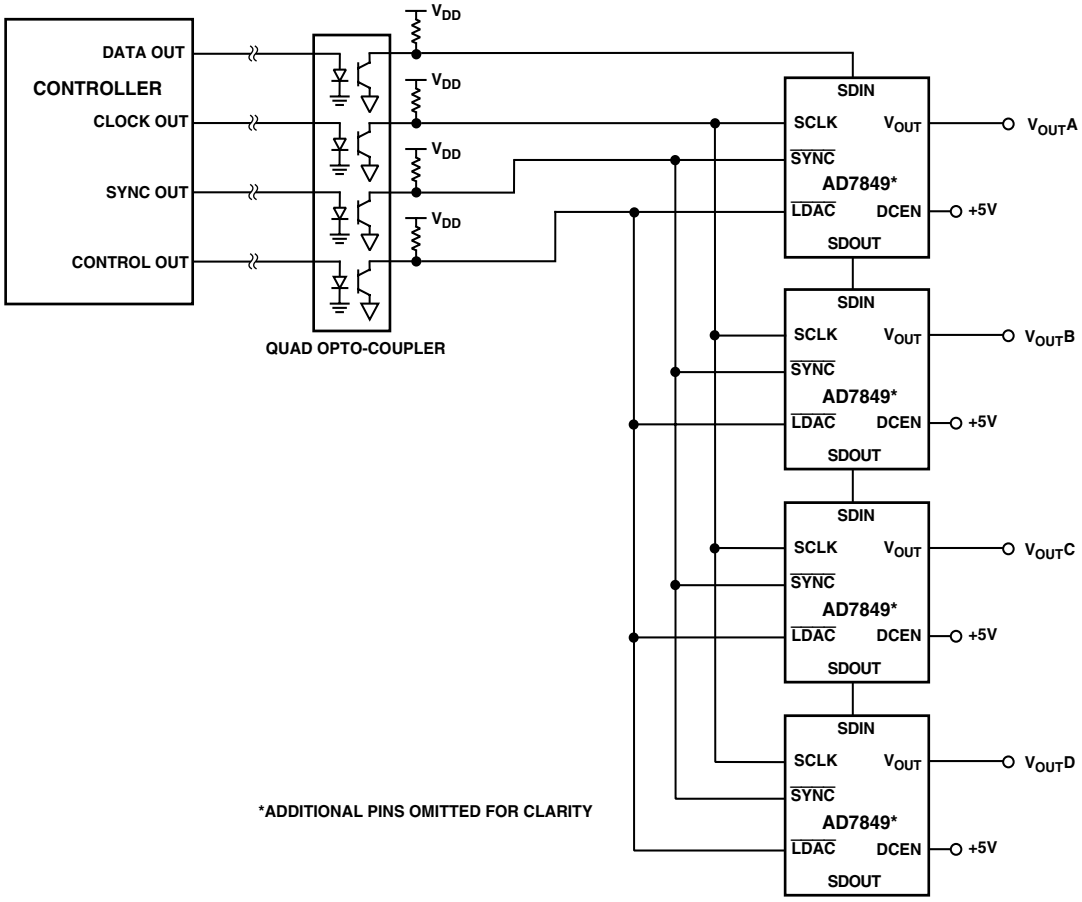
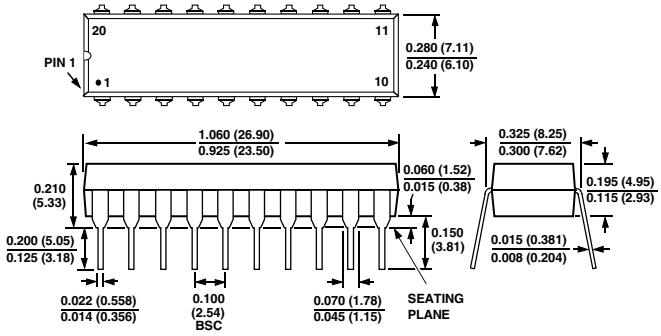


Figure 25. Four-Channel Opto-Isolated Interface

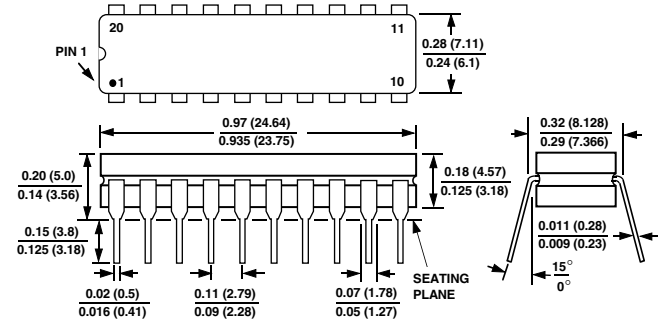
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Plastic DIP (N-20)

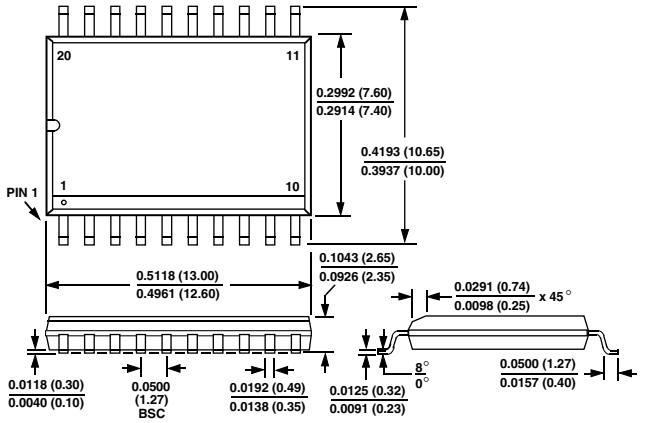


Cerdip (Q-20)



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42

SOIC (R-20)



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