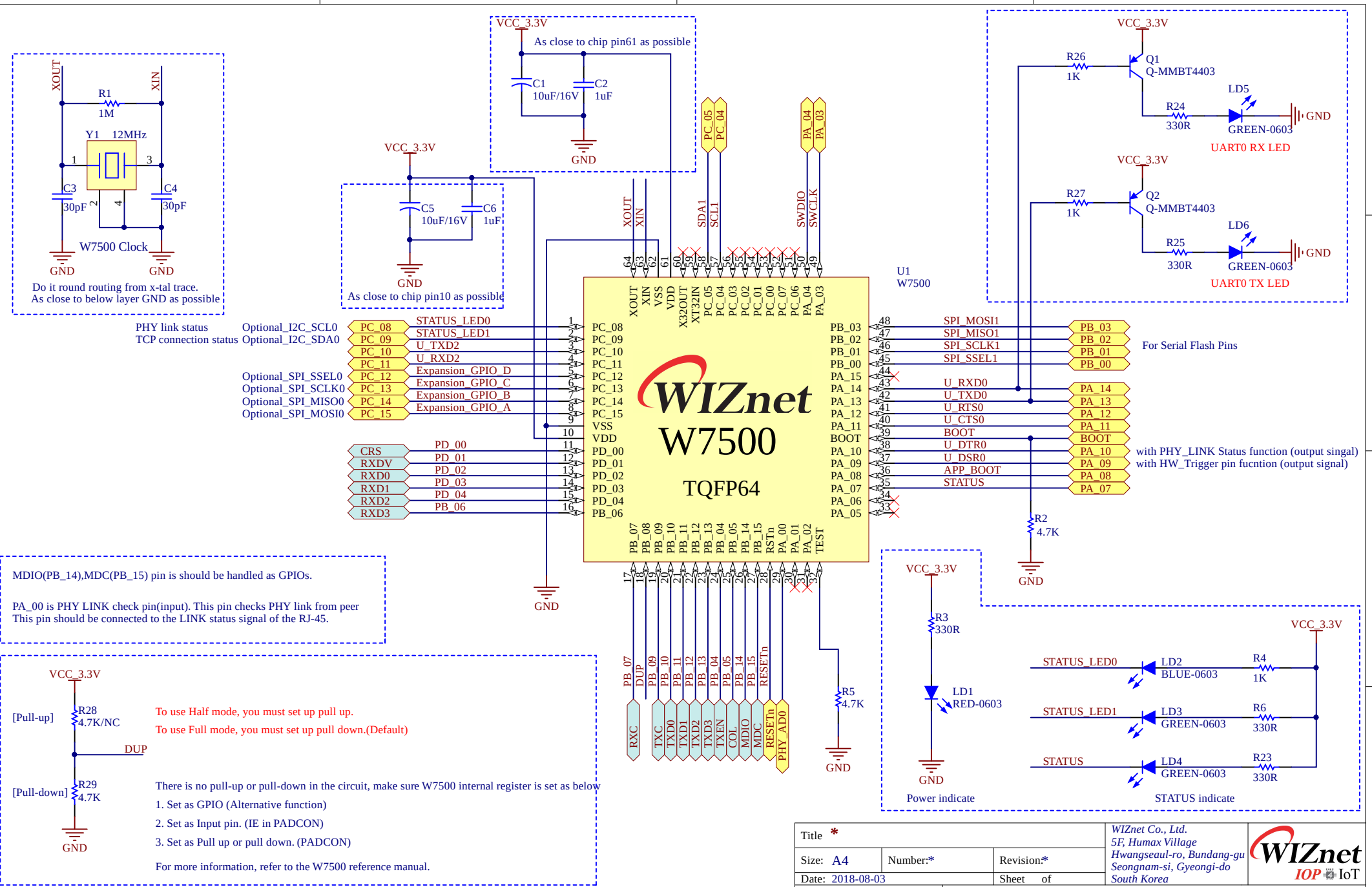
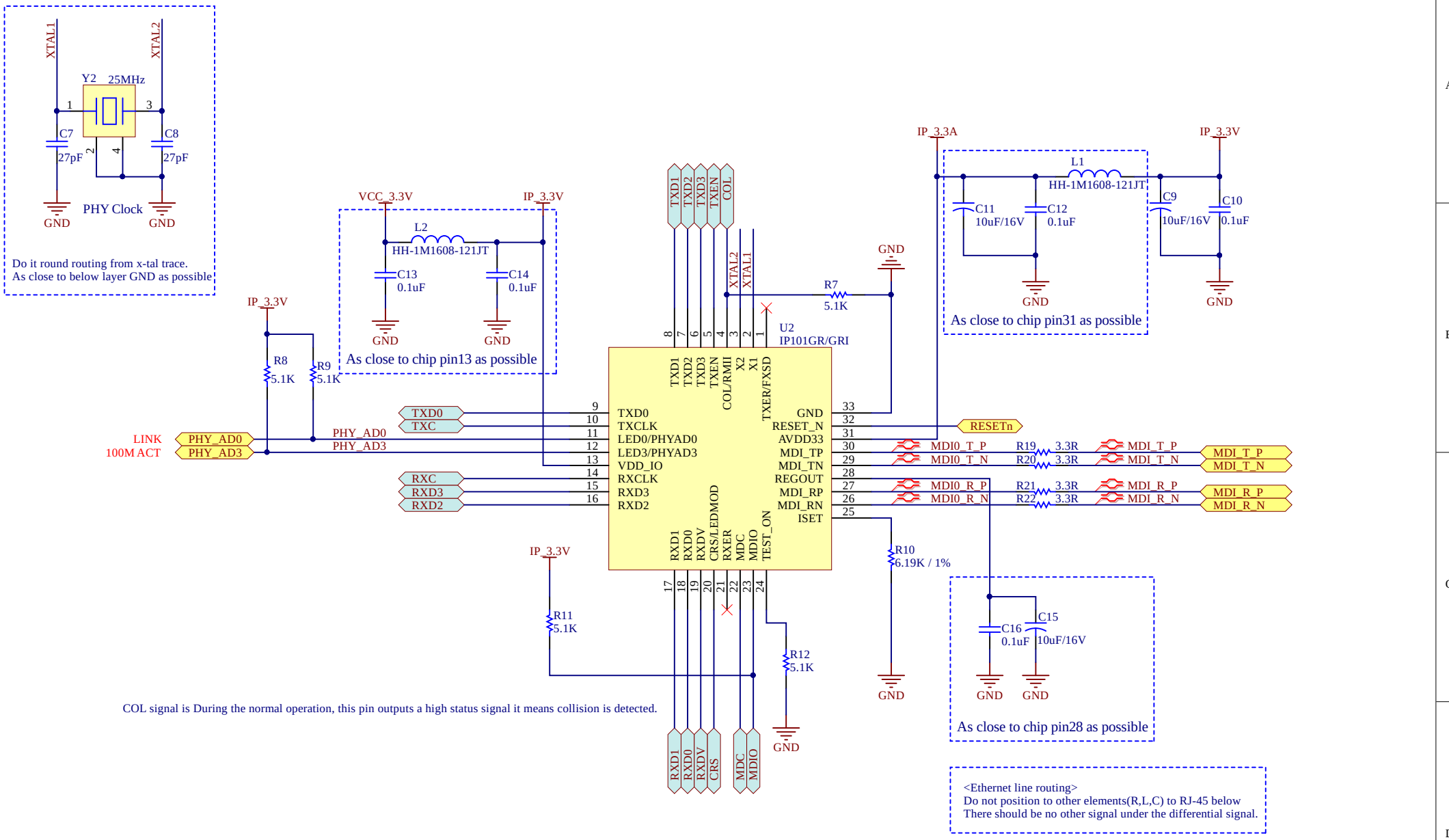
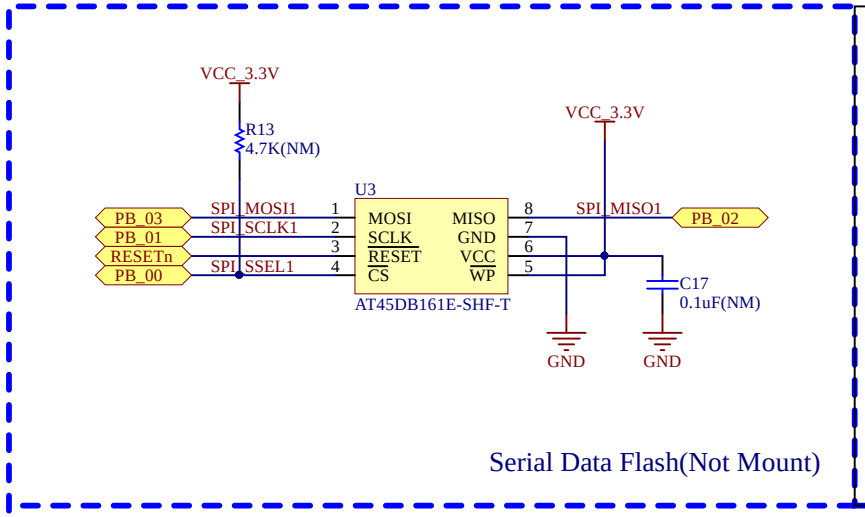
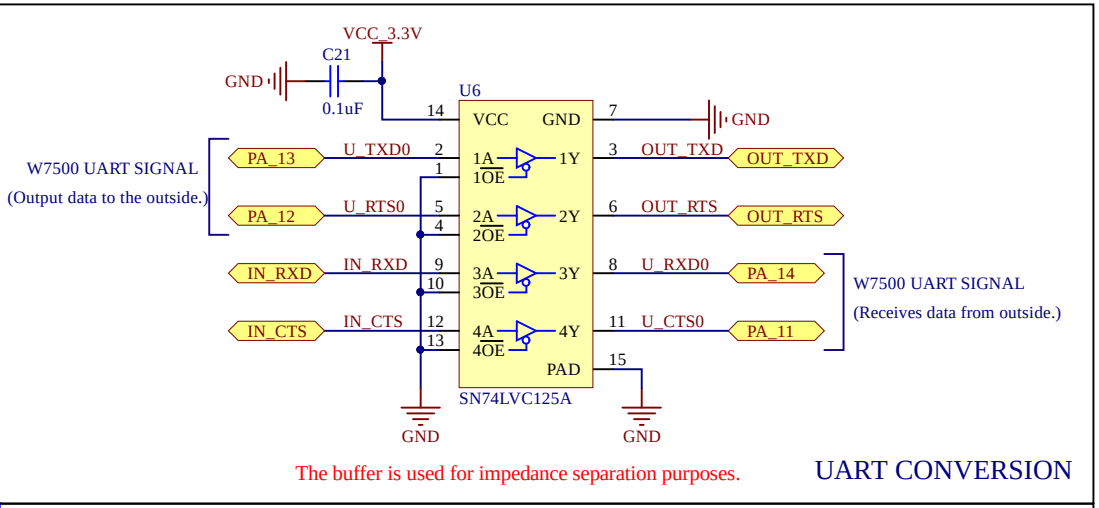
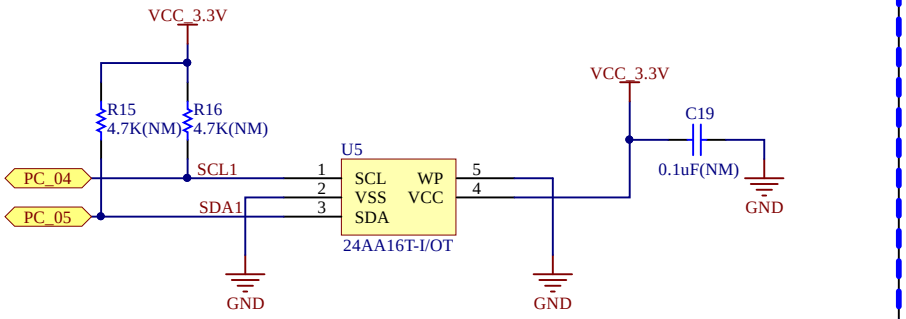

W7500 Clock
Do it round routing from x-tal trace.
As close to below layer GND as possible
As close to chip pin61 as possible
As close to chip pin10 as possible
PHY link status
TCP connection status
Optional_I2C_SCL0
Optional_I2C_SDA0
Optional_SPI_SSEL0
Optional_SPI_SCLK0
Optional_SPI_MISO0
Optional_SPI_MOSI0
U1
W7500
TQFP64
For Serial Flash Pins
with PHY_LINK Status function (output singal)
with HW_Trigger pin fucntion (output signal)
UART0 RX LED
UART0 TX LED
Power indicate
STATUS indicate
MDIO(PB_14),MDC(PB_15) pin is should be handled as GPIOs.
PA_00 is PHY LINK check pin(input). This pin checks PHY link from peer
This pin should be connected to the LINK status signal of the RJ-45.
To use Half mode, you must set up pull up.
To use Full mode, you must set up pull down.(Default)
There is no pull-up or pull-down in the circuit, make sure W7500 internal register is set as below
1. Set as GPIO (Alternative function)
2. Set as Input pin. (IE in PADCON)
3. Set as Pull up or pull down. (PADCON)
For more information, refer to the W7500 reference manual.
Title *
Size: A4
Number:*
Revision:*
Date: 2018-08-03
Sheet of
Team: Team Module
Drawn By: Edward
WIZnet Co., Ltd.
5F, Humax Village
Hwangseaul-ro, Bundang-gu
Seongnam-si, Gyeongi-do
South Korea

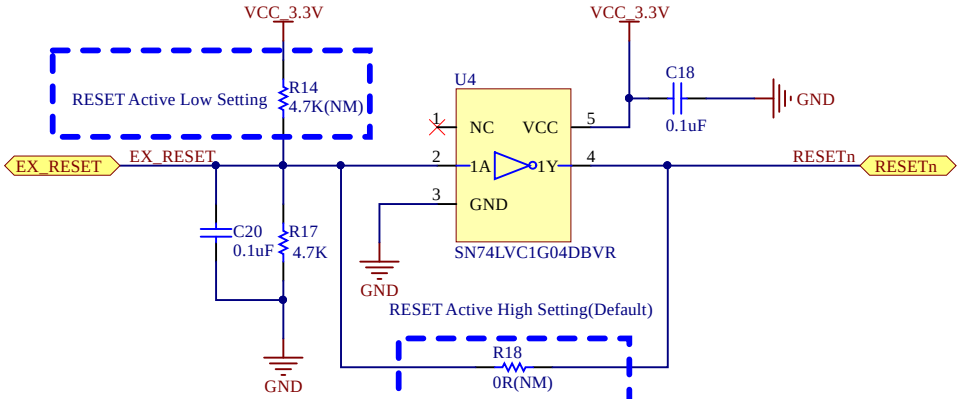


Title *			WIZnet Co., Ltd. 5F, Humax Village Hwangseaul-ro, Bundang-gu Seongnam-si, Gyeongi-do South Korea
Size: A4	Number:*	Revision:*	
Date: 2018-08-03		Sheet of	
Team: Team Module	Drawn By: Edward		









Mode	U4	R14	R17	R18
Active High(Default)	Mount		Mount	
Active Low		Mount		Mount

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Size: A4	Number:*	Revision:*	
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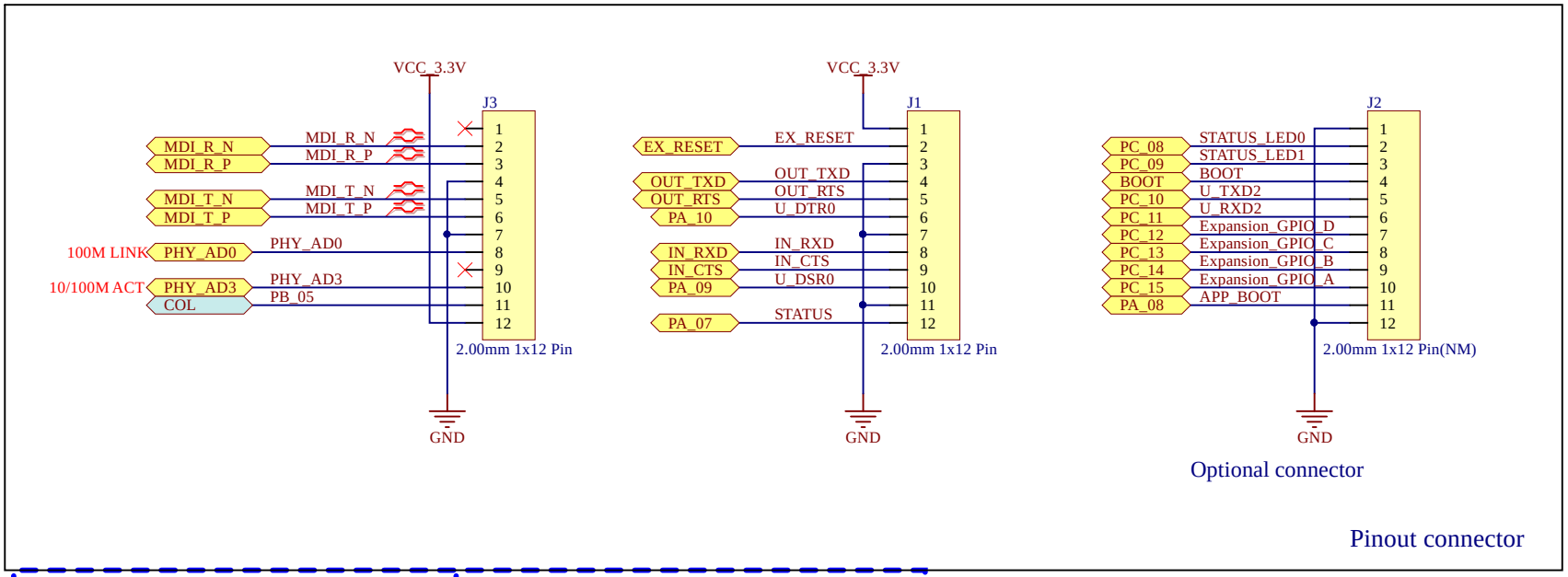

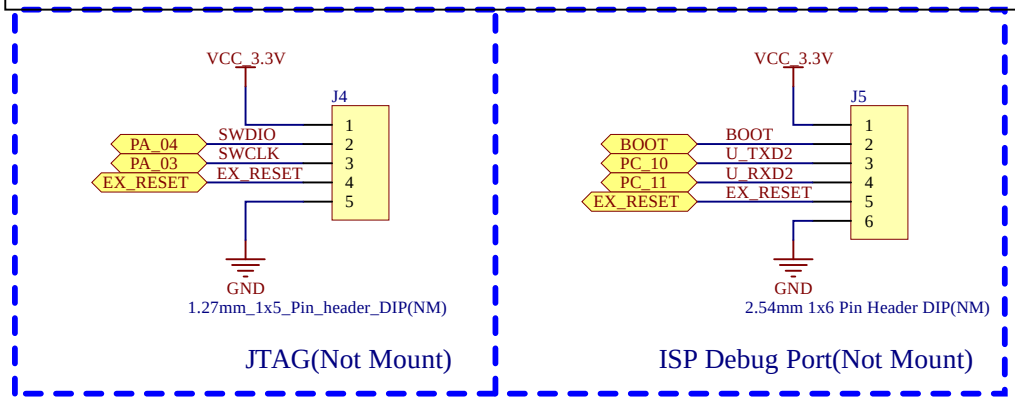

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