ETM09E-03

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Application Manual

Real Time Clock Module

RTC-4543SA/SB

SEIKO EPSON CORPORATION

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CONTENTS

32-kHz Output Serial RTC Module

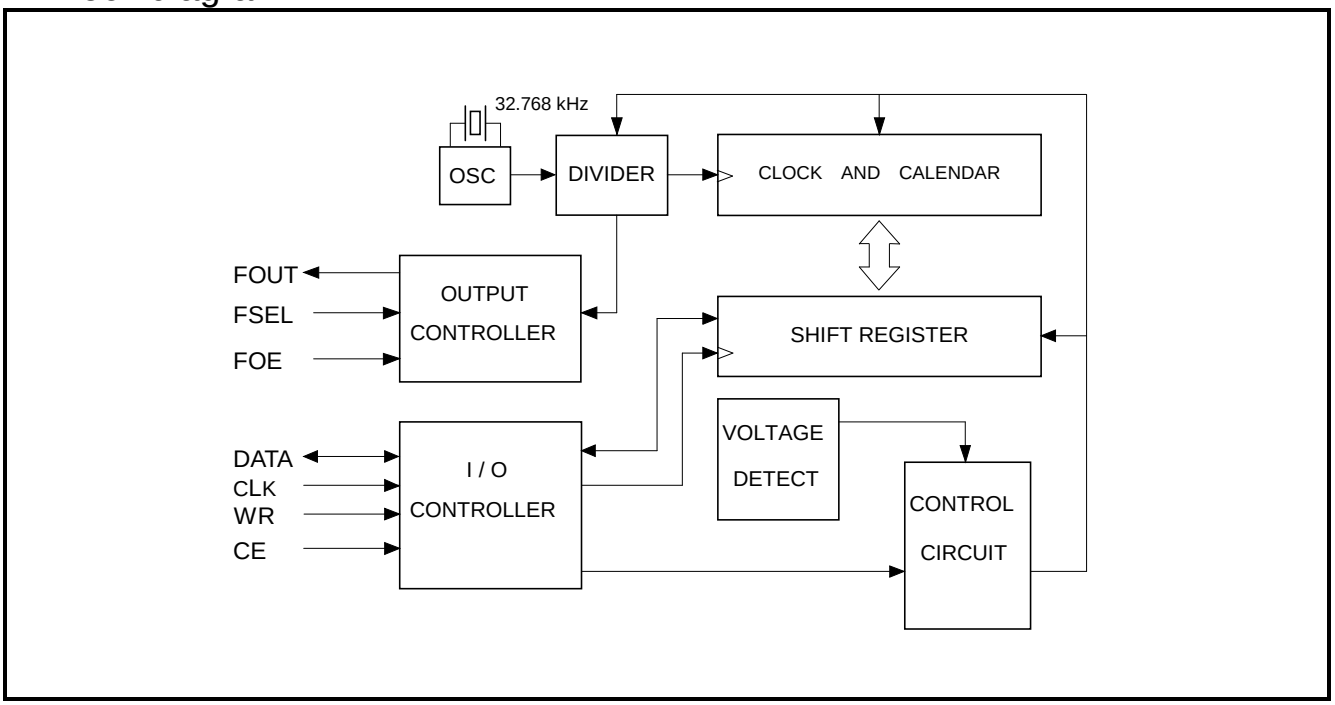
RTC - 4543 SA/SB

- Built-in crystal permits operation without requiring adjustment
- Built-in time counters (seconds, minutes, hours) and calendar counters (days, days of the week months, years)
- Operating voltage range: 2.5 V to 5.5 V
- Supply voltage detection voltage: 1.7 ±0.3 V
- Low current consumption: 1.0 μA/2.0 V (Max.)
- Automatic processing for leap years
- Output selectable between 32.768 kHz/1 Hz

1. Overview

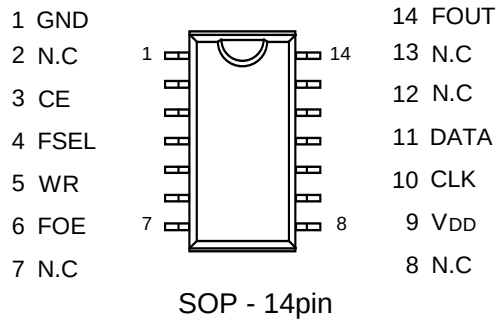
This module is a real-time clock with a serial interface and a built-in crystal oscillator. This module is also equipped with clock and calendar circuits, an automatic leap year compensation function, and a supply voltage detection function.
In addition, this module has a 32.768 kHz/1 Hz selectable output function for hardware control that is independent of the RTC circuit.
This module is available in a compact SOP 14-pin package (RTC-4543SA) and a thin SOP 18-pin package (RTC-4543SB).

2. Block diagram



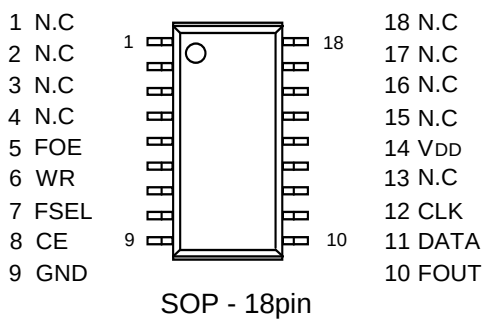
3. Pin Connections

RTC - 4543SA



SOP - 14pin

RTC - 4543SB



SOP - 18pin

4. Pin Functions

Signal	Pin No. SOP-14pin (SOP-18pin)	I/O	Function
GND	1 (9)		Connects to negative (-) side (ground) of the power supply.
CE	3 (8)	Input	Chip enable input pin. When high,the chip is enabled. When low,the DATA pin goes to high impedance and the CLK,DATA,and WR pins are not able to accept input.In addition, when low,the TM bit is cleared.
FSEL	4 (7)	Input	Serect the frequency that is output from the FOUT pin. High : 1 Hz Low : 32.768 kHz
WR	5 (6)	Input	DATA pin input/output switching pin. High : DATA input (when writing the RTC) Low : DATA output (when reading the RTC)
FOE	6 (5)	Input	When high, the frequency selected by the FSEL pin is output from the FOUT pin. When low, the FOUT pin goes to high impedance.
V_{DD}	9 (14)		Connects to positive (+) side of the power supply.
CLK	10 (12)	Input	Serial clock input pin. Data is gotten at the rising edge during a write, and data is output at the rising edge during a read.
DATA	11 (11)	Bi-directional	Input/outout pin that is used for writing and reading data.
FOUT	14 (10)	Output	Outputs the frequency selected by the FSEL pin. 1 Hz output is synchronized with the internal one-second signal. This output is not affected by the CE pin.
N.C.	2,7,8,12,13 (1,2,3,4,13, 15,16,17,18)		Although these pins are not connected internally,they should always be left open in order to obtain the most stable oscillation possible.

* Always connect a passthrough capacitor of at least 0.1 μF as close as possible between V_{DD} and GND.

5. Electrical Characteristics

5-1. Absolute Maximum Ratings

Item	Symbol	Conditions	Min.	Max.	Unit
Supply voltage	V_{DD}	Ta=+25 °C	-0.3	7.0	V
Input voltage	V_I		GND-0.3	V_{DD}+0.3	V
Output voltage	V_O		GND-0.3	V_{DD}+0.3	V
Storage temperature	T_{STG}	-	-55	+125	°C

5-2. Operating Condition

Item	Symbol	Conditions	Min.	Max.	Unit
Operating supply voltage	V_{DD}	-	2.5	5.5	V
Data holding voltage	V_{CLK}	-	1.4	5.5	V
Operating temperature	T_{OPR}	No condensation	-40	+85	°C

5-3. Frequency Characteristics

Item	Symbol	Conditions	Max.	Unit
Frequency tolerance	$\Delta f/f_O$	Ta=+25 °C , V_{DD}=5.0 V	5 ± 23 *	$\times 10^{-6}$
Frequency temperature characteristics	Top	-10to+70 °C +25 °C ref	+ 10 / - 120	$\times 10^{-6}$
Frequency voltage characteristics	f/V	Ta=+25 °C , V_{DD}=2.0 to 5.5 V	± 2	$\times 10^{-6}$/V
Oscillation start time	t_{STA}	Ta=+25 °C , V_{DD}=2.5 V	3	s
Aging	fa	Ta=+25 °C , V_{DD}=5 V , first year	± 5	$\times 10^{-6}$

* Monthly deviation: Approx. 1 min.

5-4. DC Characteristics

Unless specified otherwise: V_{DD} = 5 V ± 10 %, Ta = - 40 to +85 °C

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Current consumption(1)	$I_{DD}1$	V_{DD}=5.0 V	CE=L , FOE=L FSEL=H		1.5	3.0	µA
Current consumption(2)	$I_{DD}2$	V_{DD}=3.0 V			1.0	2.0	µA
Current consumption(3)	$I_{DD}3$	V_{DD}=2.0 V			0.5	1.0	µA
Current consumption(4)	$I_{DD}4$	V_{DD}=5.0 V	CE=L , FOE=H FSEL=L		4.0	10.0	µA
Current consumption(5)	$I_{DD}5$	V_{DD}=3.0 V			2.5	6.5	µA
Current consumption(6)	$I_{DD}6$	V_{DD}=2.0 V	No load on the FOUT pin		1.5	4.0	µA
Input voltage	V_{IH}	WR,DATA,CE,CLK, FOE,FSEL pins		0.8 V_{DD}			V
	V_{IL}					0.2 V_{DD}	V
Input off/leak current	I_{OFF}	WR,CE,CLK,FOE,FSEL pins V_{IN} = VDD or GND				0.5	µA
Output voltage	$V_{OH(1)}$	V_{DD}=5.0 V	I_{OH}=-1.0 mA DATA , FOUT pins	4.5			V
	$V_{OH(2)}$	V_{DD}=3.0 V		2.0			V
	$V_{OL(1)}$	V_{DD}=5.0 V	I_{OL}= 1.0 mA DATA , FOUT pins			0.5	V
	$V_{OL(2)}$	V_{DD}=3.0 V				0.8	V
Output load condition (fanout)	N / CL	FOUT pin		2 LSTTL / 30 pF Max.			
Output leak current	I_{OZH}	V_{OUT}=5.5 V DATA , FOUT pins		-1.0		1.0	µA
	I_{OZL}	V_{OUT}=0 V DATA , FOUT pins		-1.0		1.0	µA
Supply voltage detection voltage	V_{DT}	-		1.4	1.7	2.0	V

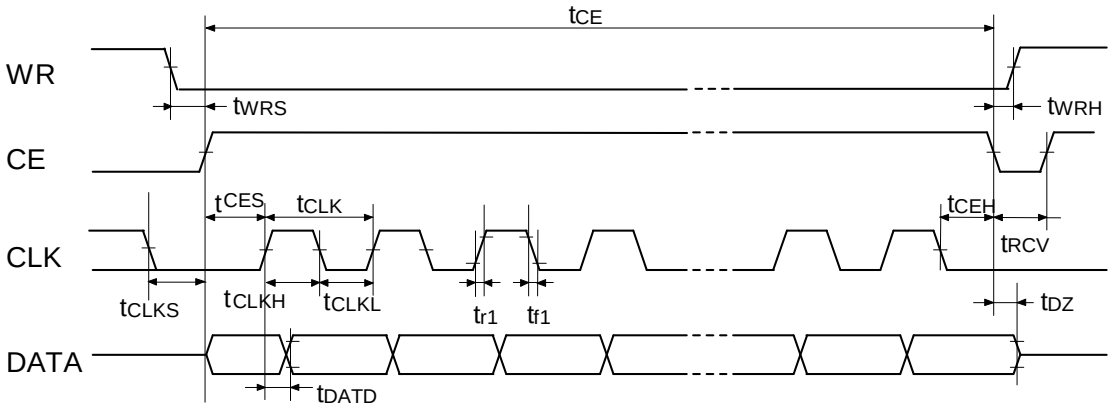
5-5. AC Characteristics

Unless specified otherwise: Ta = - 40 to +85 °C, CL = 50 pF

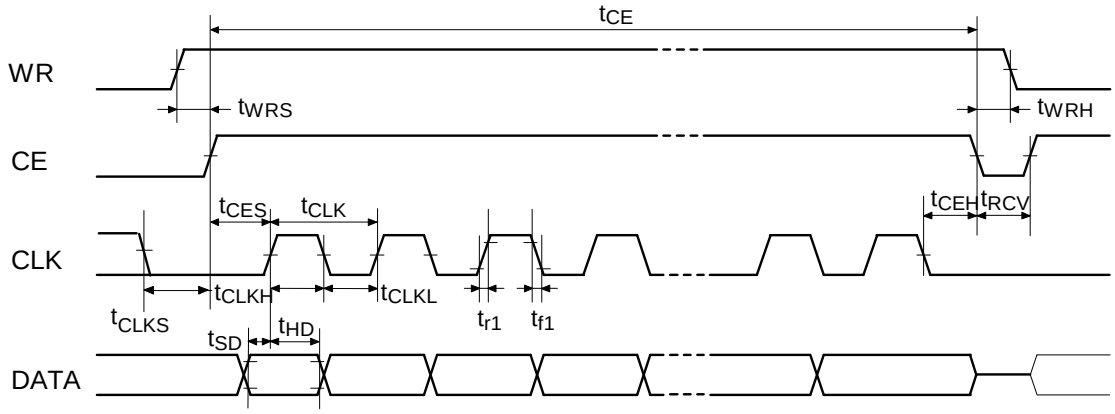
Item	Symbol	V_{DD}=5 V ± 10 %		V_{DD}=3 V ± 10 %		Unit
		Min.	Max.	Min.	Max.	
CLK clock cycle	t_{CLK}	0.75	7800	1.5	7800	µs
CLK low pulse width	t_{CLKL}	0.375	3900	0.75	3900	µs
CLK high pulse width	t_{CLKH}	0.375	3900	0.75	3900	µs
CLK setup time	t_{CLKS}	25		50		ns
CE setup time	t_{CES}	0.375	3900	0.75	3900	µs
CE hold time	t_{CEH}	0.375		0.75		µs
CE enable time	t_{CE}		0.9		0.9	s
Write data setup time	t_{SD}	0.1		0.2		µs
Write data hold time	t_{HD}	0.1		0.1		µs
WR setup time	t_{WRS}	100		100		ns
WR hold time	t_{WRH}	100		100		ns
DATA output delay time	t_{DATD}		0.2		0.4	µs
DATA output floating time	t_{DZ}		0.1		0.2	µs
Clock input rise time	t_{r1}		50		100	ns
Clock input fall time	t_{f1}		50		100	ns
FOUT rise time (CL=30 pF)	t_{r2}		100		200	ns
FOUT fall time (CL=30 pF)	t_{f2}		100		200	ns
Disable time (CL=30 pF)	t_{XZ}		100		200	ns
Enable time (CL=30 pF)	t_{ZX}		100		200	ns
FOUT duty ratio (CL=30 pF)	Duty	40	60	40	60	%
Wait time	t_{RCV}	0.95		1.9		µs

5-6. Timing Charts

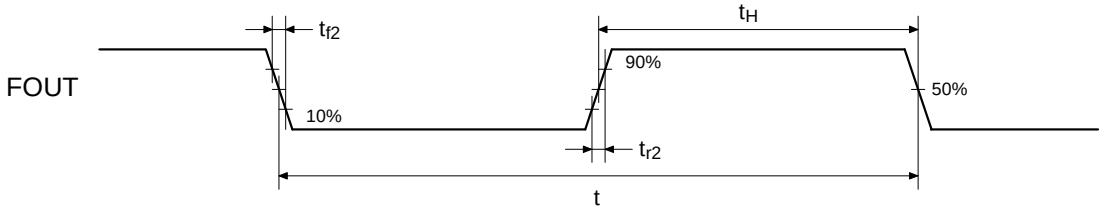
(1) Data read



(2) Data write

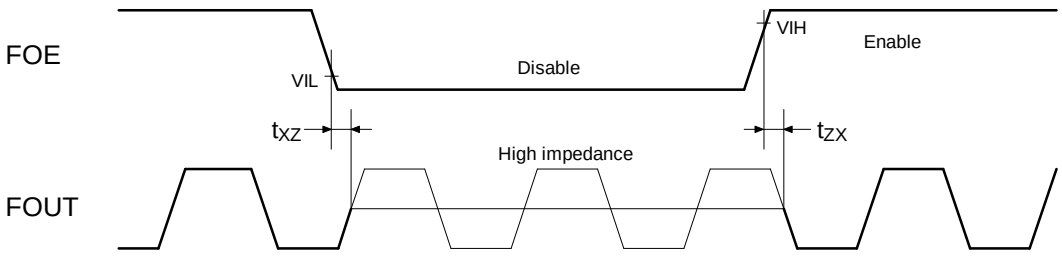


(3) FOUT output



$$Duty = \frac{t_H}{t} \times 100 \ [\%]$$

(4) Disable/enable

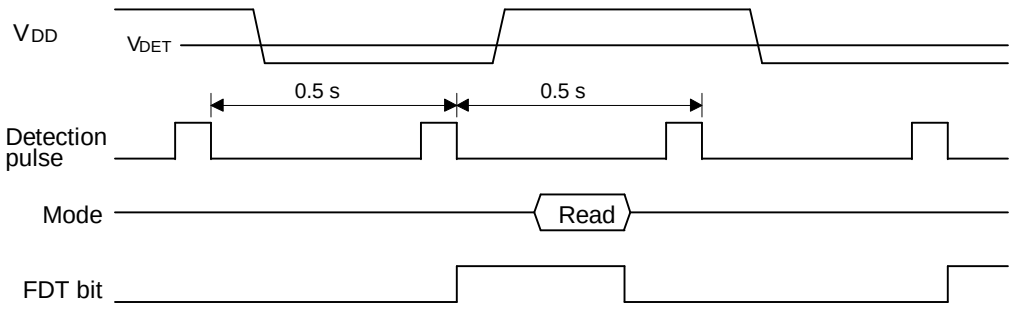


6. Timer Data Organization

- The counter data is BCD code.
- Writes and reads are both performed on an LSB-first basis.

	MSB							LSB
Second (0 to 59)	**FDT**	**s40**	**s20**	**s10**	**s8**	**s4**	**s2**	**s1**
Minutes (0 to 59)	*****	**mi40**	**mi20**	**mi10**	**mi8**	**mi4**	**mi2**	**mi1**
Hour (0 to 23)	*****	*****	**h20**	**h10**	**h8**	**h4**	**h2**	**h1**
Day of the week (1 to 7)					*****	**w4**	**w2**	**w1**
Day (1 to 31)	*****	*****	**d20**	**d10**	**d8**	**d4**	**d2**	**d1**
Month (1 to 12)	**TM**	*****	*****	**mo10**	**mo8**	**mo4**	**mo2**	**mo1**
Year (0 to 99)	**y80**	**y40**	**y20**	**y10**	**y8**	**y4**	**y2**	**y1**

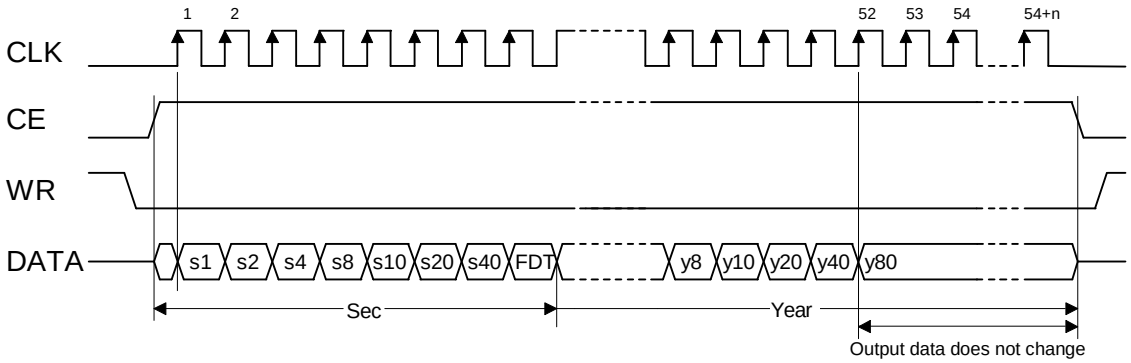
- Calendar counter.
  From 1 Jan 2001 to 31 Dec 2099, it is updated by an automatic calendar function.
  If a year is 4 multiples, it is a leap year, then date is updated
  in order to 28 Feb, 29 Feb, Mar 1.
  Because there is the case that a leap year does not match when using data of year of except the Christian era, please be careful.
  Data of a day of the week run in cycles with 7 from 1.
  A recommended example are 1=Sun, 2=Mon,,,6=Fri, 7=Sat.
- Clock counter. Only 24 hours system is supported.
- ∗bits. These bits are used as memory.
- TM bit. This is a test bit for shipping test. Always clear this bit to “0”.
- FDT bit: Supply voltage detection bit
  - This bit is set to “1” when voltage of 1.7 ±0.3 V or less is detected between V_{DD} and GND.
  - The FDT bit is cleared if all of the digits up to the year digits are read.
  - Although this bit can be both read and written, clear this bit to "0" in case of the write cycle.



The supply voltage detection circuit monitors the supply voltage once every 0.5 seconds; if the supply voltage is lower than the detection voltage value, the FDT bit is set to “1”.

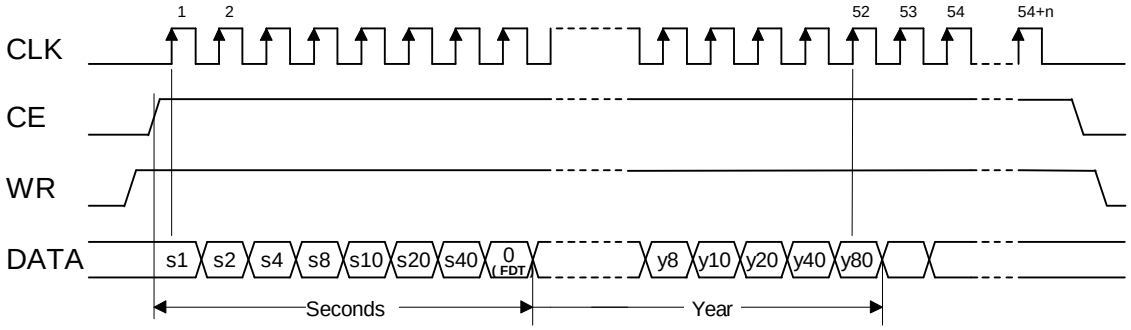
7. Description of Operation

7-1.Data reads



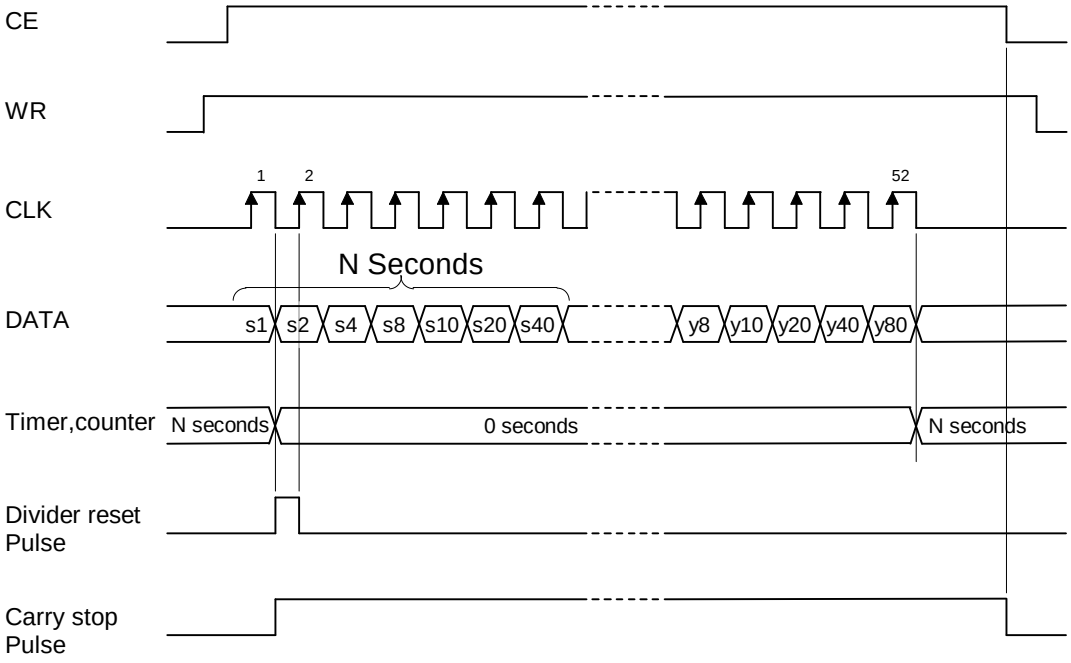
1) When the WR pin is low and the CE pin is high, the RTC enters data output mode.
2) At the first rising edge of the CLK signal, the clock and calendar data are loaded into the shift register and the LSB of the seconds digits is output from the DATA pin.
3) The remaining seconds, minutes, hour, day of the week, day, month, and year data is shifted out, in sequence and in synchronization with the rising edge of the CLK signal, so that the data is output from the DATA pin.
   The output data is valid until the rising edge of the 52nd clock pulse; even if more than 52 clock pulses are input, the output data does not change.
4) If data is required in less than 52 clock pulses, that part of the data can be gotten by setting the CE pin low after the necessary number of clock pulses have been output.
   Example: If only the data from “seconds” to “day of the week” is needed:
   After 28 clock pulses, set the CE pin low in order to get the data from “seconds” to “day of the week.”
5) When performing successive data read operations, a wait (tRCV) is necessary after the CE pin is set low.
6) Note that if an update operation (a one-second carry) occurs during a data read operation, the data that is read will have an error of -1 second.
7) Complete data read operations within tCE (Max.) = 0.9 seconds, as described earlier.

7-2. Data writes



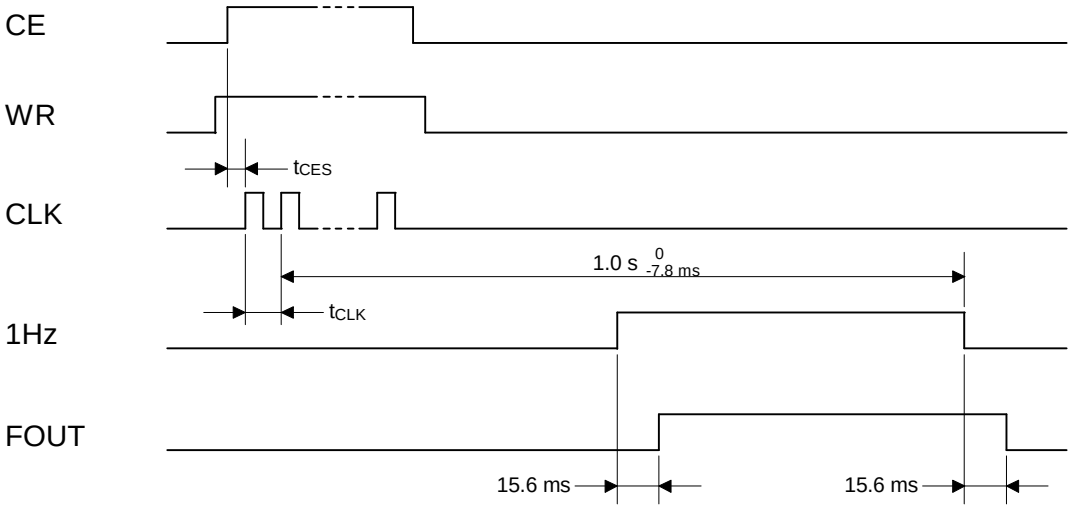
1) RTC 4543 shifts to data input state by condition of WR terminal ="H",CE terminal ="H".
2) Writing-data synchronize to a rising edge of CLK, and it inputs into an RTC from LSB of sec.
3) Inside counter less than second is reset between falling edges of first CLK from a rising edge of next CLK. And update of Clock register is prohibited by the first falling edge of CLK.
4) In writing of data to RTC, all 52 clock is necessary.
   When CE goes to LOW before the 52 bits transmission is completed, there is the possibility that * ,FDT and a year digit were destroyed.
   If a serial communication break occurs, do verify 8 bits of * bit andFDTbit and year data.
5) In a rising edge of 52 clock, all data is written to RTC. Data after 53 bits is ignored.
6) When CE goes to LOW, RTC re-starts update.
   Please finish write access within 0.9 second = tCE (Max.).
7) Between write access and read access, recovery timing(tRCV) is necessary.
   Please do not set the time and date which is non-existence.

7-3. Data writes (Divider Reset)



After the counter is reset, carries to the seconds digit are halted.After the data write operation, the prohibition on carries to the seconds counter is lifted by setting the CE pin low.
Complete data write operations within tCE (Max.) = 0.9 seconds, as described earlier.

7-4. FOUT output and 1 Hz carries

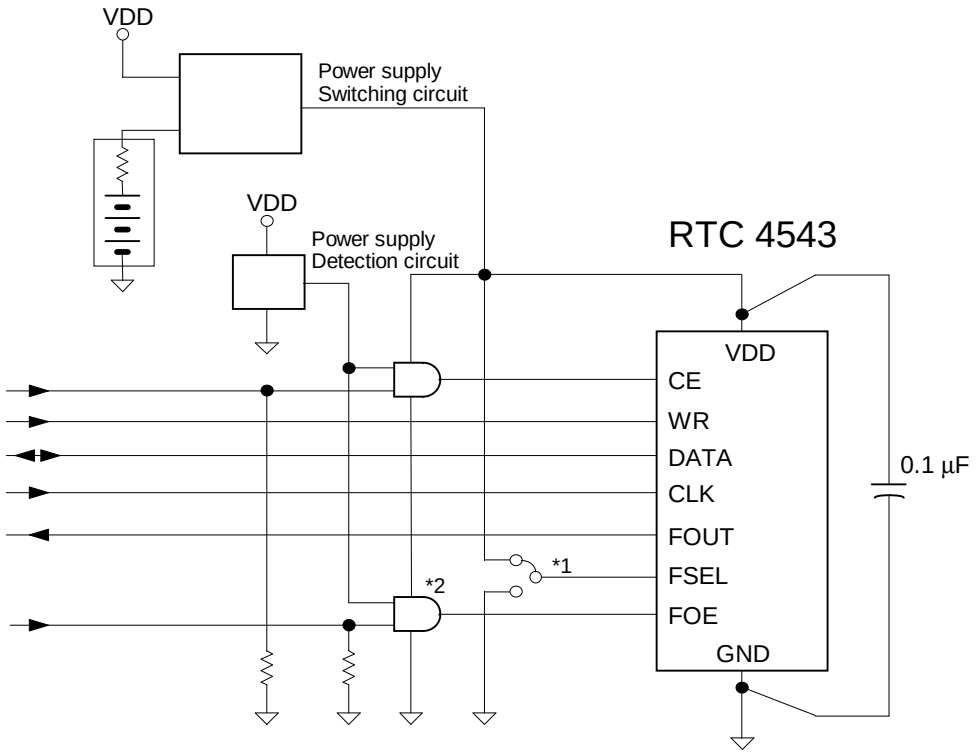


During a data write operation, because a reset is applied to the Devider counter (from the 128 Hz level to the 1 Hz level) after the CE pin goes high during the time between the falling edge of the first clock cycle and the rising edge of the second clock cycle, the length of the first 1 Hz cycle after the data write operation is 1.0 s $^{+0\ /\ -7.8ms}$ +t_{CES}+t_{CLK}. Subsequent cycles are output at 1.0-second intervals.

The 1-Hz signal that is output on FOUT is the internal 1-Hz signal with a 15.6-ms shift applied.

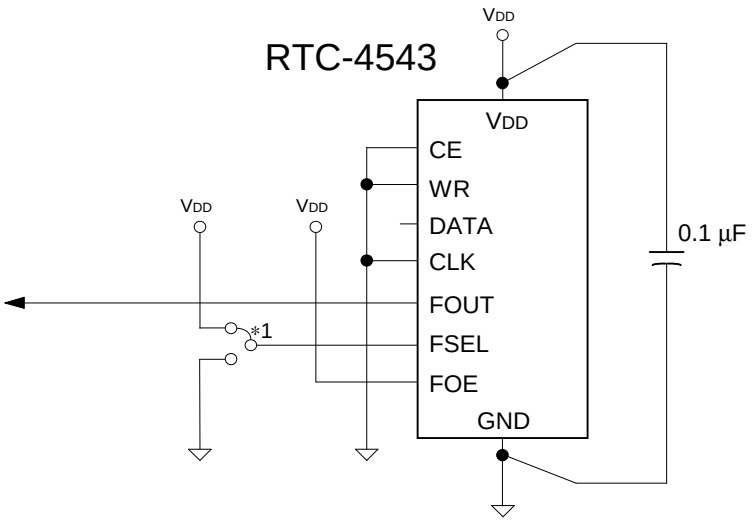
8. Examples of External Circuits

- Example 1. When used as an RTC + clock source



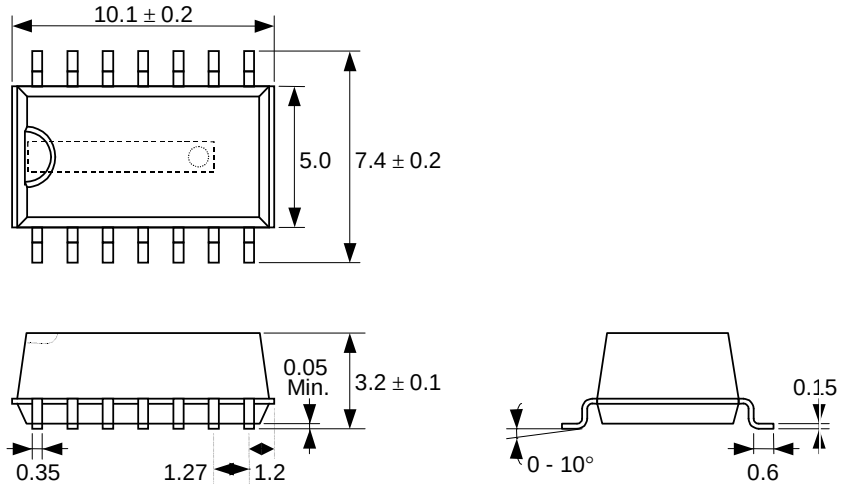
*1: FOUT output frequency setting (High: 1 Hz; low: 32.768 kHz)
*2: Prohibits FOUT output during back up, reducing current consumption.

- Example 2. When used as a clock source (oscillator)



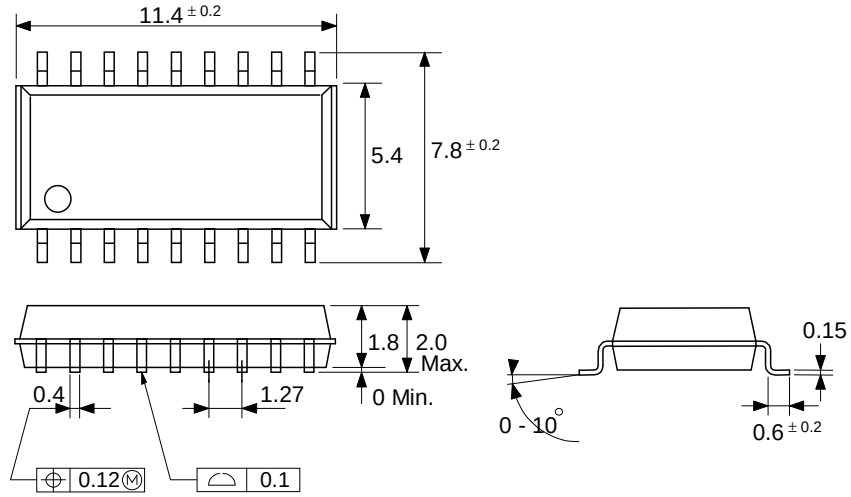
9. External Dimensions

RTC - 4543 SA (SOP-14pin)



∗ The cylinder of the crystal oscillator can be seen in this area (front), but it has no affect on the performance of the device.

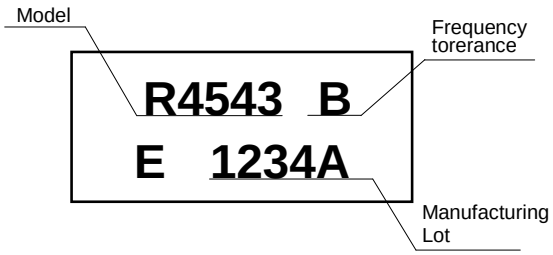
RTC - 4543 SB (SOP-18pin)



10. Layout of Package Markings

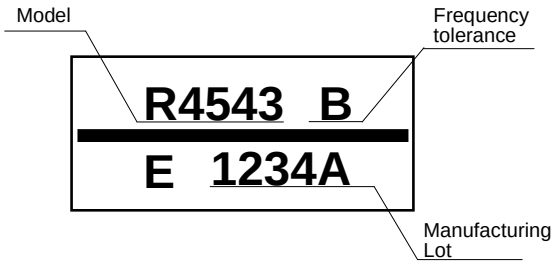
RTC - 4543 SA

(SOP-14pin)



RTC - 4543 SB

(SOP-18pin)



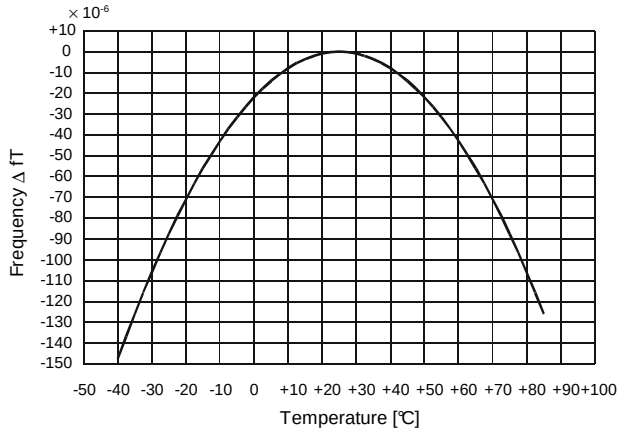
Note :
The markings and their positions as pictured above are only approximations.
These illustrations do not define the details of the style, size, and position of the characters marked on the packages.

11. Reference Data

(1) Example of Frequency-Temperature Characteristics

θ_T = +25 °C Typ.

α = -0.035 × 10^{-6}/ °C ^{2} Typ.



Determining the frequency stability (clock accuracy)

1.The frequency-temperature characteristics can be approximated by the following equation:

$\Delta f_T = \alpha(\theta_T-\theta_X)^2$

Δf_T	: Frequency deviation at any given temperature
α(/°C^2)	: Second-order temperature ((-0.035±0.005)×10^{-6}/°C^2)
θ_T(°C)	: Highest temperature(+25 °C±5 °C)
θ_X(°C)	: Any given temperature

2. In order to determine the clock accuracy, add in the frequency tolerance and the voltage characteristics.

$\Delta f/f = \Delta f/f_0 + \Delta f_T + \Delta fv$

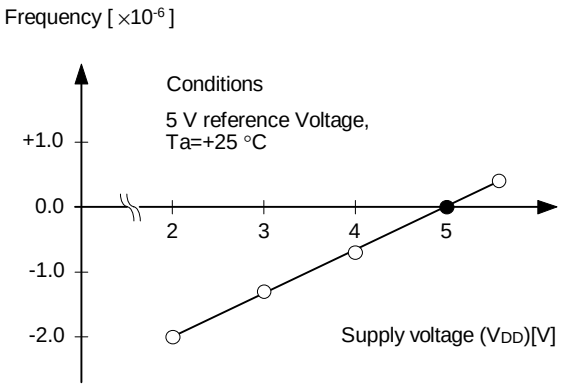
$\Delta f/f$	: Clock accuracy at any given temperature and voltage (frequency stability)
$\Delta f/f_0$	: Frequency accuracy
Δf_T	: Frequency deviation at any given temperature
Δf_V	: Frequency deviation at any given voltage

3. Determining the daily error

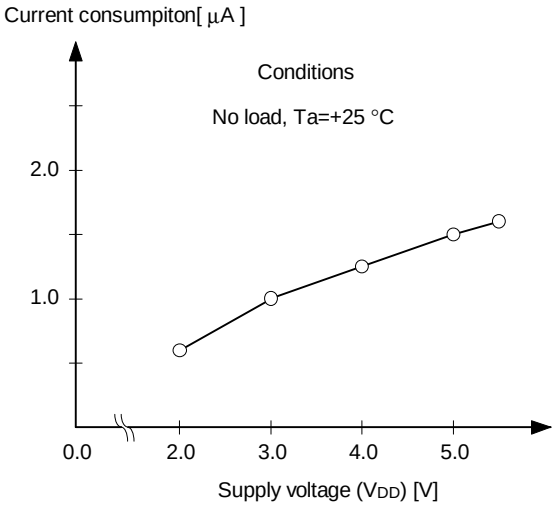
Daily error =$\Delta f/f \times 86400$ (seconds)

With error of 11.574 × 10^{-6}, the error of the clock is about one second per day.

(2)Example of Frequency-Voltage Characteristics



(3)Example of Current Consumption-Voltage Characteristics



Note : This data shows values obtained from a sample lot.

12. Application notes

1) Notes on handling

This module uses a C-MOS IC to realize low power consumption. Carefully note the following cautions when handling.

(1) Static electricity

While this module has built-in circuitry designed to protect it against electrostatic discharge, the chip could still be damaged by a large discharge of static electricity. Containers used for packing and transport should be constructed of conductive materials. In addition, only soldering irons, measurement circuits, and other such devices which do not leak high voltage should be used with this module, which should also be grounded when such devices are being used.

(2) Noise

If a signal with excessive external noise is applied to the power supply or input pins, the device may malfunction or "latch up." In order to ensure stable operation, connect a filter capacitor (preferably ceramic) of greater that 0.1 µF as close as possible to the power supply pins (between VDD and GNDs). Also, avoid placing any device that generates high level of electronic noise near this module.

* Do not connect signal lines to the shaded area in the figure shown in Fig. 1 and, if possible, embed this area in a GND land.

(3) Voltage levels of input pins

When the input pins are at the mid-level, this will cause increased current consumption and a reduced noise margin, and can impair the functioning of the device. Therefore, try as much as possible to apply the voltage level close to VDD or GND.

(4) Handling of unused pins

Since the input impedance of the input pins is extremely high, operating the device with these pins in the open circuit state can lead to unstable voltage level and malfunctions due to noise. Therefore, pull-up or pull-down resistors should be provided for all unused input pins.

2) Notes on packaging

(1) Soldering heat resistance.

If the temperature within the package exceeds +260 °C, the characteristics of the crystal oscillator will be degraded and it may be damaged. The reflow conditions within our reflow profile is recommended. Therefore, always check the mounting temperature and time before mounting this device. Also, check again if the mounting conditions are later changed.

* See Fig. 2 profile for our evaluation of Soldering heat resistance for reference.

(2) Mounting equipment

While this module can be used with general-purpose mounting equipment, the internal crystal oscillator may be damaged in some circumstances, depending on the equipment and conditions. Therefore, be sure to check this. In addition, if the mounting conditions are later changed, the same check should be performed again.

(3) Ultrasonic cleaning

Depending on the usage conditions, there is a possibility that the crystal oscillator will be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, state of the inside of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

(4) Mounting orientation

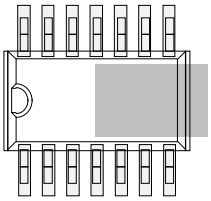
This device can be damaged if it is mounted in the wrong orientation. Always confirm the orientation of the device before mounting.

(5) Leakage between pins

Leakage between pins may occur if the power is turned on while the device has condensation or dirt on it. Make sure the device is dry and clean before supplying power to it.

Fig. 1: Example GND Pattern

RTC - 4543 SA (SOP-14pin)



RTC - 4543 SB (SOP-18pin)

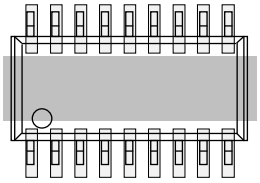
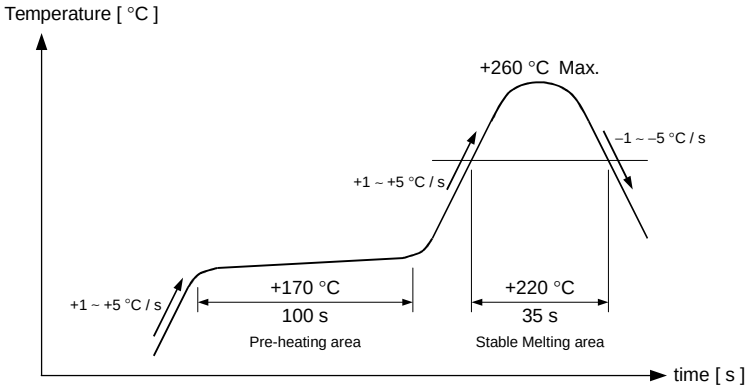


Fig. 2: Soldering Conditions of SMD Products
Air Reflow Profile



Application Manual

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