Product Technical Specification & Customer Design Guidelines

AirPrime Q2687 Refreshed

SIERRA WIRELESS®

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Document History

Version	Date	Updates
001	January 28, 2010	Creation
002	May 04, 2010	Reformatted in the rebranded SWI template.
		Moved the Power Supply Design Requirements to section 9.2 Power Supply
		In section 4 Interfaces: • Updated section 4.7.5 5-wire Serial Interface • Updated section 4.8.1 Pin Description • Updated section 4.8.3 4-wire Serial Interface
		Updated links in section 13.1 Web Site Support.
		Updated Intelligent Embedded Module weight to 8g.
		Updated the RF Component list.
		Removed references to IMP Connector throughout the document.
		Updated Figure 10 Example of a 4-wire SPI Bus Application.
		Updated Power ON information based on Tracker 01626.
		Updated U1 Chip information based on CUS57225.
		Updated antenna gain information.
		Updated FCC ID.
		Updated power consumption values in section 6 Power Consumption.
		Updated Figure 5 Q2687 Refreshed Embedded Module Mechanical Drawing and Figure 6 Maximum Bulk Occupied on the Host Board.
		Updated section 3.1.2 Start-Up Current
		Updated section 4.15 Temperature Sensor Interface
		Updated section 11.1 General Purpose Connector
		Added section 3.4 Conformance with ATEX 94/9/CE Directive
003	June 18, 2010	Updated Figure 21 Example of V24/CMOS Serial Link Implementation for UART1 and Figure 22 Example of a Full Modem V24/CMOS Serial Link Implementation for UART1
		Updated the reference in the last sentence of section 3.2 Mechanical Specifications
		Updated Table 3 Input Power Supply Voltage and Figure 3 Power Supply Ripple Graph.
		Updated Table 8 Signal Comparison between the Q26 Series Intelligent Embedded Modules.
004	August 11, 2010	Updated UART voltage tolerance from 3V to 3.3V in section 4.7 Main Serial Link (UART1).
		Added note for entering Sleep Mode in sections 7.2.1 Embedded Module Configuration and 6 Power Consumption.
		Updated the signal name of pin 22 from GPIO31/SPI1 Load to GPIO31/SPI1-Load.
		Added a note in section 4.3 General Purpose Input/Output, specifying which GPIO is associated with AT+WTBI.
		Deleted section 4.14.4 Recharging.
		Updated section 5.4.3.1 Super Capacitor.
		Added ADC index in Table 72 ADC Pin Description.
		Deleted section 13.2.6 Application Notes as these application notes no longer exits.

Version	Date	Updates
005	October 27, 2010	Deleted Figure 69.
		Updated Table 75 Electrical Characteristics of the DAC.
006	June 20, 2011	Added information for the ESIM version, Q26SM703RD, throughout the document which includes the following: • Added section 4.9.4 Embedded SIM • Added voltage start-up note after Table 3 Input Power Supply Voltage and Table 5 Current Start-Up • Added additional information in Table 10 Electrical Characteristic of a 1.8 Volt Type (1V8) Digital I/O, Table 49 Electrical Characteristics of the Temperature Monitoring Feature, and Table 69 FLASH-LED Status • Added Table 62 Electrical Characteristics of the BAT-RTC Interface (for the Q26SM703RD) • Added Table 77 Power Consumption Without Open AT Application Framework for the Q26SM703RD; Typical Values
		Added section 5.1.6 When ON/~OFF is tied to VBATT.
007	August 17, 2011	Added additional external interrupts in the following tables: • Table 7 General Purpose Connector Pin Description • Table 13 GPIO Pin Description • Table 25 UART1 Pin Description • Table 26 UART2 Pin Description • Table 65 External Interrupt Pin Description • Table 66 Electrical Characteristics of the External Input/Interrupt
		Updated the power consumption values in Table 76 Power Consumption Without Open AT Application Framework for non-ESIM modules; Typical Values.
		Added a note in sections 14.2.7 and 14.2.8 for ATEX compliance.
8.0	February 07, 2012	Updated document reference number.
		Updated Table 1 Q2687 Refreshed Embedded Module Features.
		Updated Table 94 Applicable Standards and Requirements for the Q2687 Refreshed Embedded Module.
8.1	February 08, 2012	Updated legal boilerplates.
9.0	August 15, 2012	Updated the Reset State for pin 30 (CT104-RXD2) and pin 32 (~CT106-CTS2) in the following tables: • Table 7 General Purpose Connector Pin Description • Table 13 GPIO Pin Description • Table 26 UART2 Pin Description • Table 65 External Interrupt Pin Description
10.0	December 19, 2012	Added a note regarding ADC performance in section 5.9.2.
		Updated document list in section 13.2 Reference Documents
11.0	February 04, 2013	Updated: • Figure 5 Q2687 Refreshed Embedded Module Mechanical Drawing • Figure 6 Maximum Bulk Occupied on the Host Board
		Added ADC3 restriction in section 4.15 Temperature Sensor Interface

Version	Date	Updates
12.0	March 17, 2014	Updated: • Section 1.7 Environment and Mechanics • Internal bias voltage in: ▪ Figure 32 Example of a MIC2 Differential Connection with LC Filter ▪ Figure 33 Example of a MIC2 Differential Connection without an LC Filter ▪ Figure 34 Example of a MIC2 Single-Ended Connection with LC Filter ▪ Figure 35 Example of a MIC2 Single-Ended Connection without an LC Filter
13.0	November 25, 2014	Updated: • Table 7 General Purpose Connector Pin Description • 4.7.5 4-wire Serial Interface • 4.7.6 2-wire Serial Interface • 10.1 Serial Link Access
		Added 4.7.4 8-wire Serial Interface

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1. Introduction

The Q2687 Refreshed Intelligent Embedded Module is a self-contained E-GSM/DCS/GSM850/PCS GPRS/EGPRS 900/1800/850/1900 quad-band embedded module. It supports Open AT Application Framework, the world's most comprehensive cellular development environment which allows embedded standard ANSI C applications to be natively executed directly on the embedded module. For more information about Open AT Application Framework, refer to the documents listed in section 13.2 Reference Documents.

The **Q26SM703RD** is the embedded SIM (ESIM) version of the Q2687 Refreshed. It allows the use of two different SIMs – an external SIM and an embedded SIM. Note that the ESIM application has to be personalized by the card-maker.

Note that this document only covers the Q2687 Refreshed Intelligent Embedded Module and does not cover the programmable capabilities available through Open AT Application Framework.

1.1. Physical Dimensions

- Length: 40 mm
- Width: 32.2 mm
- Thickness: 4 mm
- Weight: 8g

Note: The physical dimensions mentioned above do not include the shielding pins.

1.2. General Features

The following table lists the Q2687 Refreshed embedded module features.

Table 1. Q2687 Refreshed Embedded Module Features

Feature	Description
Shielding	The Q2687 Refreshed embedded module has complete body shielding.
Intelligent Embedded Module Control	• Full set of AT commands for GSM/GPRS/EGPRS including GSM 07.07 and 07.05 AT command sets • Status indication for GSM
GSM/DCS Output Power	• Class 4 (2 W) for GSM 850 and E-GSM • Class 1 (1 W) for DCS and PCS
GPRS	• GPRS multislot class 10 • Multislot class 2 supported • PBCCH support • Coding schemes: CS1 to CS4
EGPRS	• EGPRS multislot class 10 • Multislot class 2 supported • PBCCH support • Coding schemes MCS1 to MCS9

Feature	Description
Voice	• GSM Voice Features with Emergency calls 118 XXX • Full Rate (FR)/ Enhanced Full Rate (EFR) / Half Rate (HR) / Adaptive Multi Rate (AMR) • Echo cancellation and noise reduction • Full duplex Hands free
SMS	• SMS MT, MO • SMS CB • SMS storage into SIM card
GSM Supplementary Services	• Call Forwarding, Call Barring • Multiparty • Call Waiting, Call Hold • USSD
Data/Fax	• Data circuit asynchronous, transparent, and non-transparent up to 14400 bits/s • Fax Group 3 compatible
SIM Interface	• 1.8V/3V SIM interface • 5V SIM interfaces are available with external adaptation • SIM Tool Kit Release 99
Real Time Clock	Real Time Clock (RTC) with calendar and alarm

1.3. GSM/GPRS/EGPRS Features

- 2-Watt EGSM – GPRS 900/850 radio section running under 3.6 volts
- 1-Watt GSM-GPRS1800/1900 radio section running under 3.6 volts
- 0.5-Watt EGPRS 900/850 radio section running under 3.6 volts
- 0.4-Watt EGPRS 1800/1900 radio section running under 3.6 volts
- Hardware GSM/GPRS class 10 and EGPRS class 10 capable

1.4. Interfaces

- Digital section running under 2.8V and 1.8V
- 3V/1V8 SIM interface
- Complete Interfacing:
  - Power supply
  - Serial link
  - Analog audio
  - PCM digital audio
  - SIM card
  - Keyboard
  - USB 2.0 slave
  - Serial LCD (not available with AT commands)
  - Parallel port for specific applications (under Open AT control only)

1.5. Operating System

- Real Time Clock (RTC) with calendar
- Battery charger
- Echo cancellation + noise reduction (quadri codec)
- Full GSM or GSM/GPRS/EGPRS Operating System stack

1.6. Connection Interfaces

The Q2687 Refreshed Intelligent Embedded Module has four external connections:

- Three for RF circuit:
  - UFL connector
  - Soldered connection
  - Precidip connection
- One for baseband signals:
  - 100-pin I/O connector (compatible with Q2686 and Q2687 embedded modules)

1.7. Environment and Mechanics

1.7.1. RoHS Directive Compliant

The Q2687 Refreshed embedded module is compliant with RoHS Directive 2011/65/EU which sets limits for the use of certain restricted hazardous substances. This directive states that “from 1st July 2006, new electrical and electronic equipment put on the market does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE)”.

1.7.2. Disposing of the Product

This electronic product is subject to the EU Directive 2012/19/EU for Waste Electrical and Electronic Equipment (WEEE). As such, this product must not be disposed of at a municipal waste collection point. Please refer to local regulations for directions on how to dispose of this product in an environmental friendly manner.

2. Functional Specifications

2.1. Functional Architecture

The global architecture of the Q2687 Refreshed Embedded Module is described in the figure below.

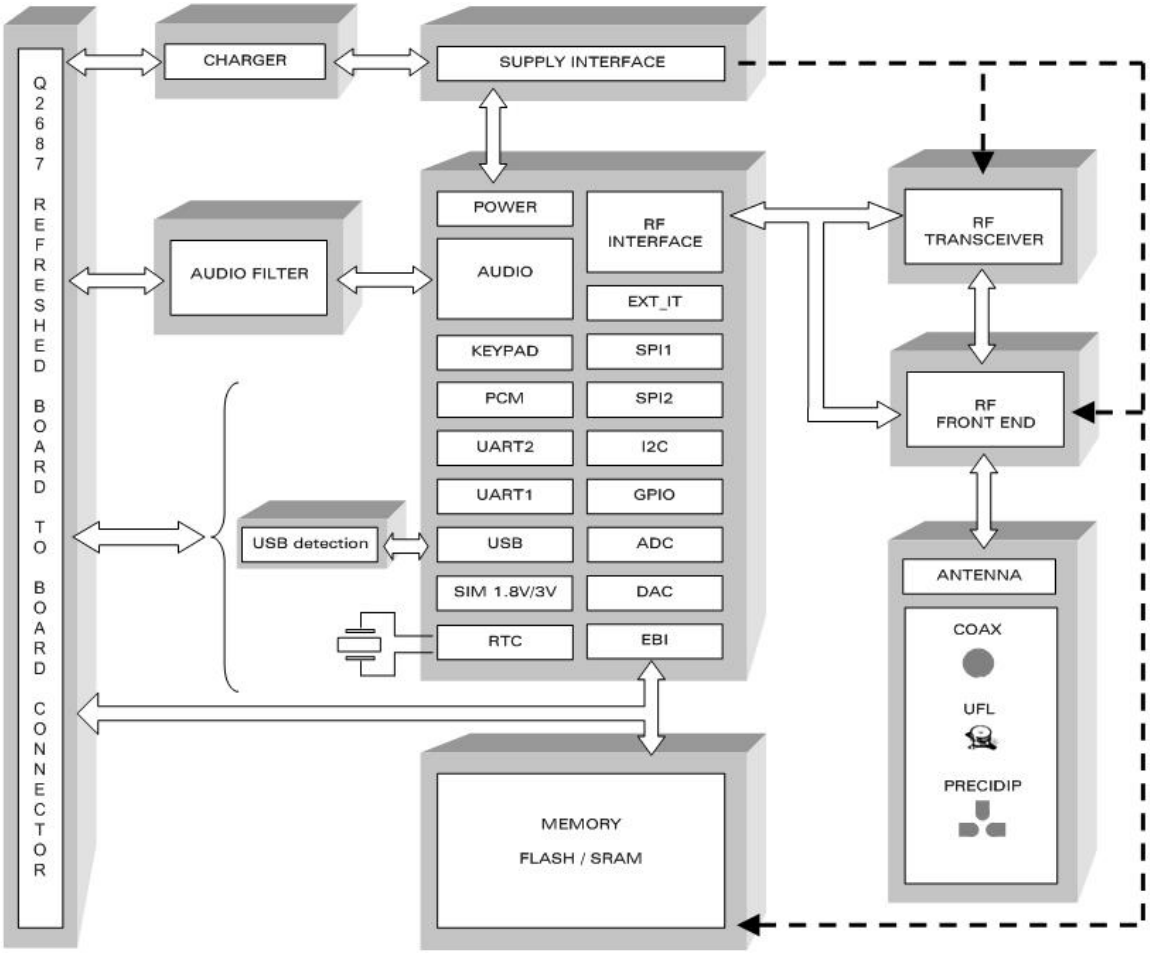


Figure 1. Functional Architecture

2.1.1. RF Functionalities

The Radio Frequency (RF) functionalities of the Q2687 Refreshed embedded module complies with the Phase II EGSM 900/DCS 1800 and GSM 850/PCS 1900 recommendations. The frequency range for the transmit band and receive band are given in the table below.

Table 2. List of RF Frequency Ranges

RF Bandwidth	Transmit Band (Tx)	Receive Band (Rx)
GSM 850	824 to 849 MHz	869 to 894 MHz
E-GSM 900	880 to 915 MHz	925 to 960 MHz
DCS 1800	1710 to 1785 MHz	1805 to 1880 MHz
PCS 1900	1850 to 1910 MHz	1930 to 1990 MHz

The Radio Frequency (RF) component is based on a specific quad-band chip that includes the following:

- Quad-band LNAs (Low Noise Amplifier)
- Digital Low-IF Receiver
- Offset PLL/PL (Phase Locked Loop and Polar Loop) transmitter
- Frequency synthesizer
- Digitally controlled crystal oscillator (DCXO)
- Tx/Rx FEM (Front-End module) for quad-band GSM/GPRS/EGPRS

2.1.2. Baseband Functionalities

The digital part of the Q2687 Refreshed embedded module is composed of a **PCF5213 PHILIPS chip**. This chipset uses a 0.18µm mixed technology CMOS, which allows massive integration as well as low current consumption.

2.2. Operating System

The Q2687 Refreshed Embedded Module is Open AT Application Framework compliant. With Open AT Application Framework, customers can embed their own applications with the Q2687 Refreshed embedded module and turn the Q2687 Refreshed embedded module into a solution for their specific market need.

The operating system allows for the Q2687 Refreshed Embedded Module to be controlled by AT commands. However, some interfaces in the Q2687 Refreshed embedded module may still not be available even with AT command control as these interfaces are dependent on the peripheral devices connected to the Q2687 Refreshed embedded module.

3. Technical Specifications

3.1. Power Supply

The power supply is one of the key issues in the design of a GSM terminal. Due to the burst emission in GSM/GPRS, the power supply must be able to deliver high current peaks in a short time. During these peaks, the ripple (U_{ripp}) on the supply voltage must not exceed a certain limit (refer to Table 3 Input Power Supply Voltage).

Listed below are the corresponding radio burst rates in connected mode:

- GSM/GPRS class 2 terminals emit 577µs radio bursts every 4.615ms (see Figure 2 Power Supply During Burst Emission)
- GPRS class 10 terminals emit 1154µs radio bursts every 4.615ms

In connected mode, the RF Power Amplifier current (2.0A peak in GSM /GPRS mode) flows with a ratio of:

- 1/8 of the time (around 577µs every 4.615ms for GSM /GPRS cl 2 – 2RX/1TX)

  and

- 2/8 of the time (around 1154µs every 4.615ms for GSM /GPRS cl 10 – 3RX/2TX)

  with the rising time at around 10µs.

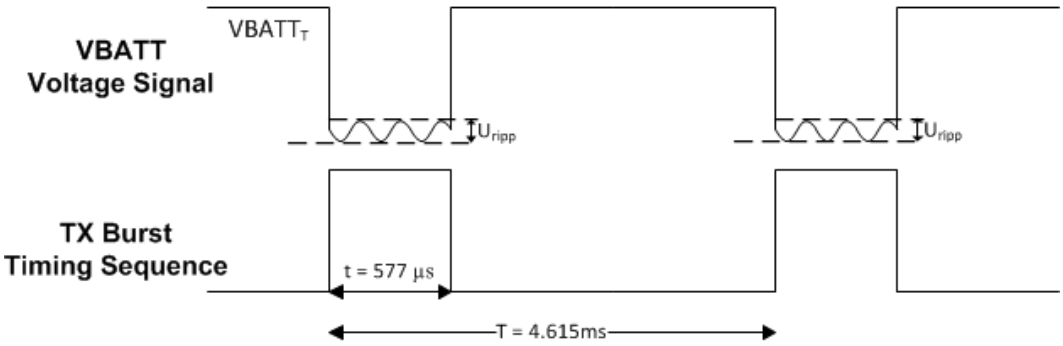


Figure 2. Power Supply During Burst Emission

Only VBATT (external power supply source) input is necessary to supply the Q2687 Refreshed embedded module. VBATT also provides for the following functions:

- Directly supplies the RF components with 3.6V. (Note that it is essential to keep a minimum voltage ripple at this connection in order to avoid any phase error or spectrum modulation degradation. On the other hand, insufficient power supply could dramatically affect some RF performances such as TX power, modulation spectrum, EMC performance, spurious emission and frequency error.)
- Internally used to provide through several regulators, the power supplies VCC_2V8 and VCC_1V8, which are needed for the baseband signals.

The Q2687 Refreshed embedded module shielding case is the grounding. The ground must be connected on the motherboard through a complete layer on the PCB.

The following table describes the electrical characteristics of the input power supply voltage that will guarantee nominal functioning of the Q2687 Refreshed embedded module.

Table 3. Input Power Supply Voltage

	V_{MIN}	V_{NOM}	V_{MAX}	Ripple Max (U_{ripp})	I_{peak} Max
VBATT	3.2V[1,2,3]	3.6V	4.8V	300mVpp (freq < 10kHz) 40mVpp (10kHz < freq < 200kHz) 3mVpp (freq > 200kHz)	2.0A

1: This value must be guaranteed during the burst (with 2.0A Peak in GSM, GPRS or EGPRS mode)

2: Maximum operating Voltage Standing Wave Ratio (VSWR) 2:1.

3: The minimum start-up voltage must be 3.25V for the Embedded SIM version, Q26SM703RD.

Note: The ESIM version of the Q2687 Refreshed requires at least 3.25V start-up voltage.

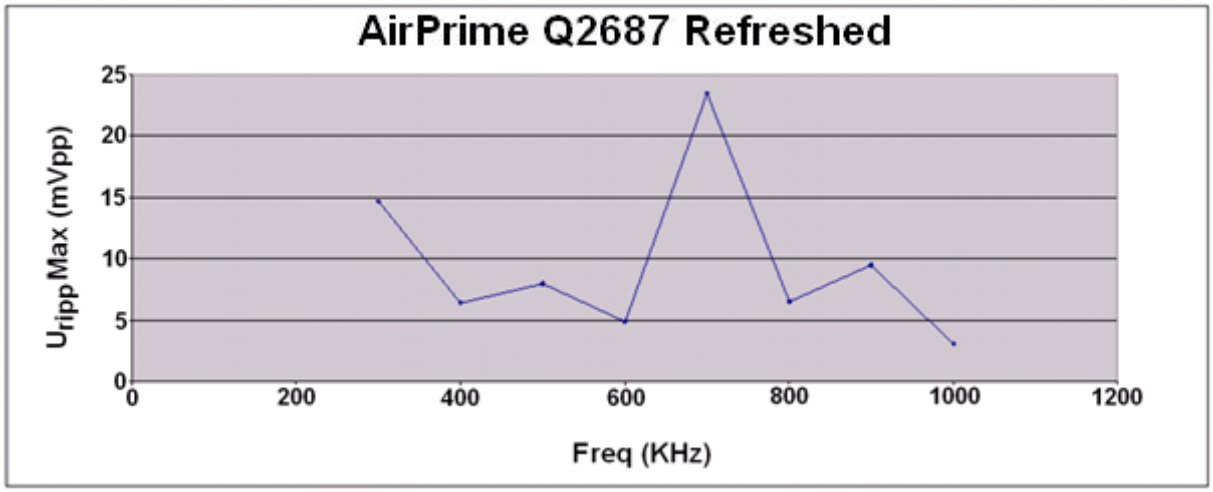


Figure 3. Power Supply Ripple Graph

When the Q2687 Refreshed embedded module is supplied with a battery, the total impedance (battery + protections + PCB) should be less than 150 mΩ.

Caution: *When the Q2687 Refreshed embedded module is in Alarm mode or Off mode, no voltage has to be applied on any pin of the 100-pin connector except on VBATT (pins 1 to 4), BAT-RTC (pin 7) for RTC operation or ON/~OFF (pin 19) to power-ON the Q2687 Refreshed embedded module.*

3.1.1. Power Supply Pin-Out

Table 4. Power Supply Pin-Out

Signal	Pin Number
VBATT	1, 2, 3, 4
GND	Shielding

The grounding connection is made through the shielding; therefore the four leads must be soldered to the ground plane.

3.1.2. Start-Up Current

During the initial second following Power ON, a peak of current appears. This peak of current is called "$I_{Startup}$ current" and has a duration of about 165ms (typical).

Figure 4 Start-up Current Waveform shows the current waveform and identifies the peak considered as the start-up current.

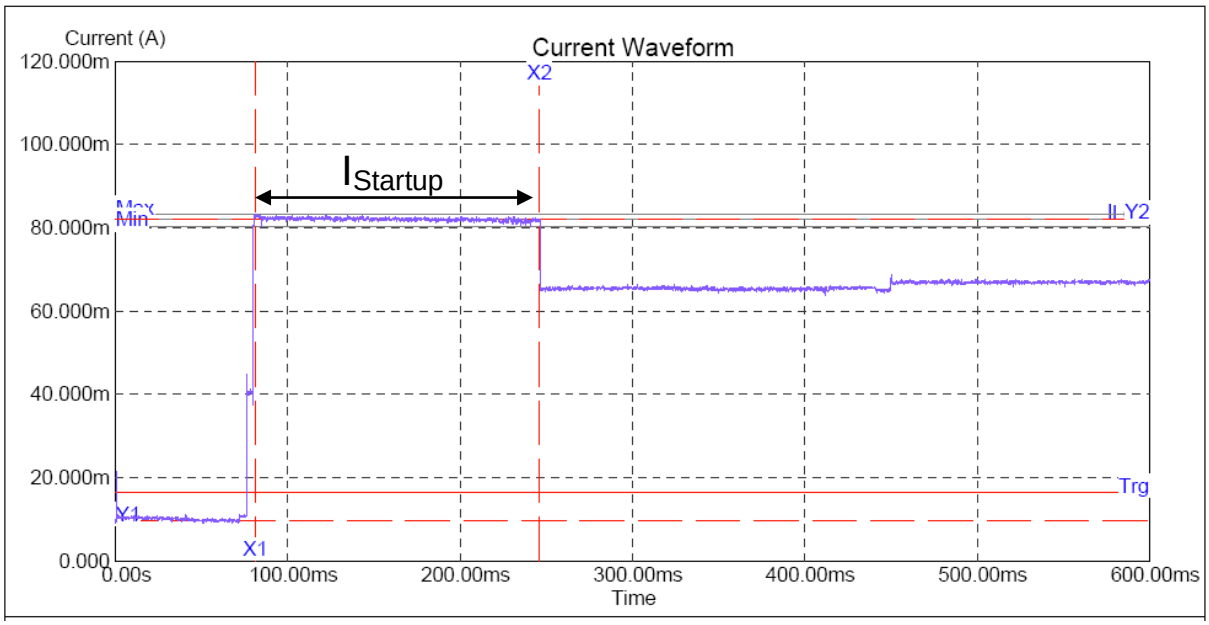


Figure 4. Start-up Current Waveform

In this condition, we can consider the following results:

Table 5. Current Start-Up

Current Peak at Ambient Temperature (25°C)	VBATTmin (3.2V)	VBATTmin (3.25V) with the Q26SM703RD*	VBATTtyp (3.6V)	VBATTmax (4.8V)
$I_{Startup}$	90mA	89mA	82mA	65mA

* The minimum start-up voltage must be 3.25V for the Embedded SIM version, Q26SM703RD.

Note: The ESIM version of the Q2687 Refreshed requires at least 3.25V start-up voltage.

3.1.3. Decoupling of Power Supply Signals

Decoupling capacitors on VBATT lines are embedded in the Q2687 Refreshed embedded module, so it should not be necessary to add decoupling capacitors close to the embedded module.

However, in case of EMI/RFI problems, the VBATT signal may require some EMI/RFI decoupling – parallel 33pF capacitors close to the embedded module or a serial ferrite bead (or both to get better results). Low frequency decoupling capacitors (22µF to 100µF) can be used to reduce TDMA noise (217Hz).

Caution: *When ferrite beads are used, the recommendation given for the power supply connection must be carefully followed (high current capacity and low impedance).*

3.2. Mechanical Specifications

The Q2687 Refreshed Embedded Module has a complete self-contained shield and the mechanical specifications are shown in the figure below, which also specifies the following:

- The area needed for the Q2687 Refreshed embedded module to fit in an application
- The drill template for the four pads to be soldered on the application board
- The dimensions and tolerance for correctly placing the 100-pin female connector on the application board

It is strongly recommended to plan a free area (no components) around the Q2687 Refreshed embedded module in order to facilitate the removal/re-assembly of the embedded module on the application board.

Also take note that when transmitting, the Q2687 Refreshed Embedded Module produces heat (due to the internal Power Amplifier). This heat will generate a temperature increase and may warm the application board on which the Q2687 Refreshed embedded module is soldered. This is especially true for GPRS Class 10 use in low band. The Q2687 Refreshed Embedded Module's built-in temperature sensor can be used to monitor the temperature inside the module. For more information, refer to section 4.15 Temperature Sensor Interface.

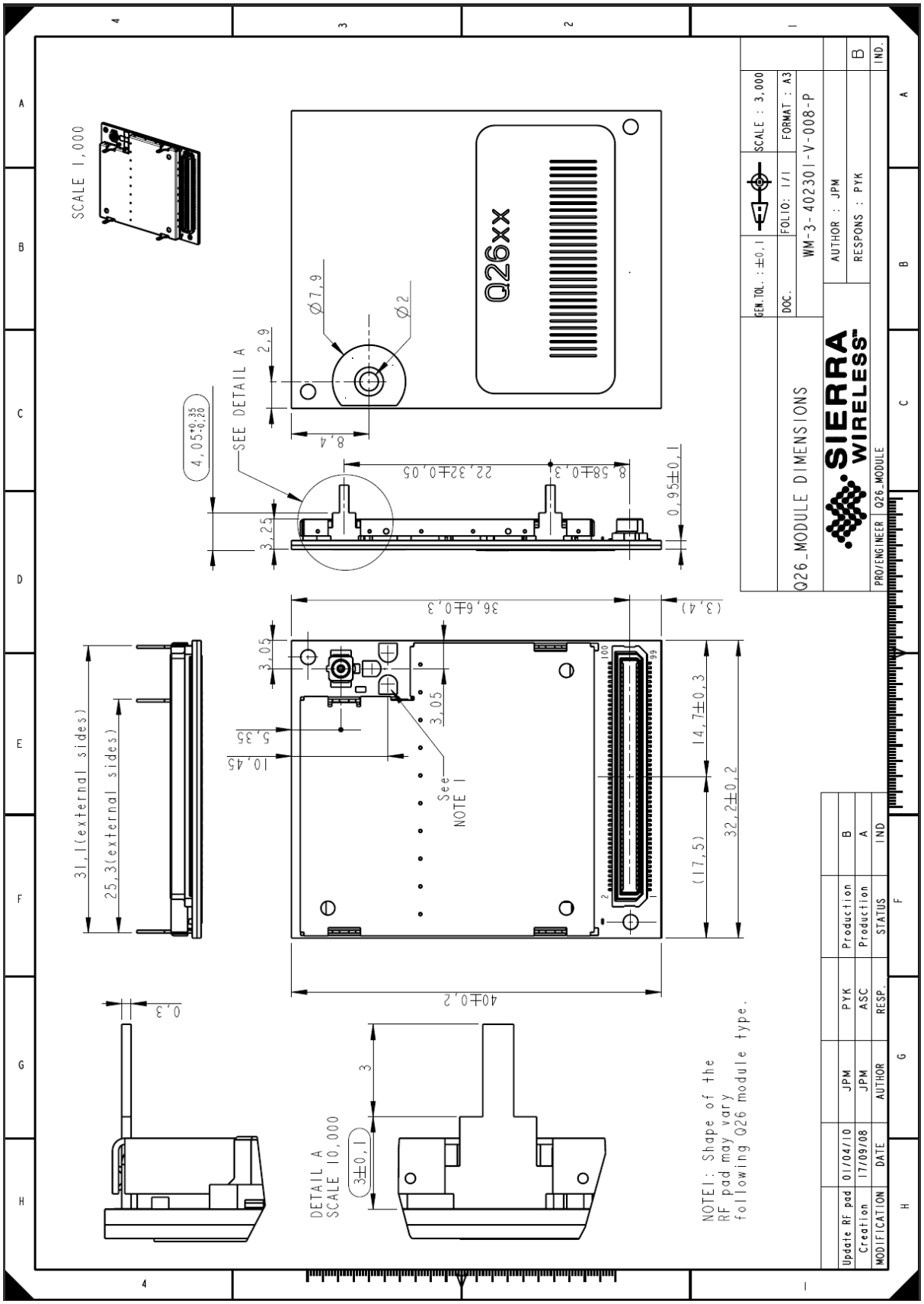


Figure 5. Q2687 Refreshed Embedded Module Mechanical Drawing

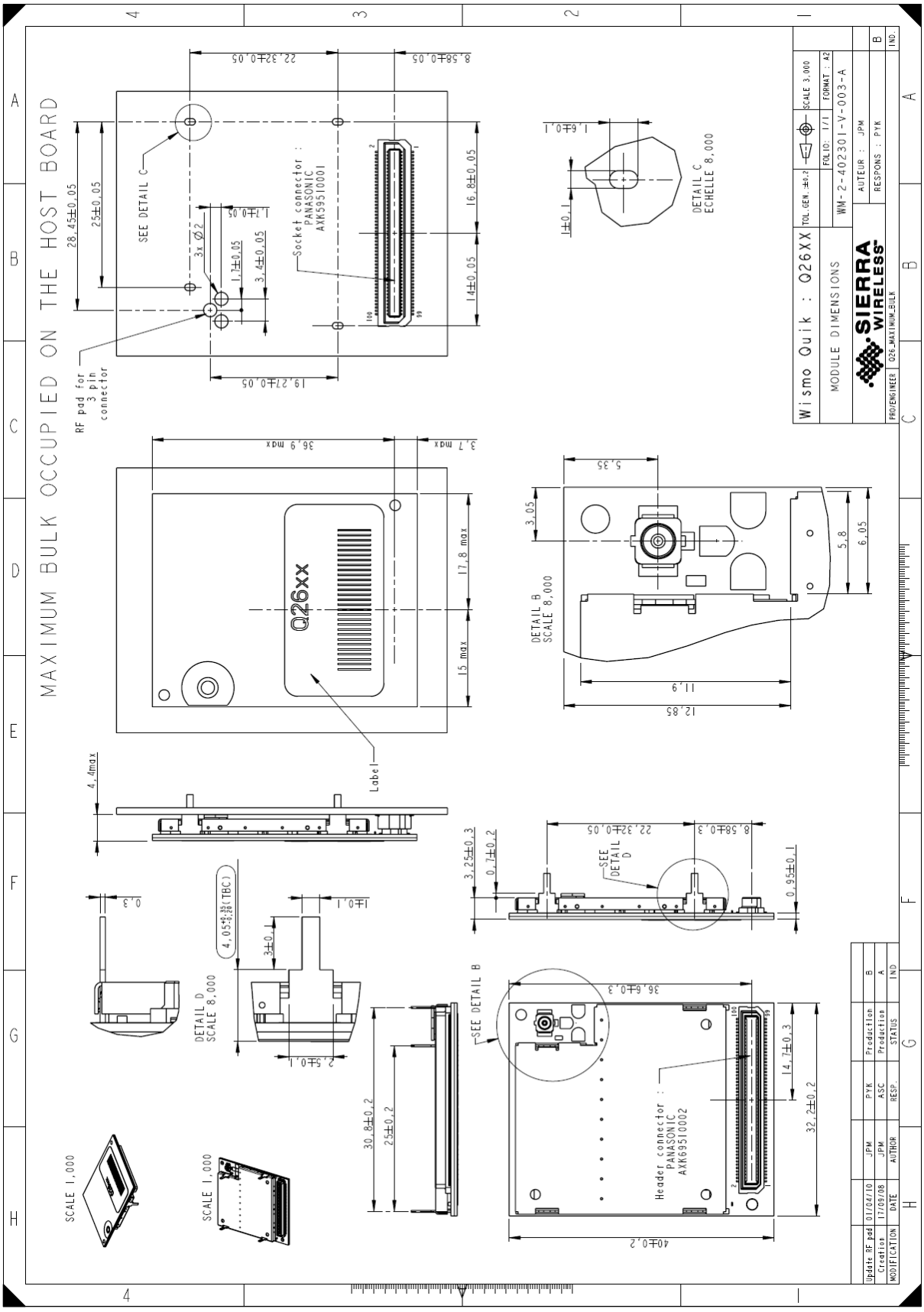


Figure 6. Maximum Bulk Occupied on the Host Board

3.3. Firmware Upgrade

The firmware upgrade process consists of downloading GSM/GPRS/EGPRS software into the corresponding internal flash memories of the Q2687 Refreshed Intelligent Embedded Module.

Downloading is done through the GSM Main Serial link port (UART1) connected to a PC using the XMODEM protocol.

A specific AT command, **AT+WDWL**, is used to start the download. For more information, refer to document [2] Firmware 7.43 AT Commands Manual.

Access to the following UART1 main serial link signals are required to carry out downloading:

- CT103-TXD1
- CT104-RXD1
- ~CT106-CTS1
- ~CT105-RTS1
- GND

Consequently, it is very important to plan and define easy access to these signals during the hardware design of the application board. For more information about these signals, refer to section 4.7 Main Serial Link (UART1).

3.4. Conformance with ATEX 94/9/CE Directive

To evaluate the conformity of a product using the Q2687 Refreshed with ATEX 94/9/CE directive, the integrator must take into account the following data from the Q2687 Refreshed:

- Sum of all capacitors: 90µF
- Sum of all inductors: 14µH
- Biggest single capacitor: 27µF
- Biggest single inductor: 12µH

4. Interfaces

Caution: *Some of the Embedded Module interface signals are multiplexed in order to limit the number of pins but this architecture includes some restrictions.*

4.1. General Purpose Connector (GPC)

A 100-pin connector is provided to interface the Q2687 Refreshed Intelligent Embedded Module with a board containing either a serial or parallel LCD module; a keyboard, a SIM connector or a battery connection.

The following table lists the interfaces and signals available on the GPC and specifies whether these interfaces and signals are driven by AT Command, Open AT or both.

Table 6. Available Interfaces and Signals

Name	Driven by AT commands	Driven by Open AT
Serial Interface		✓
Parallel Interface		✓
Keyboard Interface	✓	✓
Main Serial Link	✓	✓
Auxiliary Serial Link	✓	✓
SIM Interface	✓	✓
General Purpose IO	✓	✓
Analog to Digital Converter	✓	✓
Analog Audio Interface	✓	✓
PWM / Buzzer Output	✓	✓
Battery Charging Interface	✓	✓
External Interruption	✓	✓
BAT-RTC (Backup Battery)		
LED0 signal	✓	✓
Digital Audio Interface (PCM)		✓
USB 2.0 Interface	✓	✓

4.1.1. Pin Description

Refer to the following table for the pin description of the general purpose connector.

Table 7. General Purpose Connector Pin Description

Pin #	Signal Name		I/O Type	Voltage	I/O*	Reset State	Description	Dealing with Unused Pins
	Nominal	Mux						
1	ADC0/VBATT			VBATT	I		Power Supply	
2	ADC0/VBATT			VBATT	I		Power Supply	
3	ADC0/VBATT			VBATT	I		Power Supply	
4	ADC0/VBATT			VBATT	I		Power Supply	
5	VCC_1V8			VCC_1V8	O		1.8V Supply Output	NC
6	CHG-IN			CHG-IN	I		Charger input	NC
7	BAT-RTC			BAT-RTC	I/O		RTC Battery connection	NC
8	CHG-IN			CHG-IN	I		Charger input	NC
9	SIM-VCC			1V8 or 3V	O		SIM Power Supply	
10	VCC_2V8			VCC_2V8	O		2.8V Supply Output	NC
11	SIM-IO			1V8 or 3V	I/O	Pull-up (about 10kΩ)	SIM Data	
12	SIMPRES	GPIO18		VCC_1V8	I	Z	SIM Detection	NC
13	~SIM-RST			1V8 or 3V	O	0	SIM reset Output	
14	SIM-CLK			1V8 or 3V	O	0	SIM Clock	
15	BUZZER0			Open Drain	O	Z	Buzzer Output	NC
16	BOOT			VCC_1V8	I		Not Used	Add a test point / a jumper/ a switch to VCC_1V8 (Pin 5) in case Download Specific mode is used (See product specification for details)

Pin #	Signal Name		I/O Type	Voltage	I/O*	Reset State	Description	Dealing with Unused Pins
	Nominal	Mux						
17	LED0			Open Drain	O	1 and Undefined	LED0 Output	NC
18	~RESET			VCC_1V8	I/O		RESET Input	NC or add a test point
19	ON/~OFF			VBATT	I		ON / ~OFF Control	
20	ADC1/BAT-TEMP			Analog	I		Analog temperature	Pull to GND
21	ADC2			Analog	I		Analog to Digital Input	Pull to GND
22	GPIO31/ SPI1-Load			VCC_2V8	I/O	Z		NC
23	SPI1-CLK	GPIO28		VCC_2V8	O	Z	SPI1 Clock	NC
24	SPI1-I	GPIO30		VCC_2V8	I	Z	SPI1 Data Input	NC
25	SPI1-IO	GPIO29		VCC_2V8	I/O	Z	SPI1 Data Input / Output	NC
26	SPI2-CLK	GPIO32		VCC_2V8	O	Z	SPI2 Clock	NC
27	SPI2-IO	GPIO33		VCC_2V8	I/O	Z	SPI2 Data Input / Output	NC
28	GPIO35/SPI2-Load			VCC_2V8	I/O	Z		NC
29	SPI2-I	GPIO34		VCC_2V8	I	Z	SPI2 Data Input	NC
30	CT104-RXD2	GPIO15 / INT4		VCC_1V8	O	0	Auxiliary RS232 Receive	Add a test point for debugging
31	CT103-TXD2	GPIO14		VCC_1V8	I	Z	Auxiliary RS232 Transmit	Pull-up to VCC_1V8 with 100kΩ and add a test point for debugging
32	~CT106-CTS2	GPIO16		VCC_1V8	O	0	Auxiliary RS232 Clear To Send	Add a test point for debugging
33	~CT105-RTS2	GPIO17		VCC_1V8	I	Z	Auxiliary RS232 Request To Send	Pull-up to VCC_1V8 with 100kΩ and add a test point for debugging
34	MIC2N			Analog	I		Micro 2 Input Negative	NC

Pin #	Signal Name		I/O Type	Voltage	I/O*	Reset State	Description	Dealing with Unused Pins
	Nominal	Mux						
35	SPK1P			Analog	O		Speaker 1 Output Positive	NC
36	MIC2P			Analog	I		Micro 2 Input Positive	NC
37	SPK1N			Analog	O		Speaker 1 Output Negative	NC
38	MIC1N			Analog	I		Micro 1 Input Negative	NC
39	SPK2P			Analog	O		Speaker 2 Output Positive	NC
40	MIC1P			Analog	I		Micro 1 Input Positive	NC
41	SPK2N			Analog	O		Speaker 2 Output Negative	NC
42	A1			VCC_1V8	O		Address bus 1	NC
43	GPIO0	32kHz		VCC_2V8	I/O	32 kHz		NC
44	SCL1	GPIO26		Open Drain	O	Z	I²C Clock	NC
45	GPIO19			VCC_2V8	I/O	Z		NC
46	SDA1	GPIO27		Open Drain	I/O	Z	I²C Data	NC
47	GPIO21			VCC_2V8	I/O	Undefined		NC
48	GPIO20			VCC_2V8	I/O	Undefined		NC
49	INT1	GPIO25		VCC_2V8	I	Z	Interruption 1 Input	If INT1 is not used, it should be configured as GPIO
50	INT0	GPIO3		VCC_1V8	I	Z	Interruption 0 Input	If INT0 is not used, it should be configured as GPIO
51	GPIO1	**		VCC_1V8	I/O	Undefined		NC
52	VPAD-USB			VPAD-USB	I		USB Power supply input	NC
53	GPIO2	**		VCC_1V8	I/O	Undefined		NC
54	USB-DP			VPAD-USB	I/O		USB Data	NC
55	GPIO23	**		VCC_2V8	I/O	Z		NC
56	USB-DM			VPAD-USB	I/O		USB Data	NC

Pin #	Signal Name		I/O Type	Voltage	I/O*	Reset State	Description	Dealing with Unused Pins
	Nominal	Mux						
57	GPIO22	**		VCC_2V8	I/O	Z		NC
58	GPIO24			VCC_2V8	I/O	Z		NC
59	COL0	GPIO4		VCC_1V8	I/O	Pull-up	Keypad column 0	NC
60	COL1	GPIO5		VCC_1V8	I/O	Pull-up	Keypad column 1	NC
61	COL2	GPIO6		VCC_1V8	I/O	Pull-up	Keypad column 2	NC
62	COL3	GPIO7		VCC_1V8	I/O	Pull-up	Keypad column 3	NC
63	COL4	GPIO8		VCC_1V8	I/O	Pull-up	Keypad column 4	NC
64	ROW4	GPIO13		VCC_1V8	I/O	0	Keypad Row 4	NC
65	ROW3	GPIO12		VCC_1V8	I/O	0	Keypad Row 3	NC
66	ROW2	GPIO11		VCC_1V8	I/O	0	Keypad Row 2	NC
67	ROW1	GPIO10		VCC_1V8	I/O	0	Keypad Row 1	NC
68	ROW0	GPIO9		VCC_1V8	I/O	0	Keypad Row 0	NC
69	~CT125-RI	GPIO42		VCC_2V8	O	Undefined	Main RS232 Ring Indicator	NC
70	~CT109-DCD1	GPIO43		VCC_2V8	O	Undefined	Main RS232 Data Carrier Detect	NC
71	CT103-TXD1	GPIO36		VCC_2V8	I	Z	Main RS232 Transmit	Pull-up to VCC_2V8 with 100kΩ and add a test point for firmware update if the pin or UART1 is not used. Refer to section 4.7 Main Serial Link (UART1) for application examples.
72	~CT105-RTS1	GPIO38		VCC_2V8	I	Z	Main RS232 Request To Send	Pull-up to VCC_2V8 with 100kΩ and add a test point for firmware update if the pin or UART1 is not used. Refer to section 4.7.6 2-wire Serial Interface for dealing with this pin when using a 2-wire UART.
73	CT104-RXD1	GPIO37 / INT2		VCC_2V8	O	1	Main RS232 Receive	Add a test point for firmware update if the pin or UART1 is not used. Refer to section 4.7 Main Serial Link (UART1) for application examples.

Pin #	Signal Name		I/O Type	Voltage	I/O*	Reset State	Description	Dealing with Unused Pins
	Nominal	Mux						
74	~CT107-DSR1	GPIO40		VCC_2V8	O	Z	Main RS232 Data Set Ready	NC
75	~CT106-CTS1	GPIO39		VCC_2V8	O	Z	Main RS232 Clear To Send	Add a test point for firmware update if the pin or UART1 is not used. Refer to section 4.7 Main Serial Link (UART1) for application examples.
76	~CT108-2-DTR1	GPIO41 / INT3		VCC_2V8	I	Z	Main RS232 Data Terminal Ready	Pull-up to VCC_2V8 with 100kΩ if the pin or UART1 is not used. Refer to section 4.7.5 4-wire Serial Interface for dealing with this pin when using a 4-wire UART; or to section 4.7.6 2-wire Serial Interface when using a 2-wire UART.
77	PCM-SYNC			VCC_1V8	O	Pull-down	PCM Frame Synchronization	NC
78	PCM-IN			VCC_1V8	I	Pull-up	PCM Data Input	NC
79	PCM-CLK			VCC_1V8	O	Pull-down	PCM Clock	NC
80	PCM-OUT			VCC_1V8	O	Pull-up	PCM Data Output	NC
81	/OE-R/W			VCC_1V8	O		Output Enable/ Read not write	NC
82	DAC0			Analog	O		Digital to Analog Output	NC
83	/CS3			VCC_1V8	O		Chip Select 3	NC
84	/WE-E			VCC_1V8	O		Write Enable	NC
85	D0			VCC_1V8	I/O		Data for Peripheral	NC
86	D15			VCC_1V8	I/O		Data for Peripheral	NC
87	D1			VCC_1V8	I/O		Data for Peripheral	NC
88	D14			VCC_1V8	I/O		Data for Peripheral	NC
89	D2			VCC_1V8	I/O		Data for Peripheral	NC
90	D13			VCC_1V8	I/O		Data for Peripheral	NC

Pin #	Signal Name		I/O Type	Voltage	I/O*	Reset State	Description	Dealing with Unused Pins
	Nominal	Mux						
91	D3			VCC_1V8	I/O		Data for Peripheral	NC
92	D12			VCC_1V8	I/O		Data for Peripheral	NC
93	D4			VCC_1V8	I/O		Data for Peripheral	NC
94	D11			VCC_1V8	I/O		Data for Peripheral	NC
95	D5			VCC_1V8	I/O		Data for Peripheral	NC
96	D10			VCC_1V8	I/O		Data for Peripheral	NC
97	D6			VCC_1V8	I/O		Data for Peripheral	NC
98	D9			VCC_1V8	I/O		Data for Peripheral	NC
99	D7			VCC_1V8	I/O		Data for Peripheral	NC
100	D8			VCC_1V8	I/O		Data for Peripheral	NC

* The I/O direction information is only for the nominal signal. When the signal is configured in GPIO, it can always be an Input or an Output.

** For more information about multiplexing these signals, refer to section 4.3 General Purpose Input/Output.

Refer to section 4.2 Electrical Information for Digital I/O for open drain, 2V8 and 1V8 voltage characteristics and reset state definitions.

4.1.2. Pin Out Differences

Although the Q26 Series Embedded Modules are compatible, one must be careful with regards to their specific signal differences. The following table enumerates the pin out differences between the Q2686, Q2687 and the Q2687 Refreshed embedded modules.

Table 8. Signal Comparison between the Q26 Series Intelligent Embedded Modules

Pin #	Q2686			Q2687			Q2687 Refreshed		
	Signal Name	**Function**	**Value**	**Signal Name**	**Function**	**Value**	**Signal Name**	**Function**	**Value**
42	Reserved	Not in Use	-	A1	Address Bus	1V8	A1	Address Bus	1V8
51	GPIO1	General Purpose IO	1V8	CS2 / A25 / GPIO1	Chip Select, Address bus, General Purpose IO	1V8	CS2 / A25 / GPIO1	Chip Select, Address bus, General Purpose IO	1V8
53	GPIO2	General Purpose IO	1V8	A24 / GPIO2	Address bus, General Purpose IO	1V8	A24 / GPIO2	Address bus, General Purpose IO	1V8
83	NC-3	Not Connected	-	/CS3	Chip Select 3	1V8	/CS3	Chip Select 3	1V8
81, 84 – 100	NC	Not Connected	-	Parallel Interface	Parallel Bus Interface	1V8	Parallel Interface	Parallel Bus Interface	1V8

4.2. Electrical Information for Digital I/O

There are three types of digital I/Os on the Q2687 Refreshed Embedded Module:

- 2.8 volt CMOS
- 1.8 volt CMOS
- Open drain

Refer to the tables below for the electrical characteristics of these three digital I/Os.

Table 9. Electrical Characteristic of a 2.8 Volt Type (2V8) Digital I/O

Parameter		I/O Type	Minimum	Typical	Maximum	Condition
Internal 2.8V power supply		VCC_2V8	2.74V	2.8V	2.86V	
Input / Output Pin	V_{IL}	CMOS	-0.5V*		0.84V	
	V_{IH}	CMOS	1.96V		3.2V*	
	V_{OL}	CMOS			0.4V	I_{OL} = - 4 mA
	V_{OH}	CMOS	2.4V			I_{OH} = 4 mA
	I_{OH}				4mA	
	I_{OL}				- 4mA	

* Absolute maximum ratings

All 2.8V I/O pins do not accept input signal voltages above the maximum voltage specified above; except for the UART1 interface, which is 3.3V tolerant.

Table 10. Electrical Characteristic of a 1.8 Volt Type (1V8) Digital I/O

Parameter		I/O Type	Minimum	Typical	Maximum	Condition
Internal 1.8V power supply (for non-ESIM modules)		VCC_1V8	1.76V	1.8V	1.94V	
Internal 1.8V power supply (for the Q26SM703RD)		VCC_1V8	1.76V	1.92V	1.97V	
Input / Output Pin	V_{IL}	CMOS	-0.5V*		0.54V	
	V_{IH}	CMOS	1.33V		2.2V*	
	V_{OL}	CMOS			0.4V	I_{OL} = - 4 mA
	V_{OH}	CMOS	1.4V			I_{OH} = 4 mA
	I_{OH}				4mA	
	I_{OL}				- 4mA	

* Absolute maximum ratings

Table 11. Open Drain Output Type

Signal Name	Parameter	I/O Type	Minimum	Typical	Maximum	Condition
LED0	V_{OL}	Open Drain			0.4V	
	I_{OL}	Open Drain			8mA	

Signal Name	Parameter	I/O Type	Minimum	Typical	Maximum	Condition
BUZZER0	V_{OL}	Open Drain			0.4V	
	I_{OL}	Open Drain			100mA	
SDA1 / GPIO27 and SCL1 / GPIO26	V_{TOL}	Open Drain			3.3V	Tolerated voltage
	V_{IH}	Open Drain	2V			
	V_{IL}	Open Drain			0.8V	
	V_{OL}	Open Drain			0.4V	
	I_{OL}	Open Drain			3mA	

The reset states of the I/Os are given in each interface description chapter. Definitions of these states are given in the table below.

Table 12. Reset State Definition

Parameter	Definition
0	Set to GND
1	Set to supply 1V8 or 2V8 depending on I/O type
Pull-down	Internal pull-down with ~60kΩ resistor
Pull-up	Internal pull-up with ~60kΩ resistor to supply 1V8 or 2V8 depending on I/O type
Z	High impedance
Undefined	**Caution:** *Undefined must not be used in an application if a special state is required at reset. These pins may be toggling a signal(s) during reset.*

4.3. General Purpose Input/Output

The Q2687 Refreshed Embedded Module provides up to 44 General Purpose I/O. They are used to control any external device such as a LCD or a Keyboard backlight.

4.3.1. Pin Description

Refer to the following table for the pin description of the general purpose input/output interface.

Table 13. GPIO Pin Description

Signal	Pin Number	I/O	I/O Type	Reset State	Multiplexed With
GPIO0	43	I/O	2V8	Undefined	32kHz***
GPIO1	51	I/O	1V8	Undefined	A25/~CS2*
GPIO2	53	I/O	1V8	Undefined	A24*
GPIO3#	50	I/O	1V8	Z	INT0
GPIO4	59	I/O	1V8	Pull up	COL0
GPIO5	60	I/O	1V8	Pull up	COL1
GPIO6	61	I/O	1V8	Pull up	COL2
GPIO7	62	I/O	1V8	Pull up	COL3

Signal	Pin Number	I/O	I/O Type	Reset State	Multiplexed With
GPIO8	63	I/O	1V8	Pull up	COL4
GPIO9	68	I/O	1V8	0	ROW0
GPIO10	67	I/O	1V8	0	ROW1
GPIO11	66	I/O	1V8	0	ROW2
GPIO12	65	I/O	1V8	0	ROW3
GPIO13	64	I/O	1V8	0	ROW4
GPIO14	31	I/O	1V8	Z	CT103/TXD2
GPIO15	30	I/O	1V8	0	CT104/RXD2 / INT4
GPIO16	32	I/O	1V8	0	~CT106/CTS2
GPIO17	33	I/O	1V8	Z	~CT105/RTS2
GPIO18	12	I/O	1V8	Z	SIMPRES
GPIO19	45	I/O	2V8	Z	Not mux
GPIO20	48	I/O	2V8	Undefined	Not mux
GPIO21	47	I/O	2V8	Undefined	Not mux
GPIO22	57	I/O	2V8	Z	Not mux**
GPIO23	55	I/O	2V8	Z	Not mux**
GPIO24	58	I/O	2V8	Z	Not mux
GPIO25	49	I/O	2V8	Z	INT1
GPIO26	44	I/O	Open drain	Z	SCL1
GPIO27	46	I/O	Open drain	Z	SDA1
GPIO28	23	I/O	2V8	Z	SPI1-CLK
GPIO29	25	I/O	2V8	Z	SPI1-IO
GPIO30	24	I/O	2V8	Z	SPI1-I
GPIO31	22	I/O	2V8	Z	SPI1-Load
GPIO32	26	I/O	2V8	Z	SPI2-CLK
GPIO33	27	I/O	2V8	Z	SPI2-IO
GPIO34	29	I/O	2V8	Z	SPI2-I
GPIO35	28	I/O	2V8	Z	SPI2-Load
GPIO36	71	I/O	2V8	Z	CT103/TXD1
GPIO37	73	I/O	2V8	1	CT104/RXD1 / INT2
GPIO38	72	I/O	2V8	Z	~CT105/RTS1
GPIO39	75	I/O	2V8	Z	~CT106/CTS1
GPIO40	74	I/O	2V8	Z	~CT107/DSR1
GPIO41	76	I/O	2V8	Z	~CT108-2/DTR1 / INT3
GPIO42	69	I/O	2V8	Undefined	~CT125/RI1
GPIO43	70	I/O	2V8	Undefined	~CT109/DCD1

* If the parallel bus is used, these pins will be mandatory for the parallel bus functionality. Refer to section 4.5 Parallel Interface.

** If a Bluetooth module is used with the Q2687 Refreshed Embedded Module, this GPIO must be reserved.

*** With Open AT Application Framework 2. For more details, refer to document [2] Firmware 7.43 AT Commands Manual.

GPIO3 is the associated GPIO used with **AT+WTBI** to monitor TDM bursts. For more information about this AT command, refer to document [2] Firmware 7.43 AT Commands Manual.

Refer to section 4.2 Electrical Information for Digital I/O for open drain, 2V8 and 1V8 voltage characteristics and reset state definitions.

4.4. Serial Interface

The Q2687 Refreshed Embedded Module may be connected to an LCD module driver through either the two SPI buses (3 or 4-wire interface) or through the I^2C bus (2-wire interface).

4.4.1. SPI Bus

Both SPI bus interfaces include:

- A CLK signal (SPIx-CLK)
- An I/O signal (SPIx-IO)
- An I signal (SPIx-I)
- A CS (Chip Select) signal complying with the standard SPI bus (any GPIO) (~SPIx-CS)
- An optional Load signal (only the SPIx-LOAD signal)

4.4.1.1. Characteristics

The following lists the features available on the SPI bus.

- Master mode operation
- The CS signal must be any GPIO
- The LOAD signal (optional) is used for word handling mode (only the SPIx-LOAD signal)
- SPI speed is from 102Kbit/s to 13Mbit/s in master mode operation
- 3 or 4-wire interface (5-wire interface is possible with the optional SPIx-LOAD signal)
- SPI-mode configuration: 0 to 3 (for more details, refer to document [2] Firmware 7.43 AT Commands Manual)
- 1 to 16 bits data length

4.4.1.2. SPI Configuration

Table 14. SPI Bus Configuration

Operation	Maximum Speed	SPI-Mode	Duplex	3-wire Type	4-wire Type	5-wire Type
Master	13 Mb/s	0,1,2,3	Half	SPIx-CLK; SPIx-IO; GPIOx as CS	SPIx-CLK; SPIx-IO; SPIx-I; GPIOx as CS	SPIx-CLK; SPIx-IO; SPIx-I; GPIOx as CS; SPIx-LOAD (not muxed in GPIO)

Refer to section 4.4.1.6 Application for more information on the signals used and their corresponding configurations.

4.4.1.3. SPI Waveforms

The figure below shows the waveforms for SPI transfers with a 4-wire configuration in master mode 0.

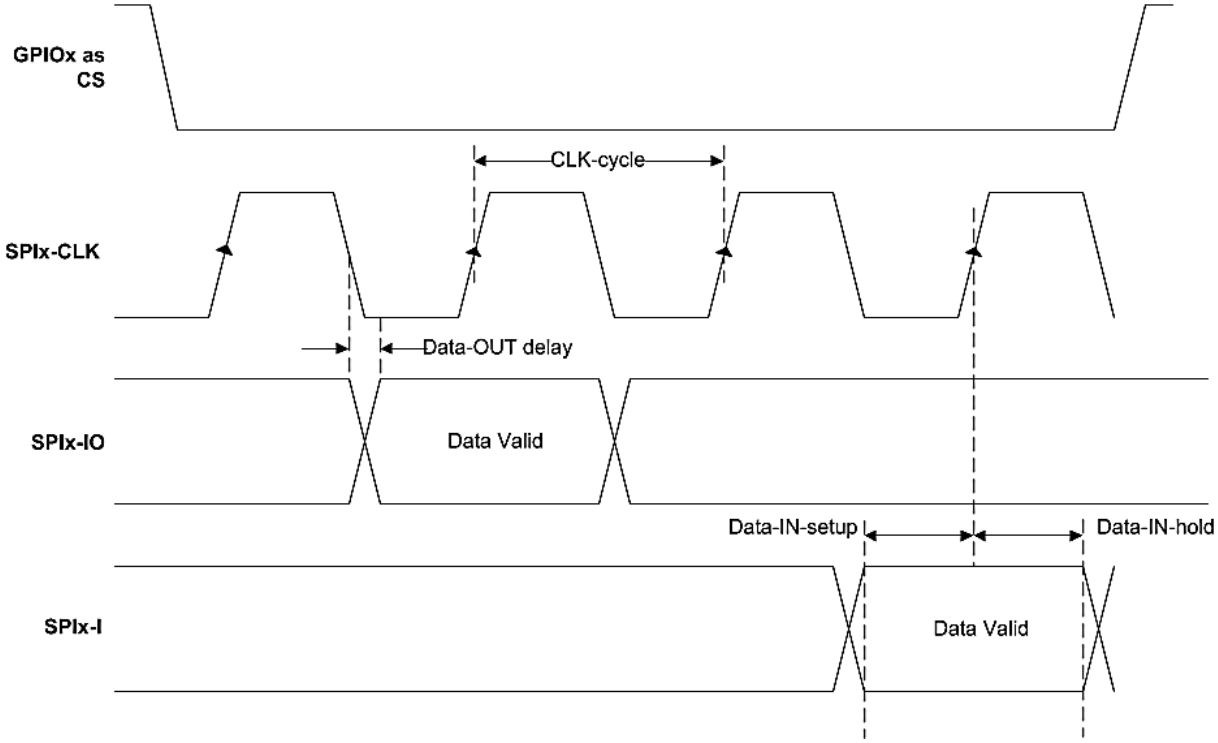


Figure 7. SPI Timing Diagram (Mode 0, Master, 4 wires)

Table 15. SPI Bus AC Characteristics

Signal	Description	Minimum	Typical	Maximum	Unit
CLK-cycle	SPI clock frequency	0.102		13	MHz
Data-OUT delay	Data out ready delay time			10	ns
Data-IN-setup	Data in setup time	2			ns
Data-OUT-hold	Data out hold time	2			ns

The following figure shows the waveform for SPI transfer with the LOAD signal configuration in master mode 0 (chip select is not represented).

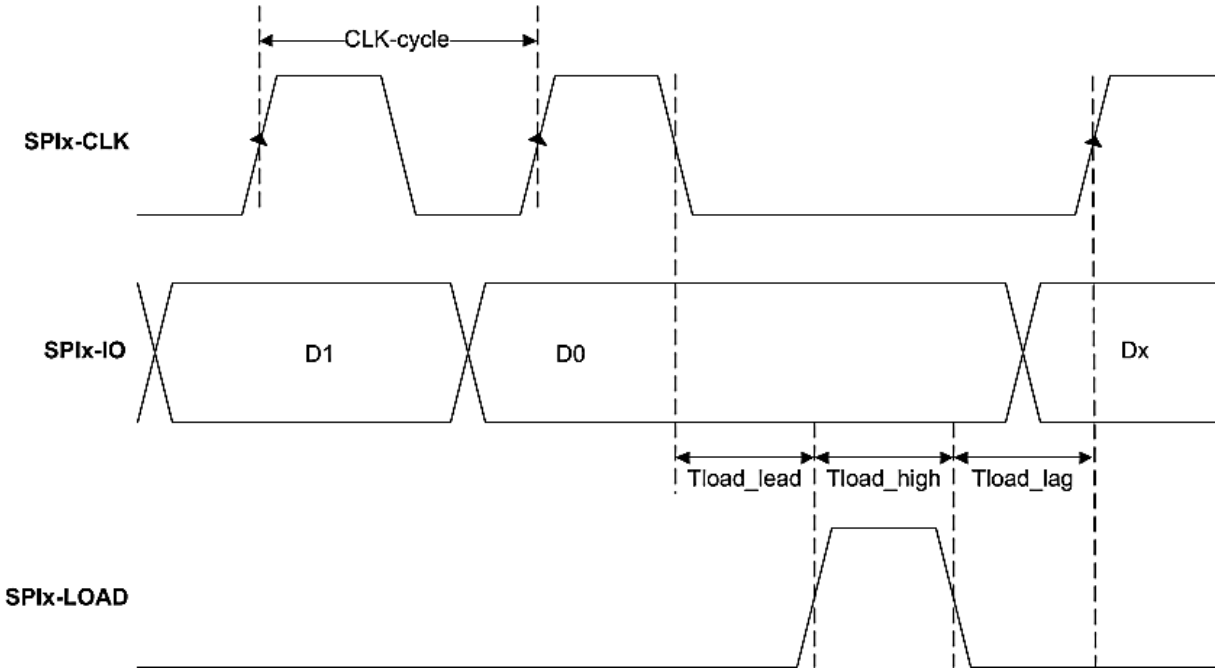


Figure 8. SPI Timing Diagram with LOAD Signal (Mode 0, Master, 4 wires)

4.4.1.4. SPI1 Pin Description

Refer to the following table for the SPI1 pin description.

Table 16. SPI1 Pin Description

Pin Number	Signal	I/O	I/O Type	Reset State	Description	Multiplexed With
22	SPI1-LOAD	O	2V8	Z	SPI load	GPIO31
23	SPI1-CLK	O	2V8	Z	SPI Serial Clock	GPIO28
24	SPI1-I	I	2V8	Z	SPI Serial input	GPIO30
25	SPI1-IO	I/O	2V8	Z	SPI Serial input/output	GPIO29

Refer to section 4.2 Electrical Information for Digital I/O for open drain, 2V8 and 1V8 voltage characteristics and reset state definitions.

4.4.1.5. SPI2 Pin Description

Refer to the following table for the SPI2 pin description.

Table 17. SPI2 Pin Description

Pin Number	Signal	I/O	I/O Type	Reset State	Description	Multiplexed With
26	SPI2-CLK	O	2V8	Z	SPI Serial Clock	GPIO32
27	SPI2-IO	I/O	2V8	Z	SPI Serial input/output	GPIO33
28	SPI2-LOAD	O	2V8	Z	SPI load	GPIO35
29	SPI2-I	I	2V8	Z	SPI Serial input	GPIO34

Refer to section 4.2 Electrical Information for Digital I/O for open drain, 2V8 and 1V8 voltage characteristics and reset state definitions.

4.4.1.6. Application

4.4.1.6.1. 3-wire Application

For the 3-wire configuration, only the SPIx-I/O is used as both input and output.

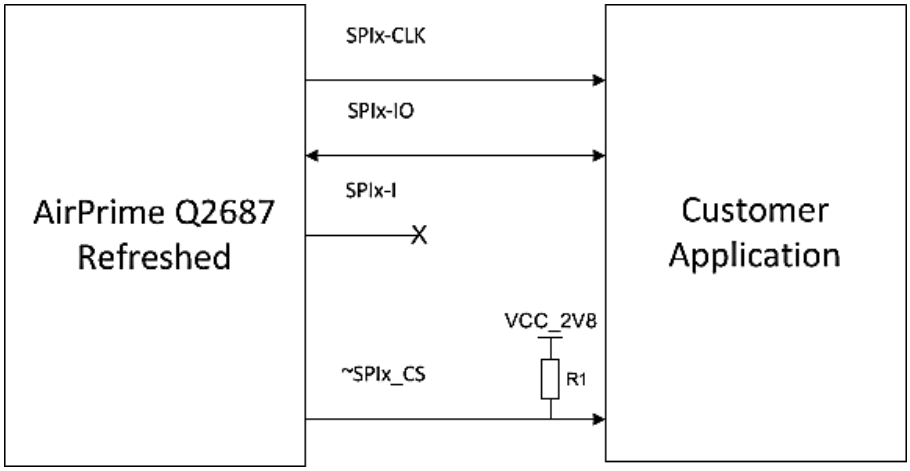


Figure 9. Example of a 3-wire SPI Bus Application

The SPIx-I line is not used in a 3-wire configuration. Instead, this can be left open or used as a GPIO for other application functionality.

One pull-up resistor, R1, is needed to set the SPIx-CS level during the reset state. Except for R1, no other external component is needed is the electrical specifications of the customer application comply with the Q2687 Refreshed embedded module interface electrical specifications.

Note that the value of R1 depends on the peripheral plugged to the SPIx interface.

4.4.1.6.2. 4-wire Application

For the 4-wire configuration, the input and output data lines are dissociated. SPIx-I/O is used as output only and SPIx-I is used as input only.

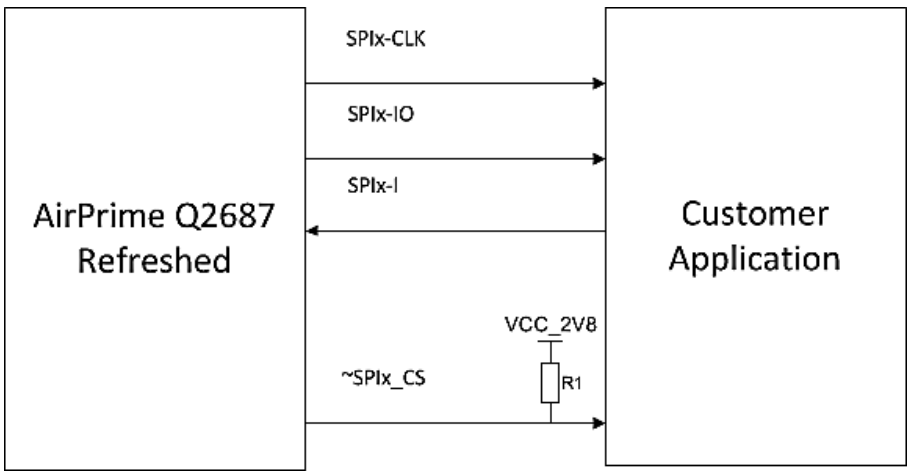


Figure 10. Example of a 4-wire SPI Bus Application

One pull-up resistor, R1, is needed to set the SPIx-CS level during the reset state. Except for R1, no other external component is needed if the electrical specifications of the customer application comply with the Q2687 Refreshed embedded module SPIx interface electrical specifications.

4.4.1.6.3. 5-wire Application

For the 5-wire configuration, SPIx-I/O is used as output only and SPIx-I is used as input only. The dedicated SPIx-LOAD signal is also used. This is an additional signal in more than a Chip Select (any other GPIOx).

4.4.2. I²C Bus

The I²C Bus interface includes a CLK signal (SCL1) and a data signal (SDA1) complying with a 100kbit/s-standard interface (standard mode: s-mode).

The I²C bus is always in master mode operation.

The maximum speed transfer is 400Kbit/s (fast mode: f-mode).

For more information on the I²C bus, see document [12] “I2C Bus Specification”, Version 2.0, Philips Semiconductor 1998.

4.4.2.1. I²C Waveforms

The figure below shows the I²C bus waveform in master mode configuration.

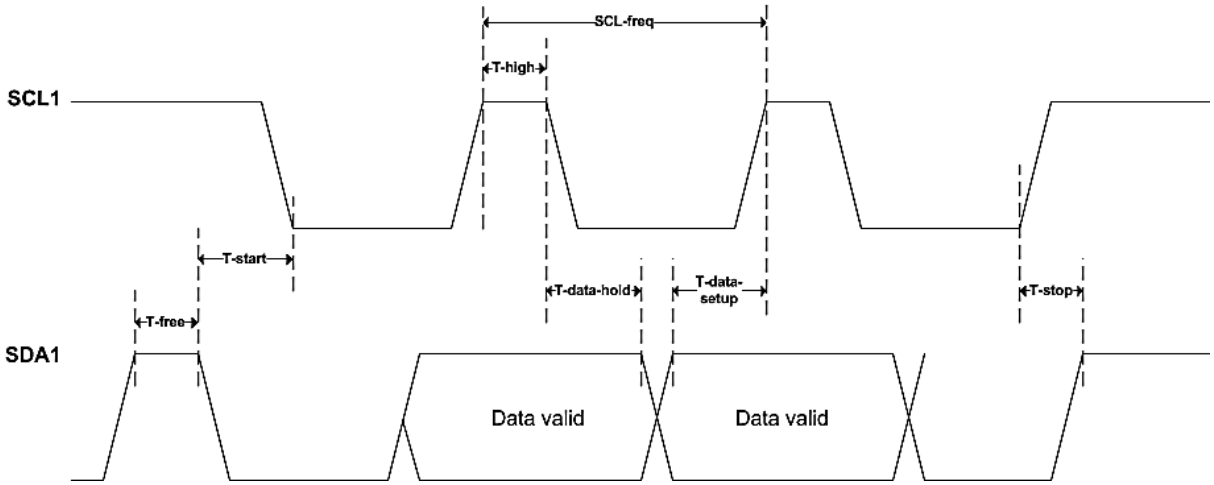


Figure 11. I²C Timing Diagram (master)

Table 18. I²C AC Characteristics

Signal	Description	Minimum	Typical	Maximum	Unit
SCL1-freq	I²C clock frequency	100		400	kHz
T-start	Hold time START condition	0.6			µs
T-stop	Setup time STOP condition	0.6			µs
T-free	Bus free time, STOP to START	1.3			µs
T-high	High period for clock	0.6			µs
T-data-hold	Data hold time	0		0.9	µs

Signal	Description	Minimum	Typical	Maximum	Unit
T-data-setup	Data setup time	100			ns

4.4.2.2. I²C Pin Description

Refer to the following table for the I²C pin description.

Table 19. I²C Pin Description

Pin Number	Signal	I/O	I/O Type	Reset State	Description	Multiplexed With
44	SCL1	O	Open drain	Z	Serial Clock	GPIO26
46	SDA1	I/O	Open drain	Z	Serial Data	GPIO27

Refer to section 4.2 Electrical Information for Digital I/O for open drain, 2V8 and 1V8 voltage characteristics and reset state definitions.

4.4.2.3. Application

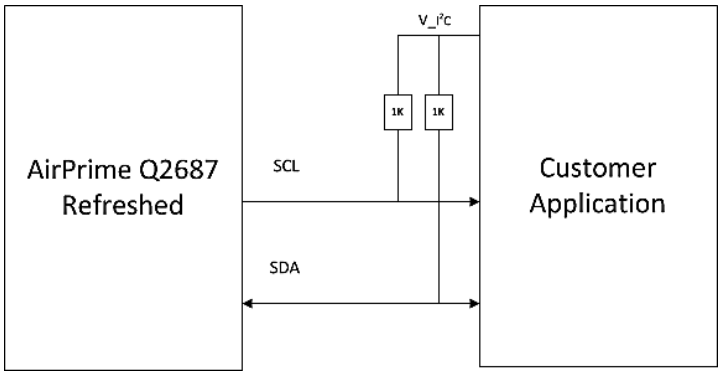


Figure 12. Example1 of an I²C Bus Application

The two lines, SCL1 and SDA1, both need to be pulled-up to the VI²C voltage. Although the VI²C voltage is dependent on the customer application component connected to the I²C bus, it must comply with the Q2687 Refreshed embedded module electrical specifications.

The VCC_2V8 (pin 10) of the Q2687 Refreshed embedded module can be used to connect the pull-up resistors if the I²C bus voltage is 2.8V.

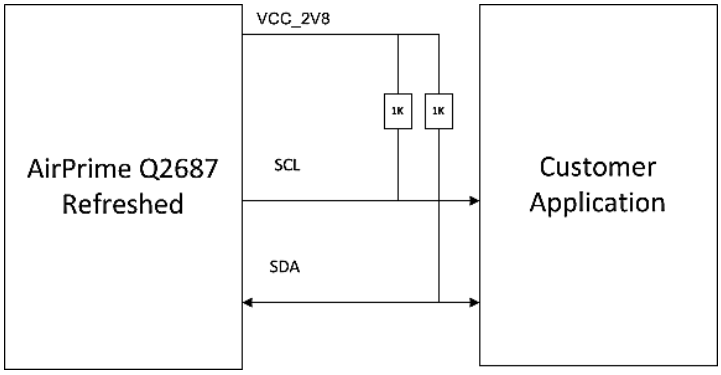


Figure 13. Example2 of an I²C Bus Application

The I^2C bus complies with both the standard mode (baud rate = 100Kbit/s) and the fast mode (baud rate = 400Kbit/s). The value of the pull up resistors varies depending on the mode used. When using Fast mode, it is recommended to use 1KΩ resistors to ensure compliance with the I^2C specifications. When using Standard mode, a higher resistance value can be used to save power consumption.

4.5. Parallel Interface

The Q2687 Refreshed Intelligent Embedded Module may be connected to a NAND memory through the 16-bit 1.8V parallel bus interface. The VCC_1V8 (pin 5) of the Q2687 Refreshed embedded module can be used to supply the power to this interface.

The following lists the features available on the parallel interface.

- Up to 128MB address range per chip select ($\overline{CS}$ and $\overline{CS3}$)
- Support for 8, 16, and 32 bit (multiplexed synchronous mode) devices
- Byte enabled signals for 16 bit and 32 bit operations
- Fully programmable timings based on AHB (a division of the ARM clock at 26 MHz) cycles (except for synchronous mode which is based on CLKBURST cycles at 26 MHz only):
  - individually selectable timings for read and write
  - 0 to 7 clock cycles for setup
  - 1 to 32 clock cycles for access cycle
  - 1 to 8 clock cycles for page access cycle
  - 0 to 7 clock cycles for hold
  - 1 to 15 clock cycles for turnaround
- Page mode Flash memory support
  - page size of 4, 8, 16 or 32
- Burst mode Flash memory support up to AHB (26 MHz) clock frequency (for devices sensitive to rising edge of the clock only)
  - AHB, AHB/2, AHB/4 or AHB/8 burst clock output
  - burst size of 4, 8, 16, 32
  - automatic CLKBURST power-down between accesses
- Intel mode ($\overline{WE}$ and $\overline{\mathrm{OE}}$) and Motorola mode (E and $R/\overline{W}$) control signals
- Synchronous write mode
- Synchronous multiplexed data/address mode (x32 mode)
- Adaptation to word, half word, and byte accesses to the external devices

4.5.1. Pin Description

Refer to the following table for the pin description of the Parallel Interface.

Table 20. Parallel Interface Pin Description

Pin Number	Signal	I/O	I/O Type	Reset State	Description	Multiplexed With
42	A1	O	1V8	1	This signal has 2 functions: external Address or byte enable 2 for 16 or 32 bits devices. Another name is used: A1_BE2	Not mux
51	/CS2	I/O	1V8	Undefined	User Chip Select 2	A25/GPIO1

Pin Number	Signal	I/O	I/O Type	Reset State	Description	Multiplexed With
53	A24	I/O	1V8	Undefined	Address line for external device/Command selection	GPIO2
81	/OE-R/W	O	1V8	1	Output enable signal (Intel mode); read not write signal (Motorola mode)	Not mux
83	/CS3	O	1V8	1	User Chip select 3	Not mux
84	/WE-E	O	1V8	1	Write enable Signal (Intel mode) enable signal (Motorola mode)	Not mux
85	D0	I/O	1V8	Pull down	Bidirectional data and address line	Not mux
86	D15	I/O	1V8	Pull down	Bidirectional data and address line	Not mux
87	D1	I/O	1V8	Pull down	Bidirectional data and address line	Not mux
88	D14	I/O	1V8	Pull down	Bidirectional data and address line	Not mux
89	D2	I/O	1V8	Pull down	Bidirectional data and address line	Not mux
90	D13	I/O	1V8	Pull down	Bidirectional data and address line	Not mux
91	D3	I/O	1V8	Pull down	Bidirectional data and address line	Not mux
92	D12	I/O	1V8	Pull down	Bidirectional data and address line	Not mux
93	D4	I/O	1V8	Pull down	Bidirectional data and address line	Not mux
94	D11	I/O	1V8	Pull down	Bidirectional data and address line	Not mux
95	D5	I/O	1V8	Pull down	Bidirectional data and address line	Not mux
96	D10	I/O	1V8	Pull down	Bidirectional data and address line	Not mux
97	D6	I/O	1V8	Pull down	Bidirectional data and address line	Not mux
98	D9	I/O	1V8	Pull down	Bidirectional data and address line	Not mux
99	D7	I/O	1V8	Pull down	Bidirectional data and address line	Not mux
100	D8	I/O	1V8	Pull down	Bidirectional data and address line	Not mux

Refer to section 4.2 Electrical Information for Digital I/O for open drain, 2V8 and 1V8 voltage characteristics and reset state definitions.

4.5.2. Electrical Characteristics

4.5.3. Asynchronous Access

For all timing diagrams in the following section, the notations hereafter are used:

- ADR is used for address bus A24, A1 or D[15:0] when used as address lines
- DATA is used for D[15:0] when used as DATA lines
- $\overline{CS}$ is used for $\overline{CS2}$ or $\overline{CS3}$
- $\overline{BE}$ is used for A1_ $\overline{BE2}$ (Double function on A1 pin)
- $\overline{\mathrm{OE}}$ and R/$\overline{W}$ are used for $\overline{OE}$ _ $R/\overline{W}$
- $\overline{WE}$ and E are used for $\overline{WE}$ _E
- $\overline{ADV}$ signal (not available on 100-pin connector) is the address valid signal

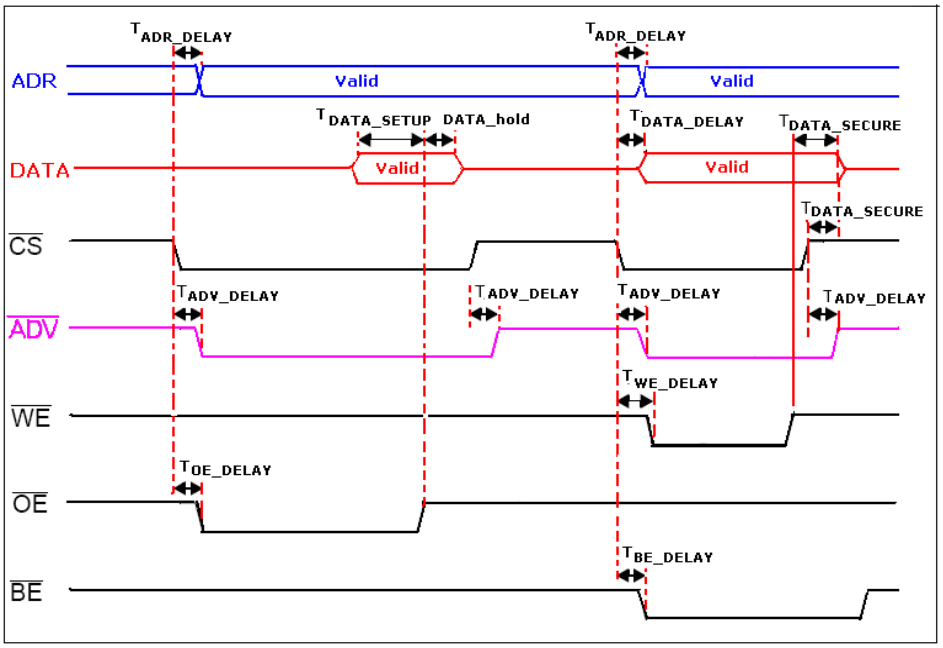


Figure 14. Asynchronous Access

The $\overline{ADV}$ signal is mentioned here because synchronous mode devices may require the signal to be asserted when an asynchronous access is performed.

Refer to the table below for the AC characteristics of asynchronous accesses.

Table 21. AC Characteristics of Asynchronous Accesses

Signal	Description	Minimum	Typical	Maximum	Unit
T_{ADR_DELAY}	ADR delay time from $\overline{CS}$ active			3	ns
T_{DATA_SETUP}	DATA to $\overline{OE}$ setup time	18			ns
T_{DATA_HOLD}	DATA hold time after $\overline{OE}$ inactive	3		4	ns
T_{DATA_DELAY}	DATA delay time from $\overline{CS}$ active			5	ns
T_{DATA_SECURE}	DATA hold time after $\overline{WE}$ inactive or $\overline{CS}$ inactive	-5[1]			ns
T_{ADV_DELAY}	ADV delay time from $\overline{CS}$ active and inactive			3	ns
T_{WE_DELAY}	$\overline{WE}$ delay time from $\overline{CS}$ active			3[2]	ns
T_{OE_DELAY}	$\overline{OE}$ delay time from $\overline{CS}$ active			3[2]	ns
T_{BE_DELAY}	$\overline{BE}$ delay time from $\overline{CS}$ active			3	ns

[1] This timing forces to program at least one cycle for asynchronous

[2] These maximum delays also depends on the setting of registers

4.5.4. Synchronous Access

For all timing diagrams in the following section, the notations hereafter are used:

- ADR is used for address bus as A24, A1 or D[15:0] when used as address lines
- DATA is used for D[15:0] when used as data lines
- $\overline{CS}$ is used for $\overline{CS2}$ or $\overline{CS3}$
- $\overline{BE}$ is used for A1_ $\overline{BE2}$ (Double function on A1 pin)
- $\overline{OE}$ and R/$\overline{W}$ are used for $\overline{OE}$ _ $R/\overline{W}$
- $\overline{WE}$ and E are used for $\overline{WE}$ _E
- CLKBURST is the internal clock at 26MHz (not available on connector pin-out)
- $\overline{ADV}$ signal (not available on 100-pin connector) is the address valid signal
- $\overline{BAA}$ signal (not available on 100-pin connector) is the burst address advance for synchronous operations
- $\overline{WAIT}$ signal (not available on 100-pin connector) is the wait signal for synchronous operation

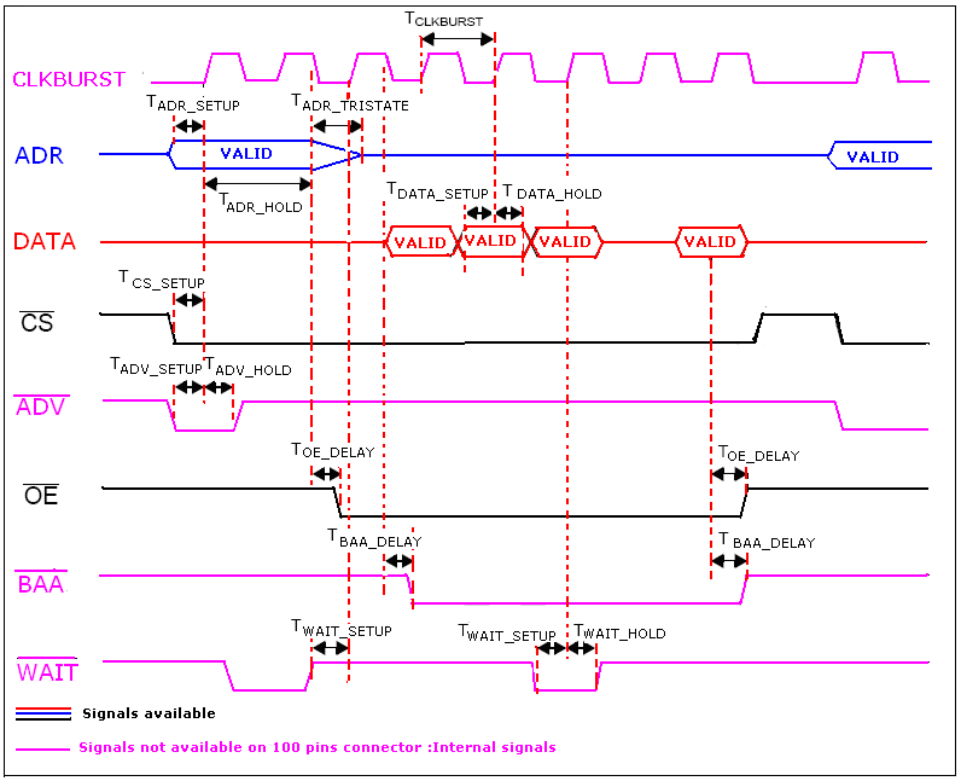


Figure 15. Synchronous Access

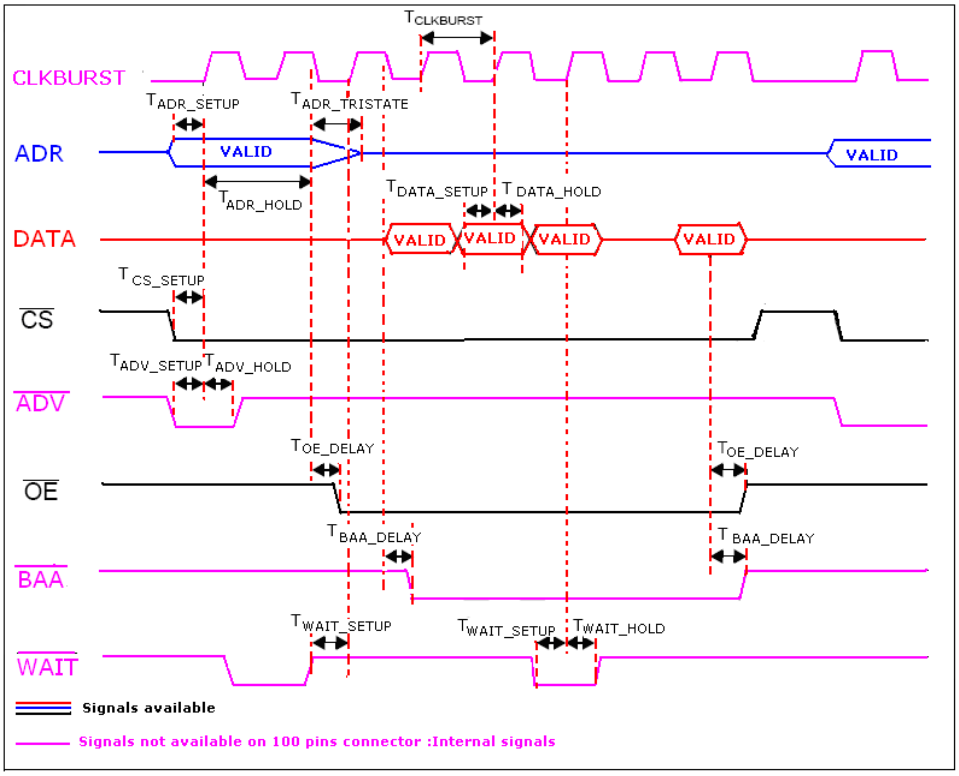


Figure 16. Read Synchronous Timing

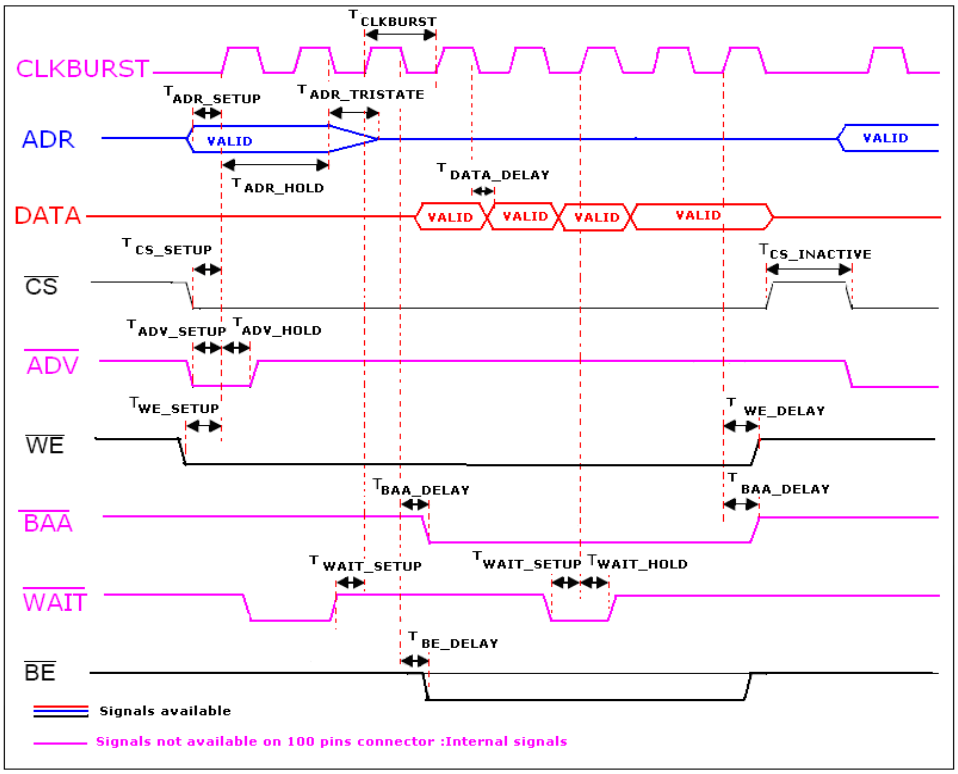


Figure 17. Write Synchronous Timing

Refer to the table below for the AC characteristics of the synchronous accesses.

Table 22. AC Characteristics of Synchronous Accesses

Signal	Description	Minimum	Typical	Maximum	Unit
T_{DATA_DELAY}	CLKBURTS falling edge to DATA valid delay			4	ns
T_{WE_SETUP}	$\overline{WE}$ to CLKBURST setup time	7			ns
T_{BE_DELAY}	CLKBURST falling edge to $\overline{BE}$ delay			4	ns
$T_{CLKBURST}$	CLKBURST clock : period time		38.4		ns
T_{ADR_SETUP}	Address bus setup time	7			ns
T_{ADR_HOLD}	Address bus hold time	19			ns
$T_{ADR\_TRISTATE}$	Address bus tristate time			10	ns
T_{DATA_SETUP}	Data bus setup time	5			ns
T_{DATA_HOLD}	Data bus hold time	3			ns
T_{CS_SETUP}	Chip select setup time	7			ns
T_{ADV_SETUP}	$\overline{ADV}$ setup time	7			ns
T_{ADV_HOLD}	$\overline{ADV}$ hold time	7			ns
T_{OE_DELAY}	Output Enable delay time			13	
T_{BAA_DELAY}	$\overline{BAA}$ delay time			13	ns
T_{WAIT_SETUP}	Wait setup time	5			ns
T_{WAIT_HOLD}	Wait hold time	5			ns

4.5.5. Additional Information Regarding Address Size Bus

The following table establishes the possible configurations depending on address bus size requested on parallel interface.

Table 23. Address Bus Size Details

Address Bus Size	Address Lines	Chip Select Available	Notes
1	A1	/CS2, /CS3	
2	A1, A24	/CS2, /CS3	
3	A1, A24, A25	/CS3	A25 is multiplexed with /CS2

Note that some signals are multiplexed. It is thus possible to have the following configurations:

- CS3*, A1, GPIO1, GPIO2
- CS3*, A1, A24, GPIO1
- CS3*, A1, A24, A25;
- CS3*, CS2*, A1, GPIO2
- CS3*, CS2*, A1, A24

4.5.6. Application

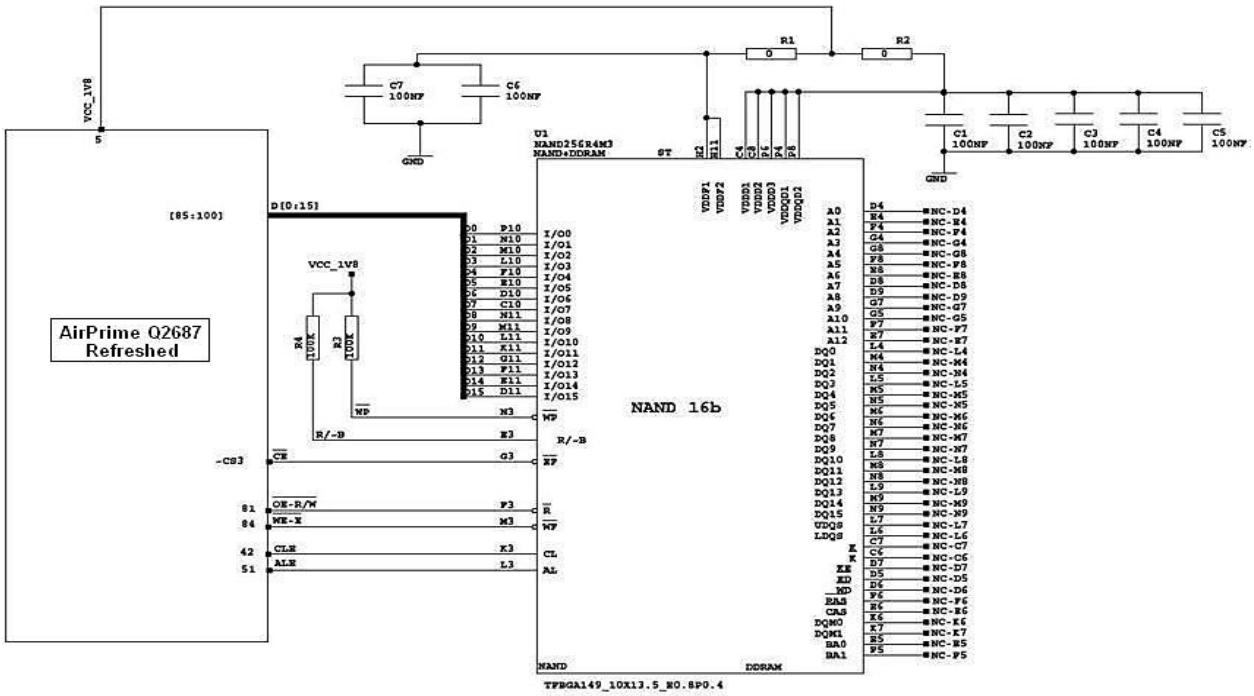


Figure 18. Example of a Parallel Bus Application (NAND Memory)

When interfaced with a NAND memory, VCC_1V8 (pin 5) can be used to supply the power to the NAND.

4.6. Keyboard Interface

This interface provides 10 connections:

- 5 rows (ROW0 to ROW4)

  and

- 5 columns (COL0 to COL4)

Scanning is digital and debouncing is performed in the Q2687 Refreshed Embedded Module. No discreet components like resistors or capacitors are needed when using this interface.

The keyboard scanner is equipped with the following:

- Internal pull-down resistors for the rows
- Pull-up resistors for the columns

Note that current only flows from the column pins to the row pins. This allows transistors to be used in place of the switch for power-on functions.

4.6.1. Pin Description

Refer to the following table for the pin description of the keyboard interface.

Table 24. Keyboard Interface Pin Description

Pin Number	Signal	I/O	I/O Type	Reset State	Description	Multiplexed With
59	COL0	I/O	1V8	Pull-up	Column scan	GPIO4
60	COL1	I/O	1V8	Pull-up	Column scan	GPIO5
61	COL2	I/O	1V8	Pull-up	Column scan	GPIO6
62	COL3	I/O	1V8	Pull-up	Column scan	GPIO7
63	COL4	I/O	1V8	Pull-up	Column scan	GPIO8
64	ROW4	I/O	1V8	0	Row scan	GPIO13
65	ROW3	I/O	1V8	0	Row scan	GPIO12
66	ROW2	I/O	1V8	0	Row scan	GPIO11
67	ROW1	I/O	1V8	0	Row scan	GPIO10
68	ROW0	I/O	1V8	0	Row scan	GPIO9

Refer to section 4.2 Electrical Information for Digital I/O for open drain, 2V8 and 1V8 voltage characteristics and reset state definitions.

With Open AT Application Framework 2, when the keyboard service is used, the set of multiplexed signals becomes unavailable for any other purpose. In the same way, if one or more GPIOs (from the table above) are allocated elsewhere, the keyboard service becomes unavailable.

4.6.2. Application

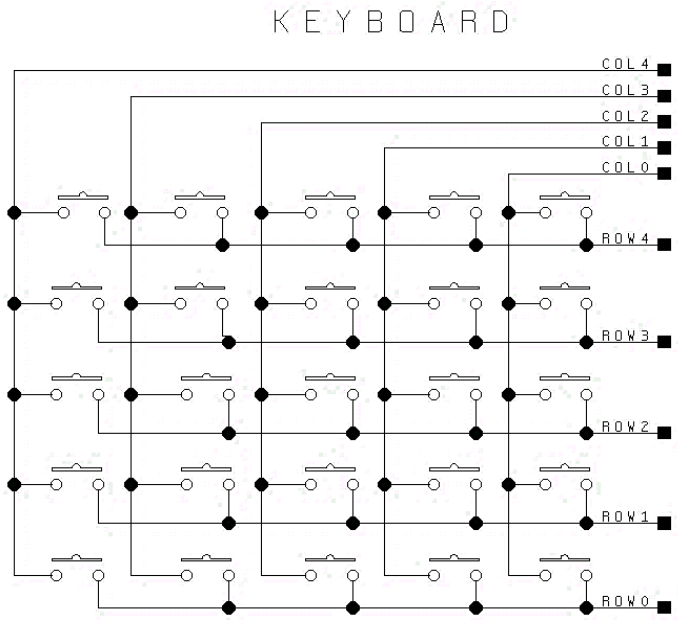


Figure 19. Example of a Keyboard Implementation

4.7. Main Serial Link (UART1)

The main serial link (UART1) is used for communication between the Q2687 Refreshed embedded module and a PC or host processor. It consists of a flexible 8-wire serial interface that complies with V24 protocol signalling, but not with the V28 (electrical interface) due to its 2.8V interface.

To get a V24/V28 (i.e. RS-232) interface, an RS-232 level shifter device is required as described in section 4.7.2 Level Shifter Implementation.

The signals used by UART1 are as follows:

- TX data (CT103-TXD1)
- RX data (CT104-RXD1)
- Request To Send (~CT105-RTS1)
- Clear To Send (~CT106-CTS1)
- Data Terminal Ready (~CT108-2-DTR1)
- Data Set Ready (~CT107-DSR1)
- Data Carrier Detect (~CT109-DCD1)
- Ring Indicator (CT125-RI1)

4.7.1. Pin Description

Refer to the following table for the pin description of the UART1 interface.

Table 25. UART1 Pin Description

Pin Number	Signal*	I/O	I/O Type	Reset State	Description	Multiplexed With
69	~CT125-RI1	O	2V8	Undefined	Ring Indicator	GPIO42
70	~CT109-DCD1	O	2V8	Undefined	Data Carrier Detect	GPIO43
71	CT103-TXD1	I	2V8	Z	Transmit serial data	GPIO36
72	~CT105-RTS1	I	2V8	Z	Request To Send	GPIO38
73	CT104-RXD1	O	2V8	1	Receive serial data	GPIO37 / INT2
74	~CT107-DSR1	O	2V8	Z	Data Set Ready	GPIO40
75	~CT106-CTS1	O	2V8	Z	Clear To Send	GPIO39
76	~CT108-2-DTR1	I	2V8	Z	Data Terminal Ready	GPIO41 / INT3
Shielding leads	CT102/GND		GND		Ground	

* According to PC view

Refer to section 4.2 Electrical Information for Digital I/O for open drain, 2V8 and 1V8 voltage characteristics and reset state definitions.

With Open AT Application Framework 2, when the UART1 service is used, the set of multiplexed signals becomes unavailable for any other purpose. In the same way, if one or more GPIOs (from the table above) are allocated elsewhere, the UART1 service becomes unavailable.

The maximum baud rate of UART1 is **921**kbit/s with Open AT Application Framework 2.33.

The rise and fall times of the reception signals (mainly CT103/TXD1) must be less than 300ns.

The UART1 interface is 2.8V type, but it is 3.3V tolerant.

Tip: *The Q2687 Refreshed embedded module is designed to operate using all the serial interface signals and it is recommended to use ~CT105/RTS1 and ~CT106/CTS1 for hardware flow control in order to avoid data corruption or loss during transmissions.*

4.7.2. Level Shifter Implementation

The level shifter must be a 2.8V with V28 electrical signal compliance.

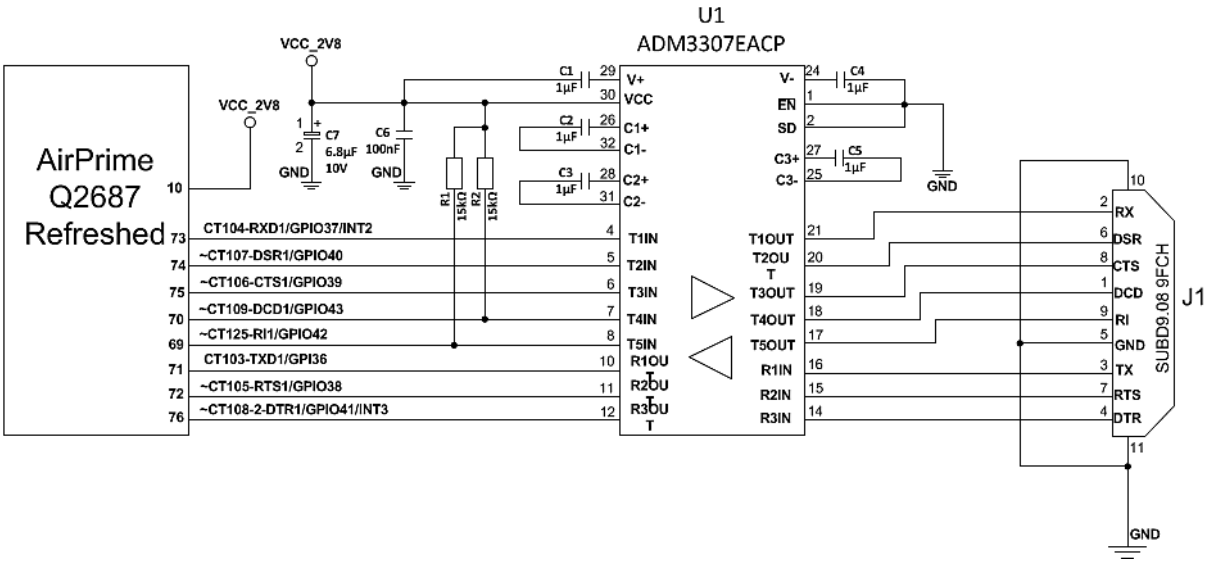


Figure 20. Example of an RS-232 Level Shifter Implementation for UART1

Note: *The U1 chip also protects the Q2687 Refreshed embedded module against ESD at 15KV (air discharge).*

4.7.2.1. Recommended Components

- R1, R2 :15KΩ
- C1, C2, C3, C4, C5 :1µF
- C6 :100nF
- C7 :6.8µF TANTAL 10V CP32136 AVX
- U1 :ADM3307EACP ANALOG DEVICES
- J1 :SUB-D9 female

R1 and R2 are only necessary during the Reset state to force the ~CT1125-RI1 and ~CT109-DCD1 signals to HIGH level.

The ADM3307EACP chip is able to speed up to 921Kb/s. If others level shifters are used, ensure that their speeds are compliant with the UART1 speed.

The ADM3307EACP can be powered by the VCC_2V8 (pin 10) of the Q2687 Refreshed embedded module or by an external regulator at 2.8 V.

If the UART1 interface is connected directly to a host processor, it is not necessary to use level shifters. The interface can be connected as defined in the following sub-section.

4.7.3. V24/CMOS Possible Designs

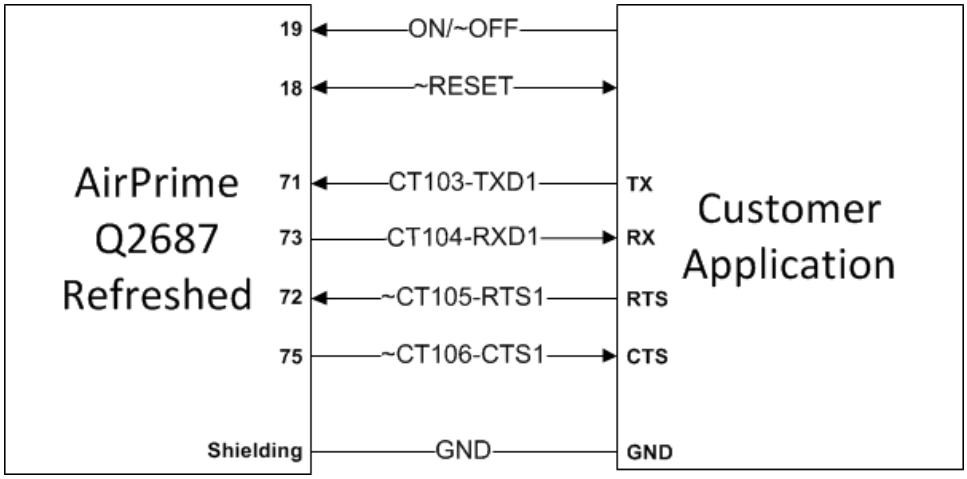


Figure 21. Example of V24/CMOS Serial Link Implementation for UART1

Note that the design presented above is a basic one and that a more flexible design to access the serial link with all modem signals is presented below.

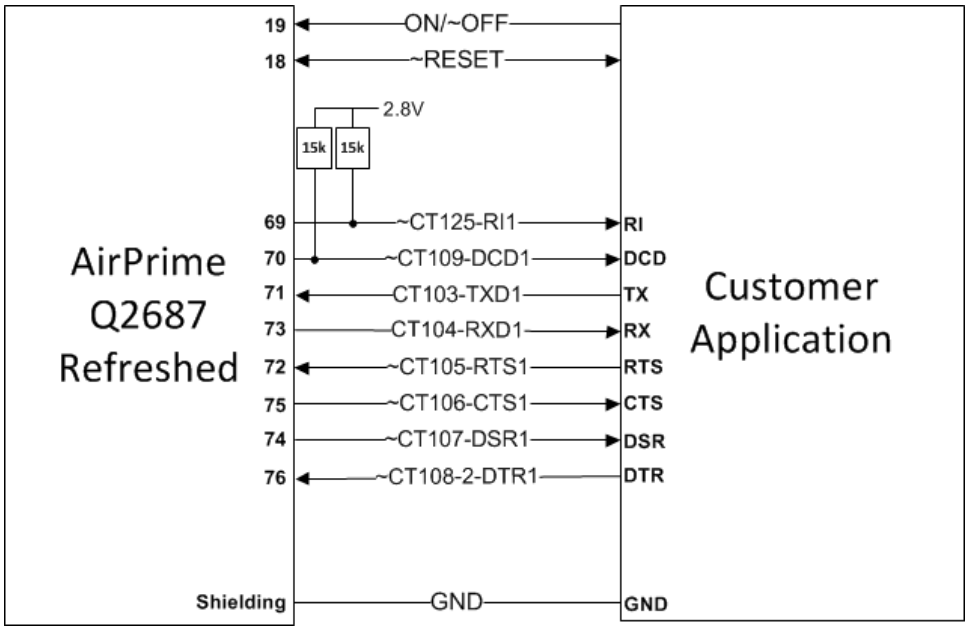


Figure 22. Example of a Full Modem V24/CMOS Serial Link Implementation for UART1

It is recommended to add a 15kΩ pull-up resistor on the ~CT125-RI1 and ~CT109-DCD1 signals to set them to HIGH level during the reset state.

Caution: *In case the Power Down mode (Wavecom 32K mode) is to be activated using Open AT Application Framework, the DTR pin must be wired to a GPIO. Refer to document [2] Firmware 7.43 AT Commands Manual for more information regarding using Open AT Application Framework to activate Wavecom 32K mode.*

4.7.4. 8-wire Serial Interface

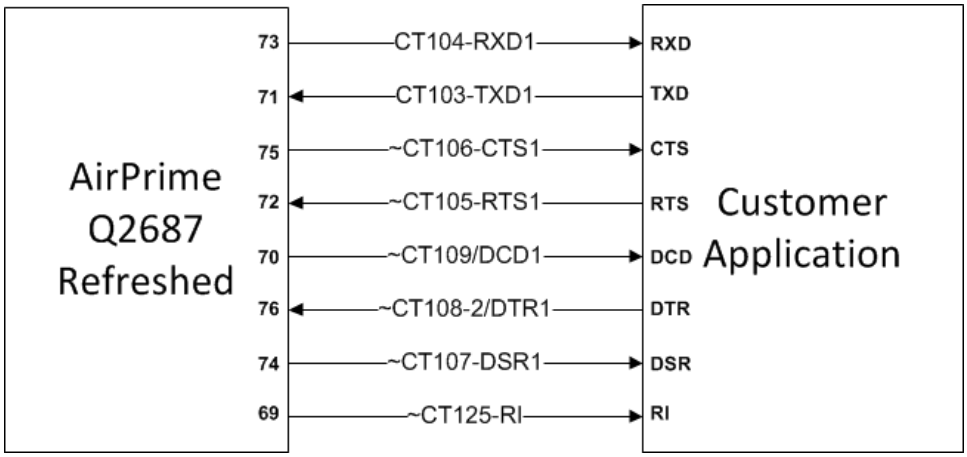


Figure 23. 8-wire Serial Interface Example

4.7.5. 5-wire Serial Interface

The signals used in this interface are as follows:

- CT103-TXD1
- CT104-RXD1
- ~CT105-RTS1
- ~CT106-CTS1
- ~CT108-2-DTR1

The ~CT108-2-DTR1 signal must be managed following the V24 protocol signaling if sleep (or active) idle mode is to be used.

The other signals and their multiplexed GPIOs are not available.

Refer to document [2] Firmware 7.43 AT Commands Manual for more information.

4.7.6. 4-wire Serial Interface

The signals used in this interface are as follows:

- CT103-TXD1
- CT104-RXD1
- ~CT105-RTS1
- ~CT106-CTS1

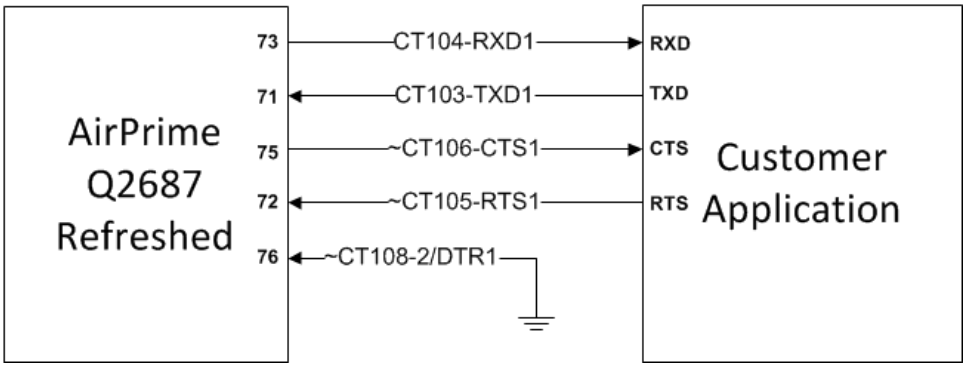


Figure 24. 4-wire Serial Interface Example

The ~CT108-2-DTR1 signal must be pulled down.

The other signals and their multiplexed GPIOs are not available.

Refer to document [2] Firmware 7.43 AT Commands Manual for more information about sleep mode control.

4.7.7. 2-wire Serial Interface

Caution: *Although this case is possible for a connected external chip, it is not recommended (and forbidden for AT command or modem use).*

The flow control mechanism has to be managed from the customer side. The signals used in this interface are as follows:

- CT103-TXD1
- CT104-RXD1

The ~CT108-2-DTR1 and ~CT105-RTS1 signals must be pulled down.

~CT105-RTS1 and ~CT106-CTS1 signals are not used; default hardware flow control on UART1 should be de-activated using AT command **AT+IFC=0,0**. Refer to document [2] Firmware 7.43 AT Commands Manual.

The other signals and their multiplexed GPIOs are not available.

Refer to document [2] Firmware 7.43 AT Commands Manual for more information about sleep mode control.

4.8. Auxiliary Serial Link (UART2)

The auxiliary serial link (UART2) is used for communications between the Q2687 Refreshed embedded module and external devices. It consists of a flexible 4-wire serial interface that complies with V24 protocol signaling, but not with the V28 (electrical interface) due to its 1.8V interface.

To get a V24/V28 (i.e. RS-232) interface, an RS-232 level shifter device is required as described in section 4.8.2 Level Shifter Implementation.

Refer to document [2] Firmware 7.43 AT Commands Manual for more information about the Bluetooth application on the auxiliary serial interface (UART2).

The signals used by UART1 are as follows:

- TX data (CT103-TXD2)
- RX data (CT104-RXD2)
- Request To Send (~CT105-RTS2)
- Clear To Send (~CT106-CTS2)

4.8.1. Pin Description

Refer to the following table for the pin description of the UART2 interface.

Table 26. UART2 Pin Description

Pin Number	Signal*	I/O	I/O Type	Reset State	Description	Multiplexed With
30	CT104-RXD2	O	1V8	0	Receive serial data	GPIO15 / INT4
31	CT103-TXD2	I	1V8	Z	Transmit serial data	GPIO14
32	~CT106-CTS2	O	1V8	0	Clear To Send	GPIO16
33	~CT105-RTS2	I	1V8	Z	Request To Send	GPIO17

* According to PC view

Refer to section 4.2 Electrical Information for Digital I/O for open drain, 2V8 and 1V8 voltage characteristics and reset state definitions.

The maximum baud rate of UART2 is **921**kbit/s with Open AT Application Framework 2.33.

Tip: *The Q2687 Refreshed embedded module is designed to operate using all the serial interface signals and it is recommended to use ~CT105/RTS2 and ~CT106/CTS2 for hardware flow control in order to avoid data corruption during transmissions.*

4.8.2. Level Shifter Implementation

The voltage level shifter must be a 1.8V with V28 electrical signal compliance.

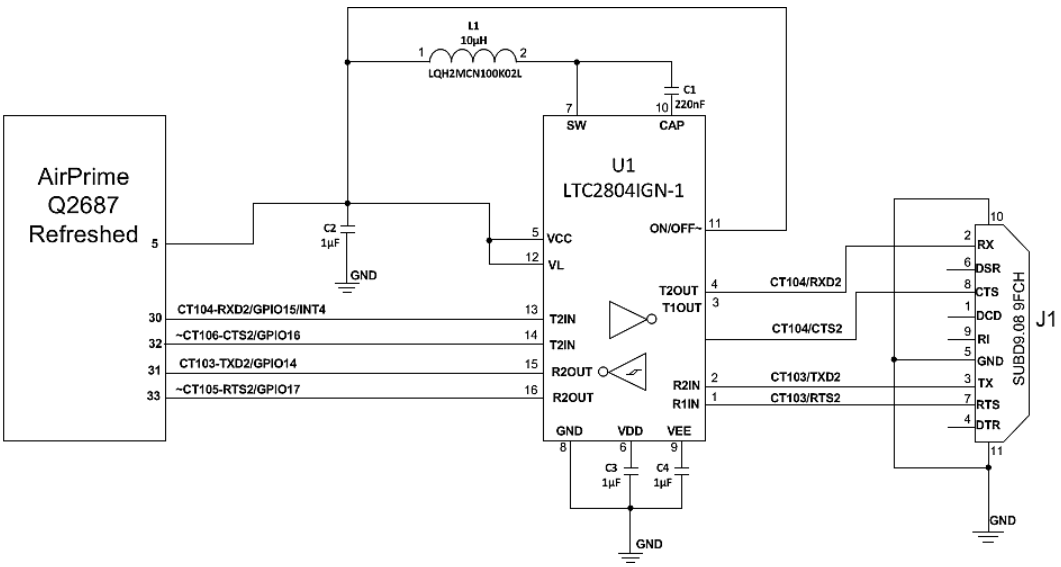


Figure 25. Example of RS-232 Level Shifter Implementation for UART2

4.8.2.1. Recommended Components

- Capacitors
  - C1 :220nF
  - C2, C3, C4 :1µF
- Inductor
  - L1 :10µH
- RS-232 Transceiver
  - U1 :LINEAR TECHNOLOGY LTC® 2804IGN
  - J1 :SUB-D9 female

The LTC2804 can be powered by the VCC_1V8 (pin 5) of the Q2687 Refreshed embedded module or by an external regulator at 1.8 V.

The UART2 interface can be connected directly to others components if the voltage interface is 1.8V.

4.8.3. 4-wire Serial Interface

The signals used in this interface are as follows:

- CT103-TXD2
- CT104-RXD2
- ~CT105-RTS2
- ~CT106-CTS2

The other signals and their multiplexed GPIOs are not available.

Refer to the technical appendixes of document [2] Firmware 7.43 AT Commands Manual for more information.

4.8.4. 2-wire Serial Interface

Caution: *Although this case is possible for a connected external chip, it is not recommended (and forbidden for AT command or modem use).*

The flow control mechanism has to be managed from the customer side. The signals used in this interface are as follows:

- CT103-TXD2
- CT104-RXD2

Signals ~CT105-RTS2 and ~CT106-CTS2 are not used; default hardware flow control on UART2 should be de-activated using AT command **AT+IFC=0,0**. Refer to document [2] Firmware 7.43 AT Commands Manual.

The signal ~CT105-RTS2 must be pulled down.

The other signals and their multiplexed GPIOs are not available.

Refer to document [2] Firmware 7.43 AT Commands Manual for more information.

4.9. SIM Interface

The Subscriber Identification Module (SIM) may be directly connected to the Q2687 Refreshed embedded module via this dedicated interface. This interface controls either a 3V or a 1V8 SIM and it is fully compliant with GSM 11.11 recommendations concerning SIM functions.

The five signals used by this interface are as follows:

- SIM-VCC: SIM power supply
- ~SIM-RST: reset
- SIM-CLK: clock
- SIM-IO: I/O port
- SIMPRES: SIM card detect

4.9.1. Pin Description

Refer to the following table for the pin description of the SIM interface.

Table 27. SIM Pin Description

Pin Number	Signal	I/O	I/O Type	Reset State	Description	Multiplexed With
9	SIM-VCC	O	2V9 / 1V8		SIM Power Supply	Not mux
11	SIM-IO	I/O	2V9 / 1V8	*Pull-up	SIM Data	Not mux
12	SIMPRES	I	1V8	Z	SIM Card Detect	GPIO18
13	~SIM-RST	O	2V9 / 1V8	0	SIM Reset	Not mux
14	SIM-CLK	O	2V9 / 1V8	0	SIM Clock	Not mux

* SIM-IO pull-up is about 10kΩ.

Refer to section 4.2 Electrical Information for Digital I/O for open drain, 2V8 and 1V8 voltage characteristics and reset state definitions.

4.9.2. Electrical Characteristics

Refer to the following table for the electrical characteristics of the SIM interface.

Table 28. Electrical Characteristics of the SIM Interface

Parameter	Conditions	Minimum	Typical	Maximum	Unit
SIM-IO V_{IH}	I_{IH} = ± 20µA	0.7xSIMVCC			V
SIM-IO V_{IL}	I_{IL} = 1mA			0.4	V
~SIM-RST, SIM-CLK V_{OH}	Source current = 20µA	0.9xSIMVCC			V
SIM-IO V_{OH}	Source current = 20µA	0.8xSIMVCC			
~SIM-RST, SIM-IO, SIM-CLK V_{OL}	Sink current = -200µA			0.4	V

Parameter	Conditions	Minimum	Typical	Maximum	Unit
SIM-VCC Output Voltage	SIMVCC = 2.9V IVCC= 1mA	2.84	2.9	2.96	V
	SIMVCC = 1.8V IVCC= 1mA	1.74	1.8	1.86	V
SIM-VCC current	VBATT = 3.6V			10	mA
SIM-CLK Rise/Fall Time	Loaded with 30pF		20		ns
~SIM-RST, Rise/Fall Time	Loaded with 30pF		20		ns
SIM-IO Rise/Fall Time	Loaded with 30pF		0.7	1	µs
SIM-CLK Frequency	Loaded with 30pF			3.25	MHz

Note: When SIMPRES is used, a low to high transition means that a SIM card is inserted and a high to low transition means that the SIM card is removed.

4.9.3. Application

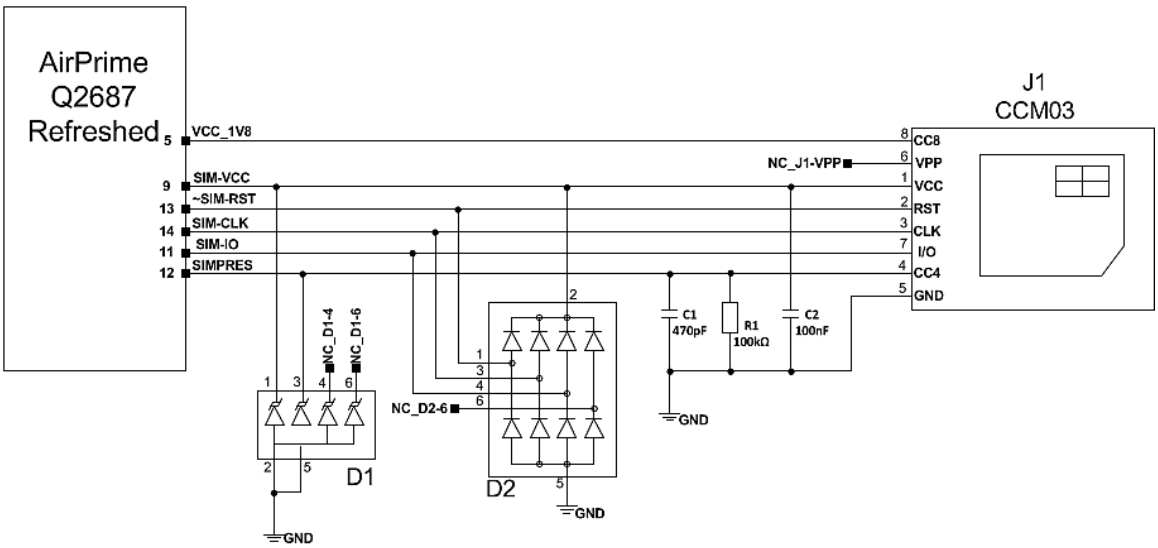


Figure 26. Example of a Typical SIM Socket Implementation

It is recommended to add Transient Voltage Suppressor diodes (TVS) on the signal(s) connected to the SIM socket in order to prevent any electrostatic discharge.

TVS diodes with low capacitance (less than 10pF) have to be connected on SIM-CLK and SIM-IO signals to avoid any disturbance of the rising and falling edge. These types of diodes are mandatory for the Full Type Approval and should be placed as close to the SIM socket as possible.

4.9.3.1. SIM Socket Pin Description

The following table lists the SIM socket pin description.

Table 29. SIM Socket Pin Description

Pin Number	Signal	Description
1	VCC	SIM-VCC
2	RST	~SIM-RST
3	CLK	SIM-CLK
4	CC4	SIMPRES with 100 kΩ pull down resistor
5	GND	GROUND
6	VPP	Not connected
7	I/O	SIM-IO
8	CC8	VCC_1V8 of the Q2687 Refreshed embedded module (pin 5)

4.9.3.2. Recommended Components

- R1 :100KΩ
- C1 :470pF
- C2 :100nF

Note: Note that this capacitor, C2, on the SIM-VCC line must not exceed 330nF.

- D1 :ESDA6V1SC6 from ST
- D2 :DALC208SC6 from SGS-THOMSON/ST Microelectronics
- J1 :ITT CANNON CCM03 series (Refer to section 11.2 SIM Card Reader.)

4.9.4. Embedded SIM

The Q26SM703RD ESIM module allows the selection of an external or embedded SIM by the software-controlled embedded SIM-Switch. Open AT Application Framework 2.33 or later can drive the embedded SIM-Switch automatically. The default configuration of the firmware is to use an external SIM. With the absence of an external SIM, this configuration is automatically switched to use the embedded SIM. The module **MUST** be reset every time there is a change in SIM selection by AT command.

The embedded SIM personalization can be made by a card-maker through the external SIM interface of the module.

4.9.4.1. AT Commands for SIM Selection

To select the internal or an external SIM, the AT Command, **AT+WHCNF**, can be used.

Table 30. Useful AT Commands for SIM Selection

AT Command	Description
AT+WHCNF=4,0	External SIM preferred, default configuration

AT Command	Description
AT+WHCNF=4,1	External SIM
AT+WHCNF=4,2	Embedded SIM
AT+WHCNF=4,3	Read the embedded SIM-Switch selected mode status
AT+CFUN=1	Reset the module

Note: The embedded module must be reset after changing the SIM selection.

For more information, refer to document [2] Firmware 7.43 AT Commands Manual.

4.10. USB 2.0 Interface

A 4-wire USB slave interface is available on the Q2687 Refreshed embedded module that complies with USB 2.0 protocol signaling, but not with the electrical interface due to the 5V interface of VPAD-USB.

The signals used by the USB interface are as follows:

- VPAD-USB
- USB-DP
- USB-DM
- GND

The USB 2.0 interface also features the following:

- 12Mbit/s full-speed transfer rate
- 3.3V type compatible
- USB Soft connect feature
- Download feature is not supported by USB
- CDC 1.1 – ACM compliant

Note: A 5V to 3.3V typical voltage regulator is needed between the external interface power in line (+5V) and the Q2687 Refreshed embedded module line (VPAD-USB).

4.10.1. Pin Description

Refer to the following table for the pin description of the USB interface.

Table 31. USB Pin Description

Pin Number	Signal	I/O	I/O Type	Description
52	VPAD-USB	I	VPAD_USB	USB Power Supply
54	USB-DP	I/O	VPAD_USB	Differential data interface positive
56	USB-DM	I/O	VPAD_USB	Differential data interface negative

4.10.2. Electrical Characteristics

Refer to the following table for the electrical characteristics of the USB interface.

Table 32. Electrical Characteristics of the USB Interface

Parameter	Minimum	Typical	Maximum	Unit
VPAD-USB, USB-DP, USB-DM	3	3.3	3.6	V
VPAD_USB Input current consumption		8		mA

4.10.3. Application

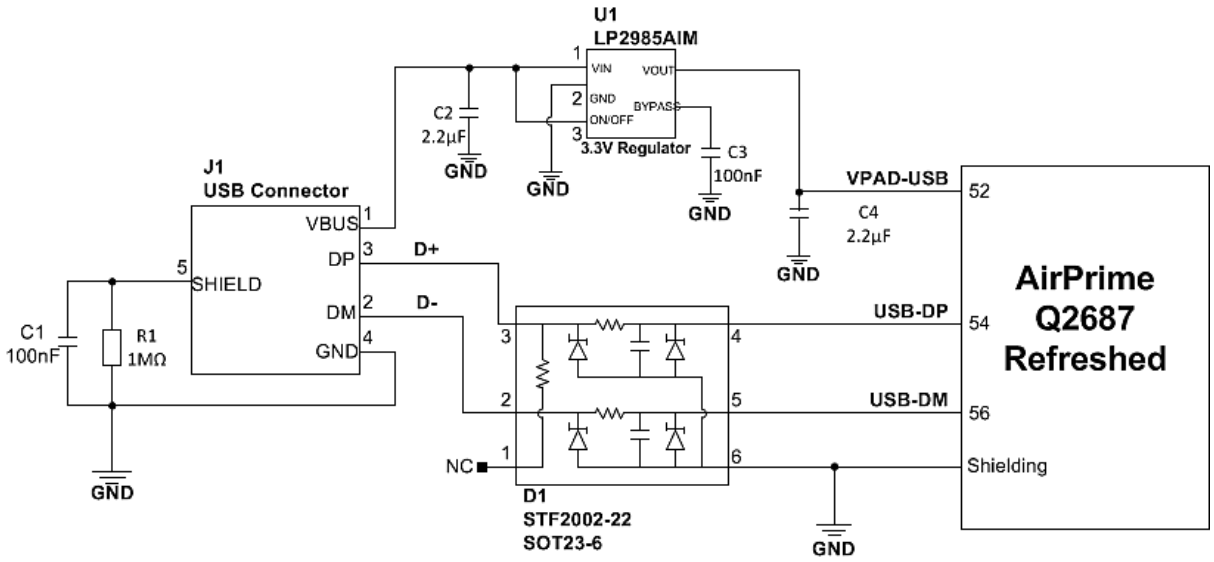


Figure 27. Example of a USB Implementation

The regulator used is a 3.3V regulator and it is supplied through J1 when the USB wire is plugged.

D1 is an EMI/RFI filter with ESD protection. The internal pull-up resistor of D1 which is used to detect the interface's full speed is not connected because it is embedded into the embedded module.

Note that both R1 and C1 have to be close to J1.

4.10.3.1. Recommended Components

- R1 :1MΩ
- C1, C3 :100nF
- C2, C4 :2.2µF
- D1 :STF2002-22 from SEMTECH
- U1 :LP2985AIM 3.3V from NATIONAL SEMICONDUCTOR

4.11. RF Interface

The RF (radio frequency) interface of the Q2687 Refreshed Embedded Module allows the transmission of RF signals. This interface has a 50Ω nominal impedance and a 0Ω DC impedance.

4.11.1. RF Connections

The antenna cable and connector should be selected in order to minimize loss in the frequency bands used for GSM 850/900MHz and 1800/1900MHz. The maximum value of loss considered between the Q2687 Refreshed embedded module and an external connector is 0.5dB.

The Q2687 Refreshed embedded module does not support an antenna switch for a car kit, but this function can be implemented externally and can be driven using a GPIO.

4.11.1.1. UFL Connector

A wide variety of cables fitted with UFL connectors from different suppliers may be used. For more information, refer to section 9.5.5.1 UFL/SMA Connector.

4.11.1.2. Soldered Solution

The soldered solution will preferably be based on an RG178 coaxial cable. For more information, refer to section 9.5.5.2 Coaxial Cable.

4.11.1.3. Precidip Connector

This connector is compatible with Precidip and is dedicated for board-to-board applications and must be soldered on the customer board. The recommended supplier is as follows:

Preci-dip SA for the Precidip connector (reference: 9PM-SS-0003-02-248//R1)

For more information, refer to section 9.5.5.3 Precidip Connector.

4.11.2. RF Performance

The RF performance is compliant with ETSI GSM 05.05 recommendations.

The main receiver parameters are:

- GSM850 Reference Sensitivity = -109 dBm typical (Static & TUHigh)
- E-GSM900 Reference Sensitivity = -109 dBm typical (Static & TUHigh)
- DCS1800 Reference Sensitivity = -108 dBm typical (Static & TUHigh)
- PCS1900 Reference Sensitivity = -108 dBm typical (Static & TUHigh)
- Selectivity @ 200 kHz: > +9 dBc
- Selectivity @ 400 kHz: > +41 dBc
- Linear dynamic range: 63 dB
- Co-channel rejection: >= 9 dBc

The main transmitter parameters are:

- Maximum output power (EGSM & GSM850): 33 dBm +/- 2 dB at ambient temperature
- Maximum output power (GSM1800 & PCS1900): 30 dBm +/- 2 dB at ambient temperature
- Minimum output power (EGSM & GSM850): 5 dBm +/- 5 dB at ambient temperature
- Minimum output power (GSM1800 & PCS1900): 0 dBm +/- 5 dB at ambient temperature

4.11.3. Antenna Specifications

The antenna must meet the requirements specified in the table below.

The optimum operating frequency depends on the application. A dual-band, tri-band or quad-band antenna should operate in these frequency bands and have the following characteristics.

Table 33. Antenna Specifications

Characteristic		E-GSM 900	DCS 1800	GSM 850	PCS 1900
TX Frequency		880 to 915 MHz	1710 to 1785 MHz	824 to 849 MHz	1850 to 1910 MHz
RX Frequency		925 to 960 MHz	1805 to 1880 MHz	869 to 894 MHz	1930 to 1990 MHz
Impedance		50Ω			
VSWR	**RX max**	1.5:1			
	TX max	1.5:1			
Typical Radiated Gain		0dBi in one direction at least			

Note: Sierra Wireless recommends a maximum VSWR of 1.5:1 for both TX and RX bands. Even so, all aspects of this specification will be fulfilled even with a maximum VSWR of 2:1.

For the list of antenna recommendations, refer to section 11.5 Antenna Cable.

4.11.3.1. Application

The antenna should be isolated as much as possible from analog and digital circuitry (including interface signals).

On applications with an embedded antenna, poor shielding could dramatically affect the receiving sensitivity. Moreover, the power radiated by the antenna could affect the application (TDMA noise, for instance).

As a general recommendation, all components or chips operated at high frequencies (microprocessors, memories, DC/DC converter) or other active RF parts should not be placed too close to the Q2687 Refreshed embedded module. In the event that this happens, the correct power supply layout and shielding should be designed and validated.

Components near RF connections or unshielded feed lines must be prohibited.

RF lines must be kept as short as possible to minimize loss.

4.12. Analog Audio Interface

The Q2687 Refreshed Embedded Module supports two microphone inputs and two speaker outputs. It also includes an echo cancellation and a noise reduction feature which allows for an improved quality of hands-free functionality.

In some cases, ESD protection must be added on the audio interface lines.

4.12.1. Pin Description

The following table lists the pin description of the analog audio interface.

Table 34. Analog Audio Pin Description

Pin Number	Signal	I/O	I/O Type	Description
40	MIC1P	I	Analog	Microphone 1 positive input
38	MIC1N	I	Analog	Microphone 1 negative input
36	MIC2P	I	Analog	Microphone 2 positive input
34	MIC2N	I	Analog	Microphone 2 negative input
35	SPK1P	O	Analog	Speaker 1 positive output
37	SPK1N	O	Analog	Speaker 1 negative output
39	SPK2P	O	Analog	Speaker 2 positive output
41	SPK2N	O	Analog	Speaker 2 negative output

4.12.2. Microphone Features

The microphone can be connected in either differential or single-ended mode. However, it is strongly recommended to use a differential connection in order to reject common mode noise and TDMA noise. When using a single-ended connection, be sure to have a very good ground plane, very good filtering, as well as shielding in order to avoid any disturbance on the audio path. Also note that using a single-ended connection decreases the audio input signal by 6dB as compared to using a differential connection.

The gain of both MIC inputs are internally adjusted and can be tuned using AT commands. For more information on AT commands, refer to document [2] Firmware 7.43 AT Commands Manual.

4.12.2.1. MIC1 Microphone Input

By default, MIC1 input is single-ended, but can be configured in differential mode.

The MIC1 input does not include an internal bias making it the standard input for an external headset or a hands-free kit. If an electret microphone is used, there must be external biasing that corresponds with the characteristics of the electret microphone used.

AC coupling is already embedded in the Q2687 Refreshed embedded module.

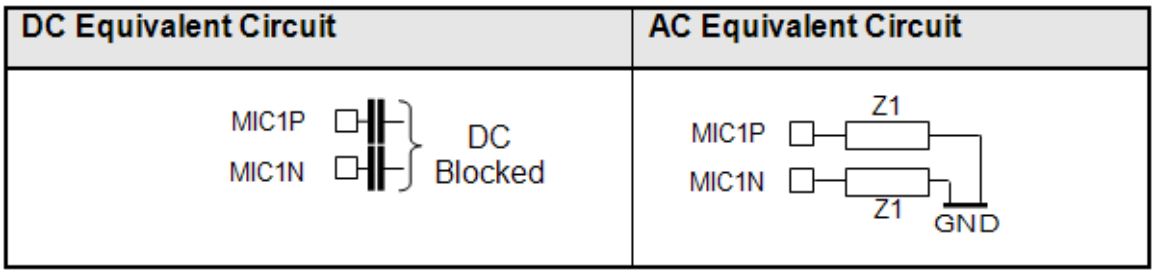


Figure 28. MIC1 Equivalent Circuits

Refer to the following table for the electrical characteristics of MIC1.

Table 35. Electrical Characteristics of MIC1

Parameter		Minimum	Typical	Maximum	Unit
DC Characteristics			N/A		V
AC Characteristics 200 Hz<F<4 kHz	Z1	70	120	160	kΩ
Working voltage (MIC1P-MIC1N)	AT+VGT*=3500(1)		13.8	18.6**	mVrms
	AT+VGT*=2000(1)		77.5	104**	mVrms
	AT+VGT*=700(1)		346	465**	mVrms
Maximum rating voltage (MIC1P or MIC1N)	Positive			+7.35	V
	Negative	-0.9			

* The input voltage depends on the input micro gain set by AT command. Refer to document [2] Firmware 7.43 AT Commands Manual.

** This value is obtained with digital gain = 0, for frequency = 1 kHz

(1) This value is given in dB, but it's possible to toggle it to index value. Refer to document [2] Firmware 7.43 AT Commands Manual for more information.

Caution: *The voltage input value for MIC1 cannot exceed the maximum working voltage; otherwise, clipping will appear.*

4.12.2.1.1. MIC1 Differential Connection Example

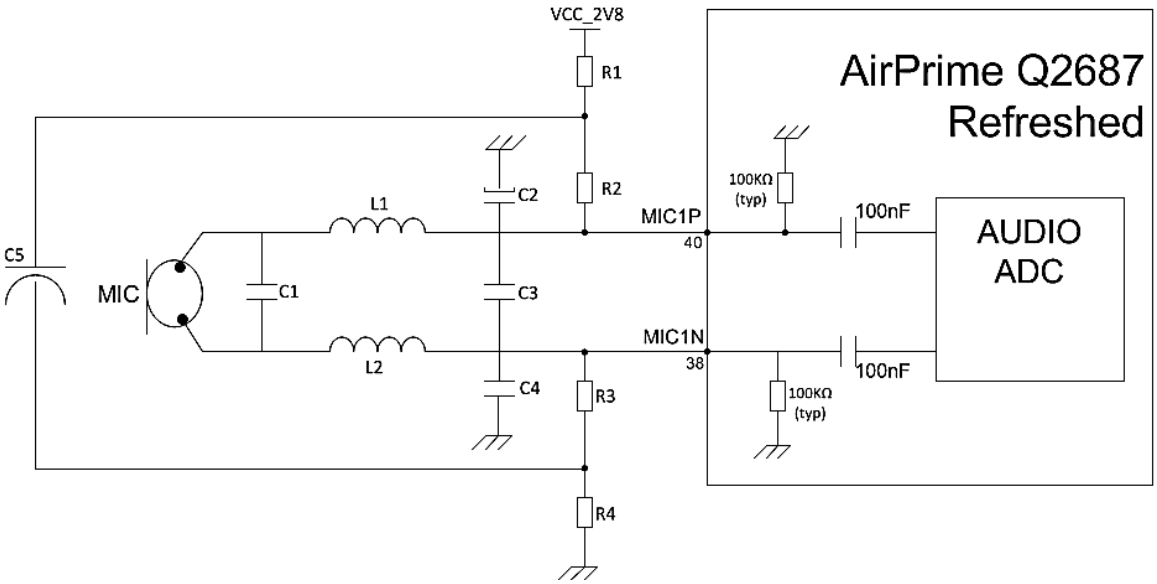


Figure 29. Example of a MIC1 Differential Connection with LC Filter

Audio quality can be very good without a filter (L1, L2, C2, C3 and C4), depending on the design. But if there is EMI perturbation, this filter can reduce TDMA noise. Note though that this filter is not mandatory. If the filter is not to be used, the capacitors must be removed and the coil replaced by 0Ω resistors as shown in the following diagram.

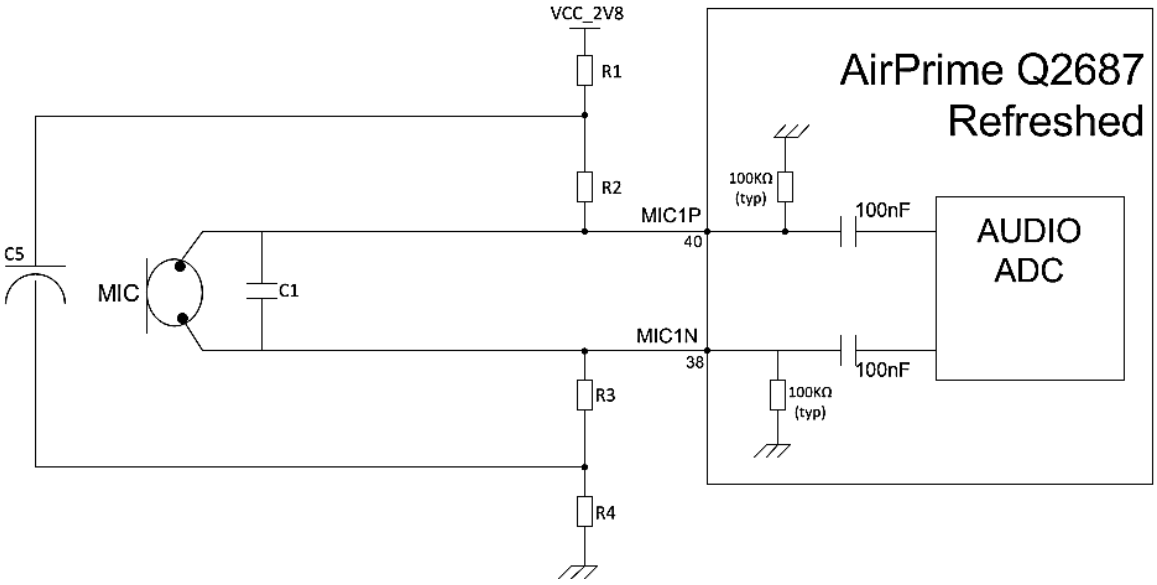


Figure 30. Example of a MIC1 Differential Connection without an LC Filter

Capacitor C1 is highly recommended to eliminate TDMA noise and it must be connected close to the microphone.

Although Vbias can be VCC_2V8 (pin 10) of the Q2687 Refreshed embedded module, it is recommended to use another 2V to 3V power supply voltage instead. This is because Vbias must be kept as “clean” as possible to avoid bad performance when a single-ended connection is used.

Caution: *TDMA noise may degrade quality when VCC_2V8 is used.*

The following table lists the recommended components to use in creating the LC filter.

Table 36. Recommended Components for a MIC1 Differential Connection

Component	Value	Notes
R1	4.7kΩ	For Vbias equal to 2.8V.
R2, R3	820Ω	
R4	1kΩ	
C1	12pF to 33pF	Must be tuned depending on the design.
C2, C3, C4	47pF	Must be tuned depending on the design.
C5	2.2µF +/- 10%	
L1, L2	100nH	Must be tuned depending on the design.

4.12.2.1.2. MIC1 Single-Ended Connection Example

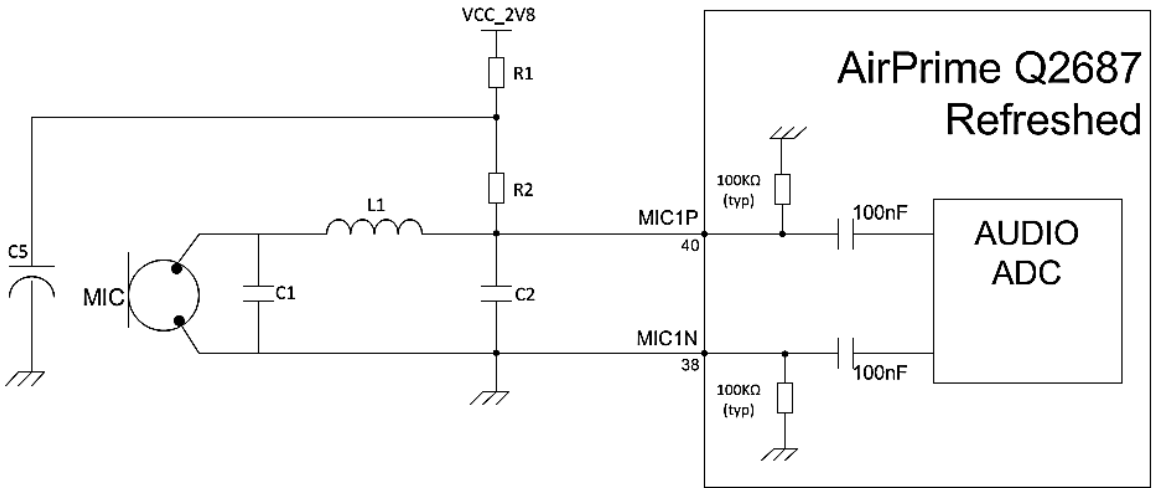


Figure 31. Example of a MIC1 Single-Ended Connection with LC Filter

The single-ended design is not recommended for improving TDMA noise rejection as it is usually difficult to eliminate TDMA noise from a single-ended design.

It is recommended to use an LC filter (L1 and C2) to eliminate TDMA noise. Note though that this filter is not mandatory. If the filter is not to be used, the capacitor C2 must be removed and the coil replaced by 0Ω resistors as shown in the following diagram.

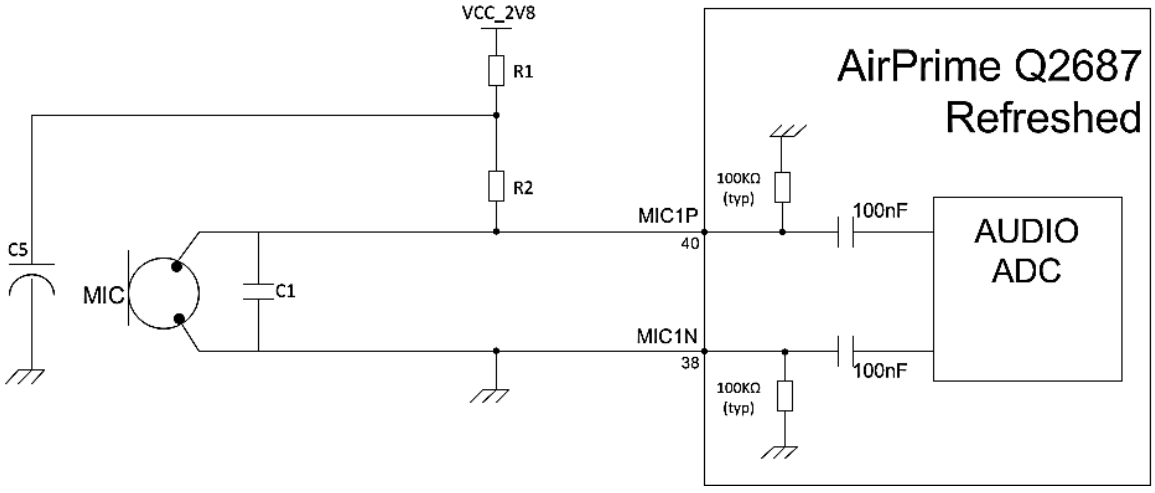


Figure 32. Example of a MIC1 Single-Ended Connection without an LC Filter

The capacitor, C1, is highly recommended to eliminate TDMA noise and it must be connected close to the microphone.

Although Vbias can be VCC_2V8 (pin 10) of the Q2687 Refreshed embedded module, it is recommended to use another 2V to 3V power supply voltage instead. This is because Vbias must be kept as “clean” as possible to avoid bad performance when a single-ended connection is used.

Caution: *TDMA noise may degrade quality when VCC_2V8 is used.*

The following table lists the recommended components to use in creating the LC filter.

Table 37. Recommended Components for a MIC1 Single-Ended Connection

Component	Value	Notes
R1	4.7kΩ	For Vbias equal to 2.8V.
R2	820Ω	
C1	12pF to 33pF	Must be tuned depending on the design.
C2	47pF	Must be tuned depending on the design.
L1	100nH	Must be tuned depending on the design.

4.12.2.2. MIC2 Microphone Input

By default, MIC2 input is differential, but can be configured in single-ended mode.

The MIC2 input already includes biasing for an electret microphone and the electret microphone may be directly connected to this input.

AC coupling is already embedded in the Q2687 Refreshed embedded module.

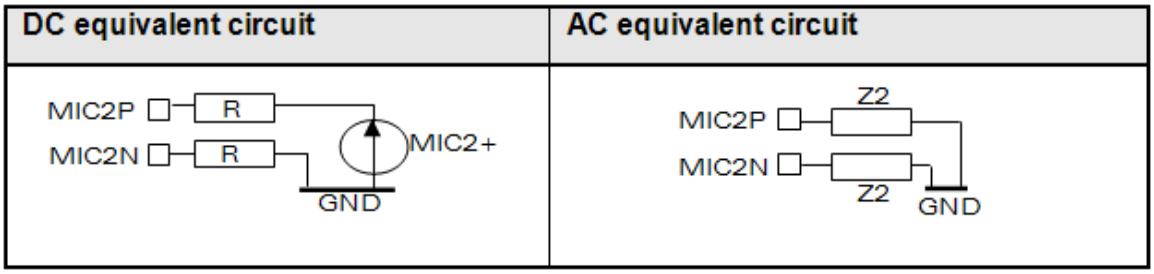


Figure 33. MIC2 Equivalent Circuits

Refer to the following table for the electrical characteristics of MIC2.

Table 38. Electrical Characteristics of MIC2

Parameter		Minimum	Typical	Maximum	Unit
Parameters Internal biasing DC Characteristics	MIC2+	2	2.1	2.2	V
	Output current		0.5	1.5	mA
	R2	1650	1900	2150	Ω

Parameter		Minimum	Typical	Maximum	Unit
AC Characteristics 200 Hz<F<4 kHz	Z2 MIC2P (MIC2N=Open)	1.1	1.3	1.6	kΩ
	Z2 MIC2N (MIC2P=Open)				
	Z2 MIC2P (MIC2N=GND)	0.9	1.1	1.4	
	Z2 MIC2N (MIC2P=GND)				
	Impedance between MIC2P and MIC2N	1.3	1.6	2	
Working voltage (MIC2P-MIC2N)	AT+VGT*=3500(1)		13.8	18.6***	mVrms
	AT+VGT*=2000(1)		77.5	104***	
	AT+VGT*=700(1)		346	466***	
Maximum rating voltage (MIC2P or MIC2N)	Positive			+7.35**	V
	Negative	-0.9			

* The input voltage depends of the input micro gain set by AT command. Refer to document [2] Firmware 7.43 AT Commands Manual.

** Because MIC2P is internally biased, it is necessary to use a coupling capacitor to connect an audio signal provided by an active generator. Only a passive microphone can be directly connected to the MIC2P and MIC2N inputs.

*** This value is obtained with digital gain = 0, for frequency = 1 kHz

(1) This value is given in dB, but it's possible to toggle it to index value. Refer to document [2] Firmware 7.43 AT Commands Manual.

Caution: *The voltage input value for MIC2 cannot exceed the maximum working voltage; otherwise, clipping will appear.*

4.12.2.2.1. MIC2 Differential Connection Example

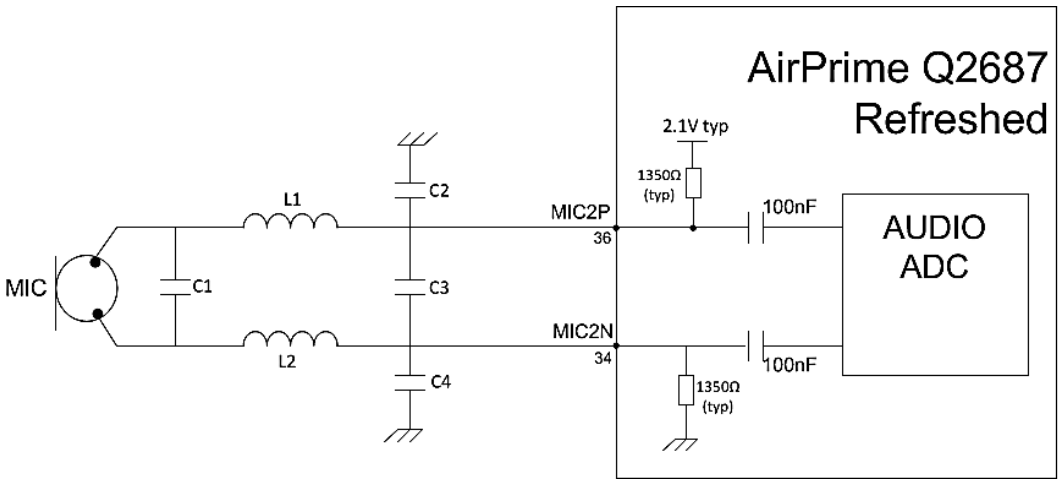


Figure 34. Example of a MIC2 Differential Connection with LC Filter

Audio quality can be very good without a filter (L1, L2, C2, C3 and C4), depending on the design. But if there is EMI perturbation, this filter can reduce TDMA noise. Note though that this filter is not mandatory. If the filter is not to be used, the capacitors must be removed and the coil replaced by 0Ω resistors as shown in the following diagram.

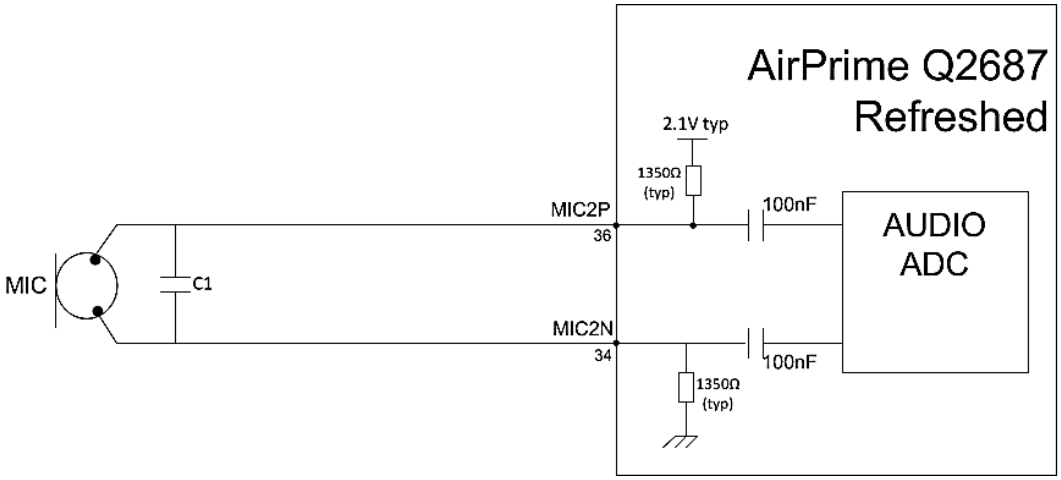


Figure 35. Example of a MIC2 Differential Connection without an LC Filter

Capacitor C1 is highly recommended to eliminate TDMA noise and it must be connected close to the microphone.

The following table lists the recommended components to use in creating the LC filter.

Table 39. Recommended Components for a MIC2 Differential Connection

Component	Value	Notes
C1	12pF to 33pF	Must be tuned depending on the design.
C2, C3, C4	47pF	Must be tuned depending on the design.
L1, L2	100nH	Must be tuned depending on the design.

4.12.2.2.2. MIC2 Single-Ended Connection Example

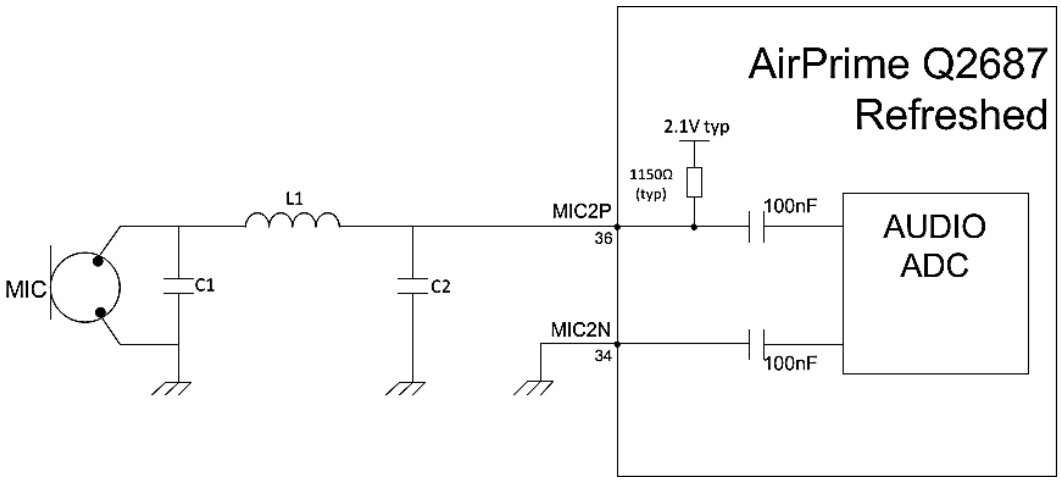


Figure 36. Example of a MIC2 Single-Ended Connection with LC Filter

The single-ended design is not recommended for improving TDMA noise rejection as it is usually difficult to eliminate TDMA noise from a single-ended design.

The internal input resistor value becomes 1150Ω due to the connection of MIC2N to the ground.

It is recommended to use an LC filter (L1 and C2) to eliminate TDMA noise. Note though that this filter is not mandatory. If the filter is not to be used, the capacitor C2 must be removed and the coil replaced by 0Ω resistors as shown in the following diagram.

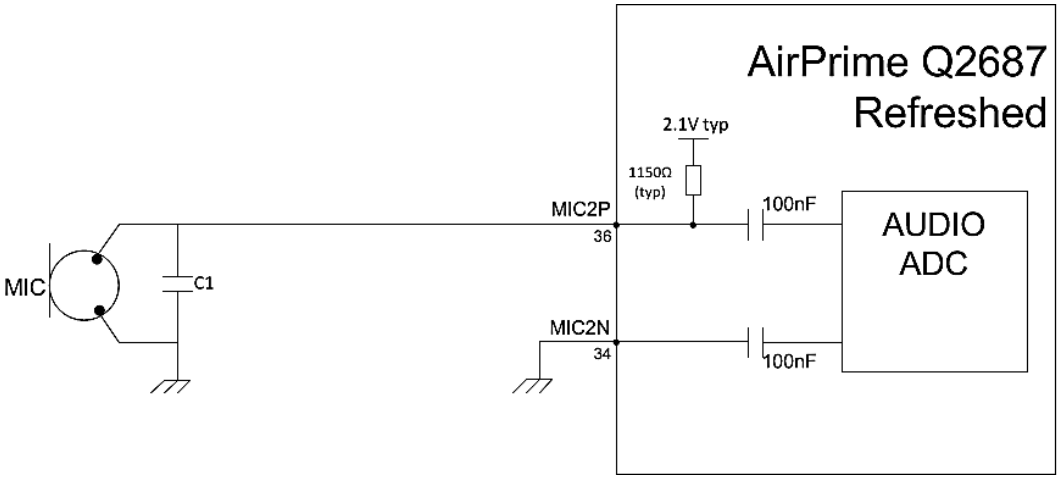


Figure 37. Example of a MIC2 Single-Ended Connection without an LC Filter

The capacitor, C1, is highly recommended to eliminate TDMA noise and it must be connected close to the microphone.

The following table lists the recommended components to use in creating the LC filter.

Table 40. Recommended Components for a MIC2 Single-Ended Connection

Component	Value	Notes
C1	12pF to 33pF	Must be tuned depending on the design.
C2		Must be tuned depending on the design.
L1		Must be tuned depending on the design.

4.12.3. Speaker Features

There are two different speaker channels, SPK1 and SPK2, available on the Q2687 Refreshed embedded module. The connection on SPK1 is fixed as single-ended, but SPK2 may be configured in either differential or single-ended mode.

However, as with the microphone connection, it is strongly recommended to use a differential connection in order to reject common mode noise and TDMA noise. Furthermore, using a single-ended connection entails losing power (the power is divided by 4 in a single-ended connection) as compared to using a differential connection.

Note that when using a single-ended connection, a very good ground plane, very good filtering, as well as shielding is needed in order to avoid any disturbance on the audio path.

The gain of each speaker output channel is internally adjusted and can be tuned using AT commands. For more information on AT commands, refer to document [2] Firmware 7.43 AT Commands Manual.

No discreet components like resistors or capacitors are needed when using this interface.

The following table lists the typical values of both speaker outputs.

Table 41. Speaker Information

Parameter	Typical	Unit	Connection
Z (SPK1P, SPK1N)	16 or 32	Ω	Single-ended mode
Z (SPK2P, SPK2N)	4	Ω	Single-ended mode
Z (SPK2P, SPK2N)	8	Ω	Differential mode

4.12.3.1. Speakers Output Power

The maximum power output of SPK1 and SPK2 are not similar because of the difference in their configuration. Because SPK2 can be connected in differential mode, it can provide more power compared to SPK1 which only allows single-ended connections. The maximal specifications given below are available with the maximum power output configuration values set by AT command, and the typical values are recommended.

Caution: *It is mandatory not to exceed the maximal speaker output power and the speaker load must be in accordance with the gain selection (gain is controlled by AT command). Exceeding beyond the specified maximal output power may damage the Q2687 Refreshed embedded module.*

4.12.3.2. SPK1 Speaker Output

SPK1 only allows for a single-ended connection.

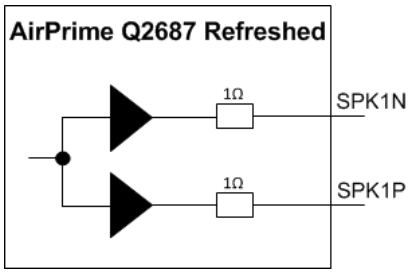


Figure 38. SPK1 Equivalent Circuits

Refer to the following table for the electrical characteristics of SPK1.

Table 42. Electrical Characteristics of SPK1

Parameter			Minimum	Typical	Maximum	Unit
Biasing voltage	-			1.30		V
Output swing voltage	RL=16Ω: AT+VGR=-1600**; single-ended		-	1.7	-	Vpp
	RL=32Ω; AT+VGR=-1600**; single-ended		-	1.9	2.75	Vpp
RL	Load resistance		14.5	32	-	Ω
IOUT	Output current; single-ended; peak value	RL=16Ω	-	40	85	mA
		RL=32Ω	-	22	-	mA
POUT	RL=16Ω; AT+VGR*=-1600**		-	25		mW
	RL=32Ω; AT+VGR*=-1600**		-	16	27	mW

Parameter		Minimum	Typical	Maximum	Unit
RPD	Output pull-down resistance at power-down	28	40	52	kΩ

* The output voltage depends of the output speaker gain set by AT command. Refer to document [2] Firmware 7.43 AT Commands Manual.

** This value is given in dB, but it's possible to toggle it to index value. Refer to document [2] Firmware 7.43 AT Commands Manual.

4.12.3.3. SPK2 Speaker Output

SPK2 can have either a single-ended or a differential connection.

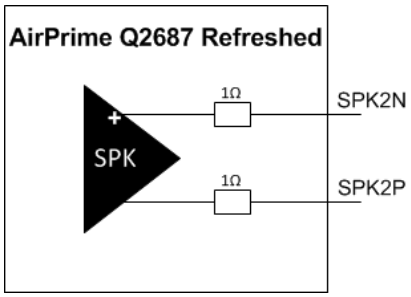


Figure 39. SPK2 Equivalent Circuits

Refer to the following table for the electrical characteristics of SPK2.

Table 43. Electrical Characteristics of SPK2

Parameter		Minimum	Typical	Maximum	Unit
Biasing voltage	SPK2P and SPK2N		1.30		V
Output swing voltage	RL=8Ω: AT+VGR=-1000*; single ended	-	-	2	Vpp
	RL=8Ω: AT+VGR=-1000*; differential	-	-	4	Vpp
	RL=32Ω: AT+VGR=-1000*; single ended	-	-	2.5	Vpp
	RL=32Ω: AT+VGR=-1000*; differential	-	-	5	Vpp
RL	Load resistance	6	8	-	Ω
IOUT	Output current; peak value; RL=8Ω	-	-	180	mA
POUT	RL=8Ω; AT+VGR=-1000*;	-	-	250	mW
RPD	Output pull-down resistance at power-down	28	40	52	kΩ
VPD	Output DC voltage at power-down	-	-	100	mV

* The output voltage depends of the output speaker gain set by AT command. This value is given in dB, but it's possible to toggle it to index value. Refer to document [2] Firmware 7.43 AT Commands Manual.

If a single-ended connection is used with SPK2, only one of either SPK2 has to be chosen. The result is a maximal output power divided by 4.

4.12.3.4. Differential Connection Example

Figure 40. Example of an SPK Differential Connection

The impedance of the speaker amplifier output in differential mode is **R ≤ 1Ω +/-10%**.

Note that the connection between the speaker and the Q2687 Refreshed embedded module pins must be designed to keep the serial impedance lower than 3Ω when it is connected in differential mode.

4.12.3.5. Single-Ended Connection Example

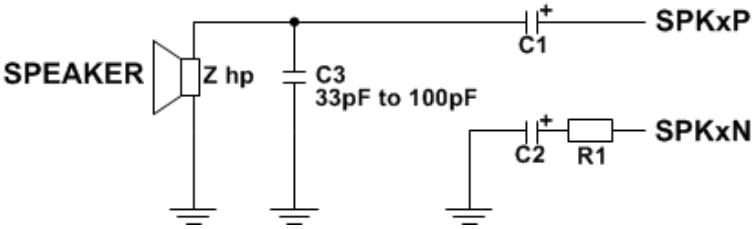


Figure 41. Example of an SPK Single-Ended Connection

Take note of the following when connecting the speaker in single-ended mode:

- 6.8µF < C1 < 47µF (depending on the characteristics of the speaker and the output power)
- C1 = C2
- R1 = Zhp

Again, note that using a single-ended connection includes losing power (-6dB) as compared to a differential connection.

In the case of a 32Ω speaker, a cheaper and smaller solution can be implemented where R1 = 82Ω and C2 = 6.8µF (ceramic).

Note that the connection between the speaker and the Q2687 Refreshed embedded module pins must be designed to keep the serial impedance lower than 1.5Ω when it is connected in single-ended mode.

Lastly, when the SPK1 channel is used, only SPK1P is useful in a single-ended connection and SPK1N can be left open.

4.12.3.6. Recommended Characteristics

- Type :10mW, electro-magnetic
- Impedance
  - Z = 8Ω for hands-free (SPK2)
  - Z = 32Ω for headset kit (SPK1)
- Sensitivity :110dB SPL minimum (0dB = 20µPa)
- Frequency response must be compatible with GSM specifications

4.13. Digital Audio Interface (PCM)

The Digital Audio Interface (PCM) interface allows connectivity with standard audio peripherals. It can be used, for example, to connect an external audio codec.

The programmability of this interface allows addressing a large range of audio peripherals.

The signals used by the Digital Audio Interface are as follows:

- **PCM-SYNC (output)**: The frame synchronization signal delivers an 8kHz frequency pulse that synchronizes the frame data in and the frame data out.
- **PCM-CLK (output)**: The frame bit clock signal controls data transfer with the audio peripheral.
- **PCM-OUT (output)**: The frame “data out” relies on the selected configuration mode.
- **PCM-IN (input)**: The frame “data in” relies on the selected configuration mode.

The Digital Audio Interface also features the following:

- IOM-2 compatible device on physical level
- Master mode only with 6 slots by frame, user only on slot 0
- Bit rate single clock mode at 768kHz only
- 16 bits data word MSB first only
- Linear Law only (no compression law)
- Long Frame Synchronization only
- Push-pull configuration on PCM-OUT and PCM-IN

Note that the digital audio interface configuration cannot differ from those specified above.

4.13.1. PCM Waveforms

The following figures describe the PCM Frame and Sampling waveforms.

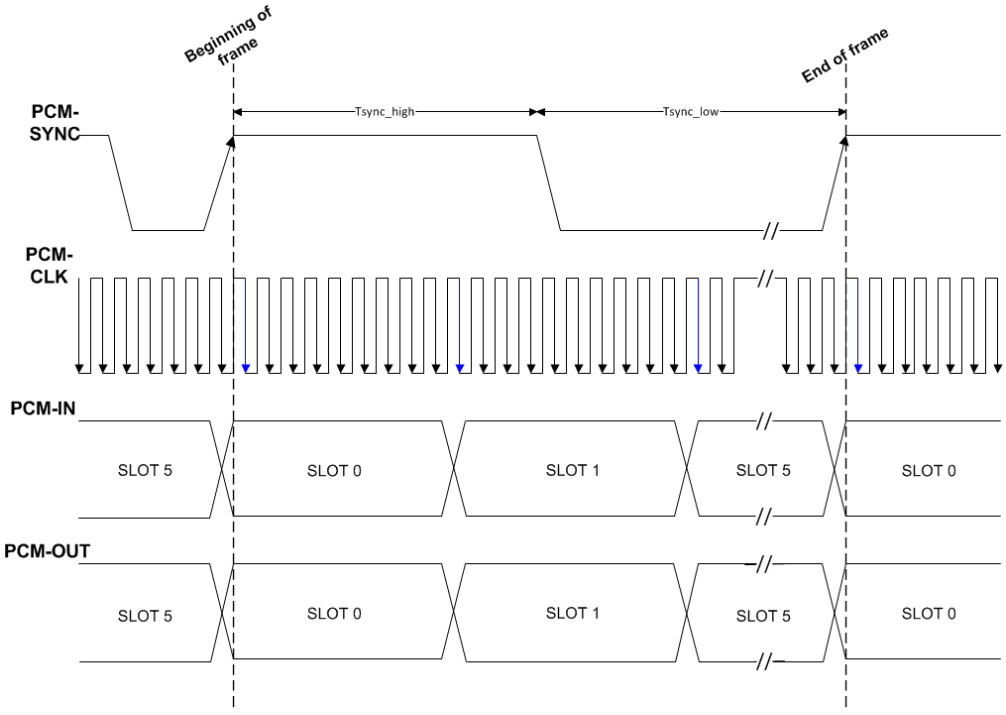


Figure 42. PCM Frame Waveform

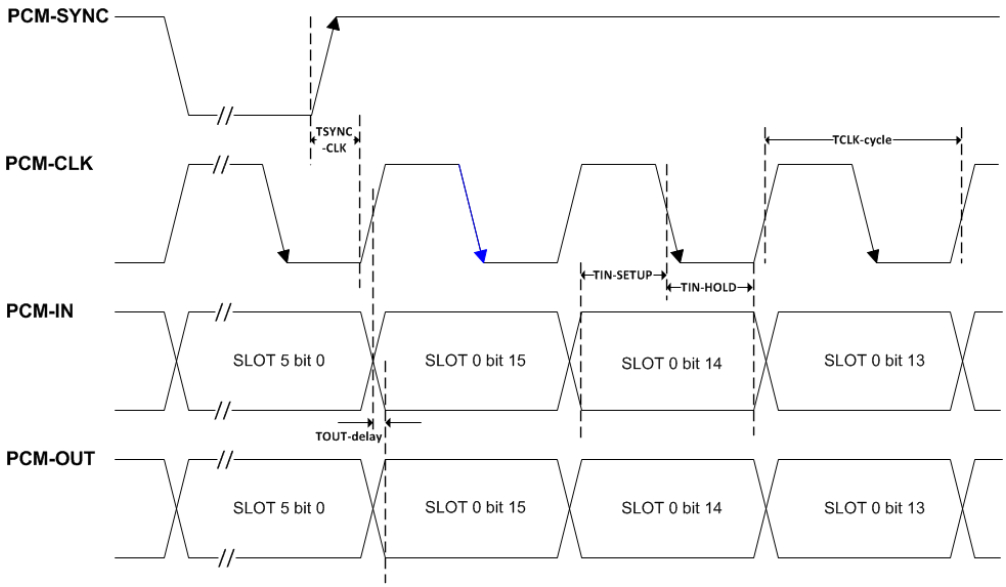


Figure 43. PCM Sampling Waveform

Refer to the following table for the AC characteristics of the digital audio interface.

Table 44. AC Characteristics of the Digital Audio Interface

Signal	Description	Minimum	Typical	Maximum	Unit
Tsync_low + Tsync_high	PCM-SYNC period		125		µs
Tsync_low	PCM-SYNC low time		93		µs
Tsync_high	PCM-SYNC high time		32		µs
TSYNC-CLK	PCM-SYNC to PCM-CLK time		-154		ns
TCLK-cycle	PCM-CLK period		1302		ns
TIN-setup	PCM-IN setup time	50			ns
TIN-hold	PCM-IN hold time	50			ns
TOUT-delay	PCM-OUT delay time			20	ns

4.13.2. Pin Description

Refer to the following table for the pin description of the digital audio (PCM) interface.

Table 45. PCM Interface Pin Description

Pin Number	Signal	I/O	I/O Type*	Reset State	Description
77	PCM-SYNC	O	1V8	Pull-down	Frame synchronization 8kHz
78	PCM-IN*	I	1V8	Pull-up	Data input
79	PCM-CLK	O	1V8	Pull-down	Data clock
80	PCM-OUT	O	1V8	Pull-up	Data output

* When using analog audio interface, the PCM_In signal should be in Hz.

Refer to section 4.2 Electrical Information for Digital I/O for open drain, 2V8 and 1V8 voltage characteristics and reset state definitions.

4.14. Battery Charging Interface

The Q2687 Refreshed embedded module supports one battery charging circuit, two algorithms and one hardware charging mode (pre-charging) for the following battery types:

- Ni-Cd (Nickel-Cadmium)
- Ni-Mh (Nickel-Metal Hydride)
- Li-Ion (Lithium-Ion) with the embedded PCM (Protection Circuit Module) algorithm 1

Note: Li-Ion batteries must be used with embedded PCM (protection circuit module).

The Q2687 Refreshed embedded module charging circuit is composed of a transistor switch which connects the CHG-IN signal (pins 6 and 8) to the VBATT signal (pins 1, 2, 3 and 4). This switch is then controlled by the two charging algorithms – algorithm 0 and algorithm 1.

Caution: *Voltage is forbidden on the CHG-IN signal if no battery is connected to the VBATT signal.*

The charger DC power supply must have an output current limited to 800mA and that the maximum charger output current provided to the battery must also correspond to the battery's electrical characteristics.

The algorithms control the frequency and the connected time of the switching. During the charging procedure, the battery charging level is monitored and when the Li-Ion algorithm is used, the battery temperature is also monitored via the ADC1/BAT-TEMP input.

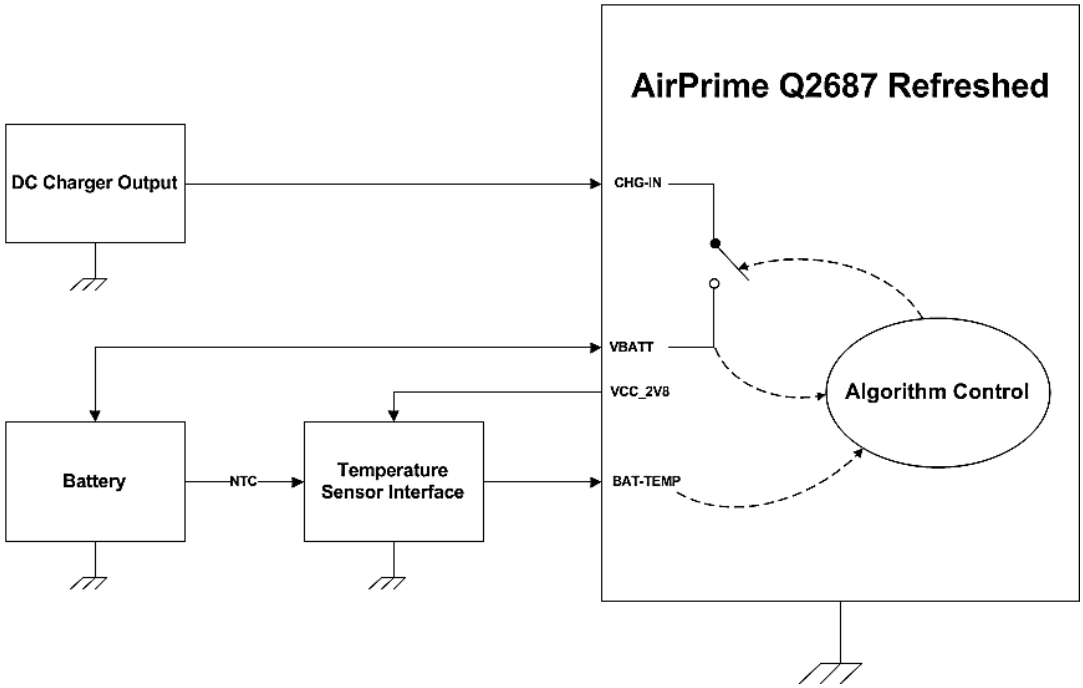


Figure 44. Battery Charging Diagram

One more charging procedure provided by the Q2687 Refreshed embedded module is the hardware charging mode which is also called "pre-charging". This is a special charging mode as it is only activated when the Q2687 Refreshed embedded module is OFF. The goal of this charging mode is to avoid battery damage by preventing the battery from being discharged to a level that is lower than the specified minimum battery level. Control of this mode is managed by hardware.

To use the battery charging functionality of the Q2687 Refreshed embedded module, 3 hardware parts are needed:

- Charger Power Supply – this provides a DC current power supply limited to 800mA, with a voltage range that corresponds to the battery and the Q2687 Refreshed embedded module specifications.
- Battery – the battery charging functionality must only be used with a rechargeable battery. The three supported battery types are: Ni-Cd, Ni-Mh and Li-Ion.
- Analog Temperature Sensor – this is only used for Li-Ion batteries to monitor their temperatures. This sensor is composed of an NTC sensor and several resistors.

4.14.1. Charging Algorithms

The Open AT Application Framework provides the charging algorithms for Li-ion, Ni-Mh and Ni-Cd type batteries.

Algorithm 0 is used for Ni-Mh and Ni-Cd type batteries, while algorithm 1 is used for Li-Ion type batteries. Temperature monitoring is only performed when using algorithm 1.

Both charging algorithms are controlled by two AT commands:

- **AT+WBCI**
- **AT+WBCM**

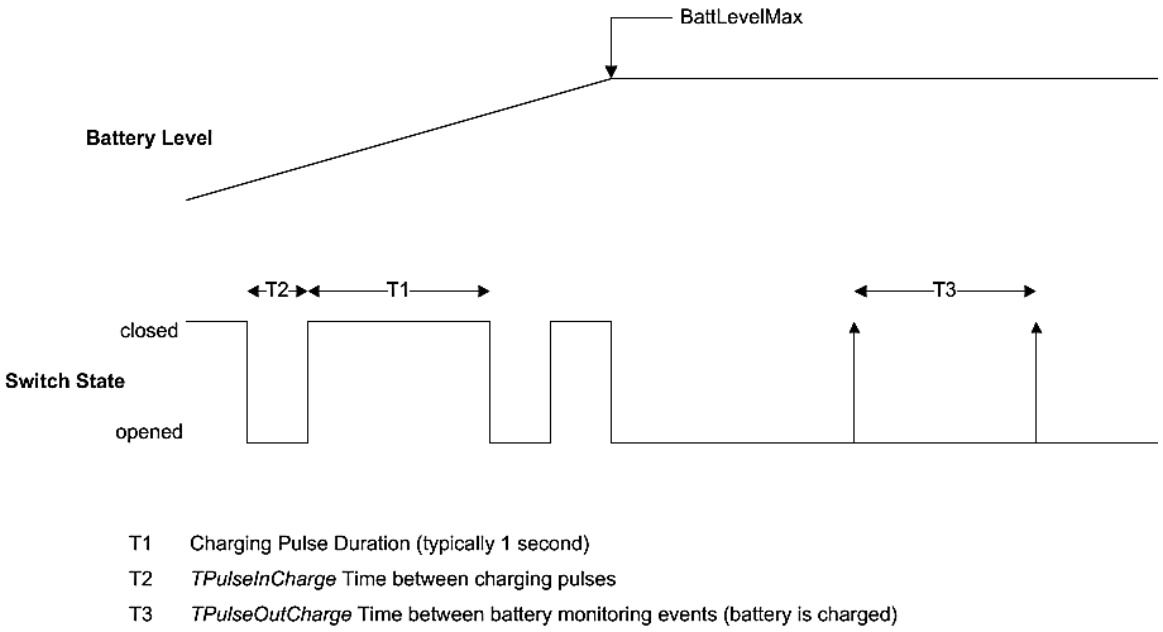
These two AT commands are used to set the charging battery parameters, select the type of battery and starts/stops the battery charging. Refer to document [2] Firmware 7.43 AT Commands Manual for more information about these AT commands.

Note: *In the following sub-sections, the parameters in bold and italic type can be modified with the **AT+WBCM** command.*

4.14.1.1. Ni-Cd/Ni-Mh Charging Algorithm

This algorithm measures the battery voltage when the DC switch is open (T2). If the voltage is below ***BattLevelMax***, the switch is closed (T1) to charge the battery. The switch is then re-opened for a time specified by ***TPulseInCharge*** (typically 100ms) and then the switch is closed again.

When the battery voltage has reached ***BattLevelMax***, the software monitors the battery voltage (typically every 5seconds; defined by ***TPulseOutCharge***) and the switch state is left open for time T3.



T1 Charging Pulse Duration (typically 1 second)
T2 *TPulseInCharge* Time between charging pulses
T3 *TPulseOutCharge* Time between battery monitoring events (battery is charged)

Figure 45. Ni-Cd/Ni-Mh Charging Waveform

Refer to the following table for the electrical characteristics of the Ni-Cd and Ni-Mh battery timing charge.

Table 46. Electrical Characteristics of Ni-Cd/Ni-Mh Battery Timing Charge

Parameter	Minimum	Typical	Maximum	Unit
T1		1		s
T2		0.1		s
T3		5		s

T1, T2, T3 and ***BattLevelMax*** may be configured using AT commands. For more information, refer to document [2] Firmware 7.43 AT Commands Manual.

Note: Only the battery level, and not the temperature, is monitored by the software.

4.14.1.2. Li-Ion Charging Algorithm

The Li-Ion algorithm provides battery temperature monitoring, which is highly recommended to prevent battery damage during the charging phase.

The Li-Ion charger algorithm can be broken down into three phases:

1. Beginning of pulse charge – this is the beginning of the alternating pulse charge (1second) and rest (100ms).
2. Constant current charge – this is when the battery voltage reaches ***DedicatedVoltStart*** (4.1V on the graph below, but specified as 4.0V as default value).
3. End of pulse charge – this is when the rest period lasts longer because the voltage has exceeded ***BattLevelMax*** (4.3V by default) during the rest period.

The three phases can be seen on the following waveform for full charging:

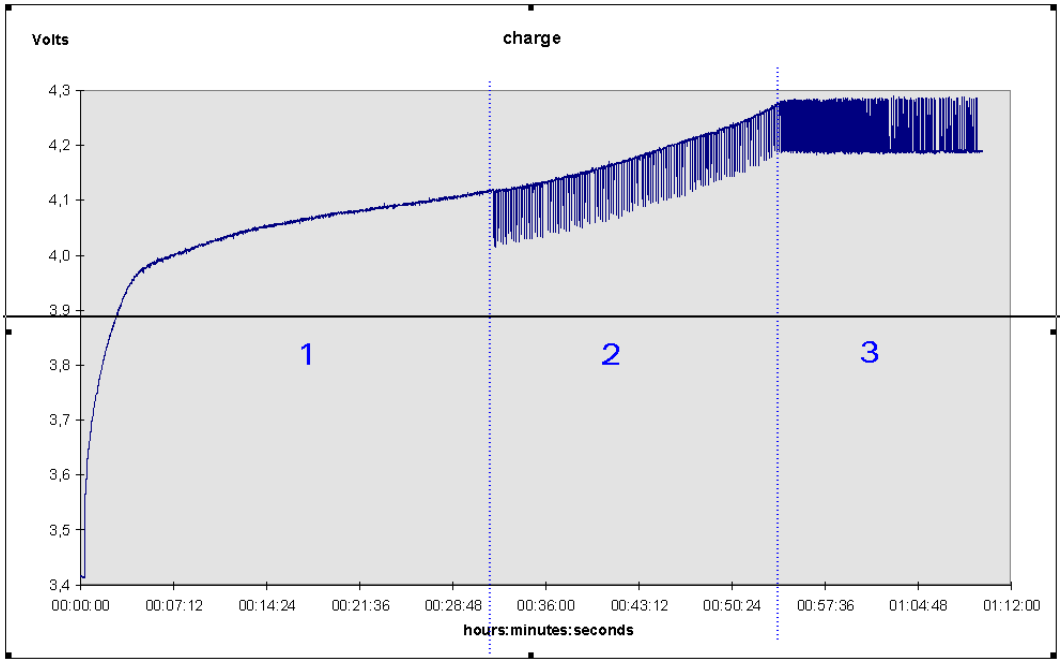


Figure 46. Li-Ion Full Charging Waveform

In the diagram above, the charge was done with an empty battery in order to know the maximum duration of a full charge; and in this specific example, complete charging took more than an hour.

The charging stops when the battery voltage has exceeded 4.3V (by default) and when the rest time between pulses has reached 10seconds. For more information, refer to section 4.14.1.2.2 Rest in Between Pulses in Phase 3.

Caution: *If the Li-Ion battery is locked by its PCM when it is plugged for the first time, charging will not take place. The Q2687 Refreshed embedded module cannot release the PCM protection inside the Lithium battery pack.*

The following table lists the electrical characteristics of the Li-Ion battery timing charge.

Table 47. Electrical Characteristics of Li-Ion Battery Timing Charge

Parameter		Minimum	Typical	Maximum	Unit
Phase 1 switching	Closed		Always		s
Phase 2 switching	Open		0.1		s
	Closed		1		s
Phase 3 switching	Open	0.1		10	s
	Closed		1		s

4.14.1.2.1. Pulse Appearance in Phase 2

The pulse is always 1second long and does not depend on the battery voltage. The pulse charge starts when while charging, the battery voltage reaches ***DedicatedVoltStart***. At the beginning of the pulse charge, the battery voltage looks like a square signal with a 91% duty cycle.

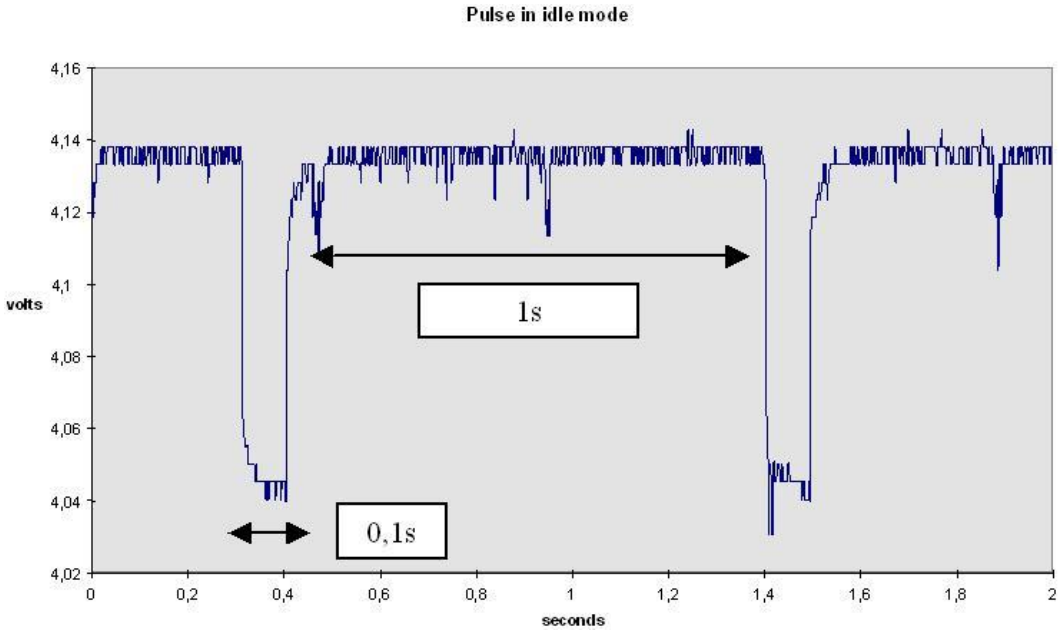


Figure 47. Phase 2 Pulse

This lasts for as long as the voltage has not exceeded ***BattLevelMax*** while resting.

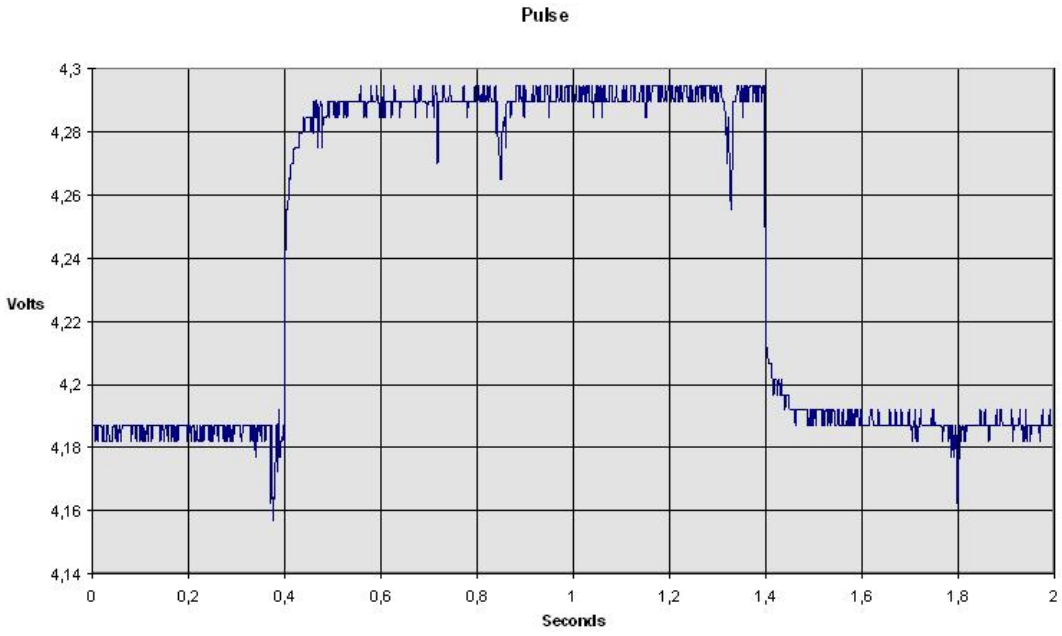


Figure 48. Phase 2 Rest

4.14.1.2.2. Rest in Between Pulses in Phase 3

At the end of the charge when the battery is almost full, the rest period between the two pulses lasts as long as the voltage stays beyond 4.2V.

When this happens, the pulse length remains the same but the rest time between the two pulses increases regularly until it reaches 10 seconds. (The minimum rest time is 100ms.)

If this period lasts more than 10 seconds, then the charge stops (as the battery is then fully charged).

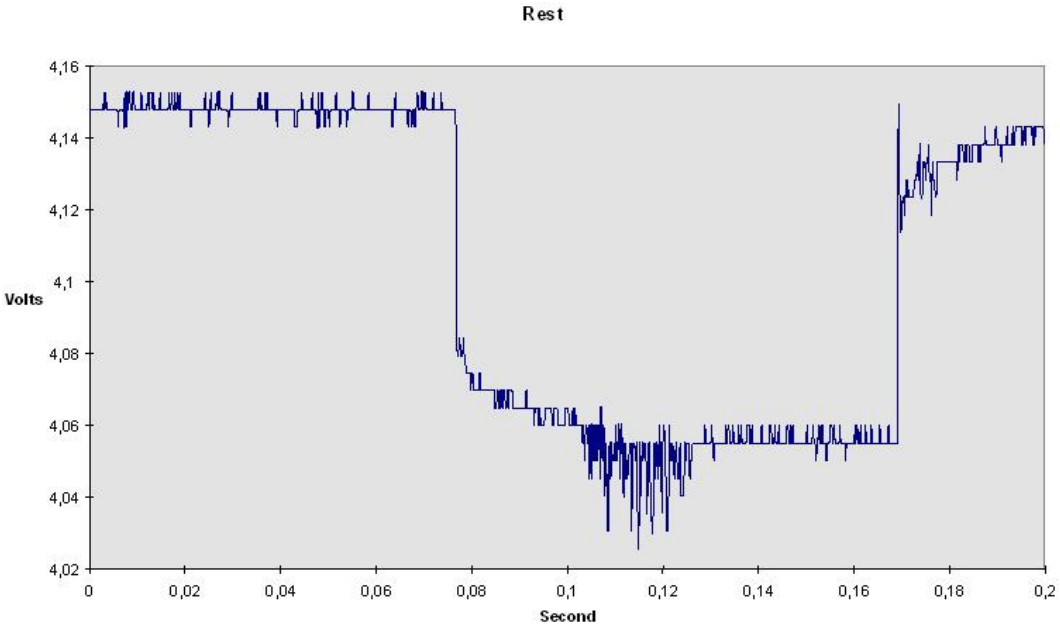


Figure 49. Phase 3 Switch

4.14.2. Pre-Charging

When a DC power supply is connected to the CHG-IN input and if the battery voltage is between 2.8V[1] and 3.2V, a constant current of 50mA is provided to the battery to prevent it from being discharged below the specified minimum battery level.

When the battery is able to supply the Q2687 Refreshed embedded module, it is automatically powered on and the software algorithm is activated to finish the charge.

When pre-charging is launched, LED0 blinks automatically.

4.14.3. Temperature Monitoring

Temperature monitoring is only available for the Li-Ion battery with algorithm 1. ADC1/BAT-TEMP (pin 20) input must be used to sample the analog temperature signal provided by an NTC temperature sensor. The minimum and maximum temperature range may be set by AT command.

Refer to the following table for the pin description of the battery charging interface.

Table 48. Battery Charging Interface Pin Description

Pin Number	Signal	I/O	I/O Type	Description
6, 8	CHG-IN	I	Analog	Current source input
20	ADC1/BAT-TEMP	I	Analog	A/D converter

[1] For the Lithium-ion battery, the minimum voltage must be higher than the PCM lock level. Take note that if the voltage goes below the PCM lock level (in this case, 2.8V), charging is not guaranteed.

Refer to the following table for the electrical characteristics of the battery charging interface.

Table 49. Electrical Characteristics of the Temperature Monitoring Feature

Parameter			Minimum	Typical	Maximum	Unit
Charging operating temperature (for non-ESIM modules)			0		50	°C
Charging operating temperature (for the Q26SM703RD)			-40	25	85	°C
ADC1/BAT-TEMP (pin 20)	Maximum output code			1635		LSB
	Sampling rate			216		S/s
	Input Impedance (R)			1M		Ω
	Input signal range		0		2	V
CHG-IN (pin 6, 8)	Voltage (for I=Imax)		4.6*			V
	Voltage (for I=0)	non-ESIM modules			6*	V
		Q26SM703RD			6.5*	
	Current Imax		400**		800	mA

* To be configured as specified by the battery manufacturer.

** Be careful as this value has to be selected in function of the power consumption mode used. Refer to the power consumption tables in section 6 Power Consumption for more information.

4.14.4. Application

The VCC_2V8 voltage provided by the Q2687 Refreshed embedded module can be used to polarize the NTC sensor. However, additional resistors (R1 and R2) must be used to adjust the maximum voltage from the ADC input to 2V.

If another polarized voltage is used, the resistors must be adjusted accordingly.

Note that it is not recommended to use the VCC_1V8 voltage.

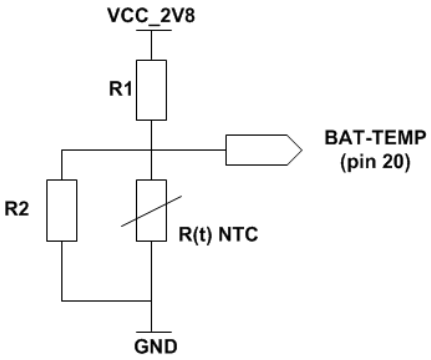


Figure 50. Example of an ADC Application

The R(t) resistor is the NTC and should be placed close to the battery. Usually, it is integrated into the battery.

4.14.4.1. Temperature Computation Method

The following computations and values represent the ambient temperature in °C.

The resistor value depends on the temperature:

$$R(t) = R(t_0)\ e^{B\left(\frac{1}{t+273}-\frac{1}{t_0+273}\right)}$$

- t_o represents the ambient temperature (+25°C) associated to $R(t_o)$ which is the nominal resistor
- B is the thermal sensibility (4250K)
- t represents the temperature in °C

$$R(t) = R(t_0)\ e^{B\left(\frac{25-t}{298*(t+273)}\right)}$$

$$V_{BAT-TEMP} = \frac{(R(t)//R2)}{(R(t)//R2)+R1} * VCC\_2V8$$

$$BatteryTemperature(mV) = V_{BAT-TEMP} * 1000$$

For more information about NTC equations, refer to your NTC provider specifications.

4.14.5. Charger Recommendations

The following table specifies the charger recommendations.

Table 50. Charger Recommendations

Parameter	Minimum	Typical	Maximum	Unit	Remarks
Input voltage	90		265	Vrms	
Input frequency	45		65	Hz	
Output voltage limit			6	V	No load
Output voltage limit	4.6			V	Io max
Output current	(1)	1C(2)	(3)	mA	
Output Voltage			150	mVpp	Io max
Ripple					Vout=5.3V

(1) See the cell battery specifications for current charging conditions.

(2) 1C = Nominal capacity (of the battery cell).

(3) See the cell battery specifications for current charging conditions. T1 and D1 must be chosen according to the nominal capacity battery cell.

It is recommended to let the output voltage (Vo) drop to less than 1.18V in less than 1second when the AC/DC adapter is unplugged.

4.15. Temperature Sensor Interface

A temperature sensor is implanted in the Q2687 Refreshed embedded module which is used to detect the temperature in the embedded module. The software can be used to report the temperature via **ADC3**. For more details about **ADC3**, refer to document [2] Firmware 7.43 AT Commands Manual.

Note: ADC3 is not available during network initialization.

The following waveform describes the characteristic of this function.

The average step of the Q2687 Refreshed is 13mV/°C and the formula for computing the temperature sensor output is as follows:

VTemp (V) = -0.013 x Temperature (°C) + 1.182

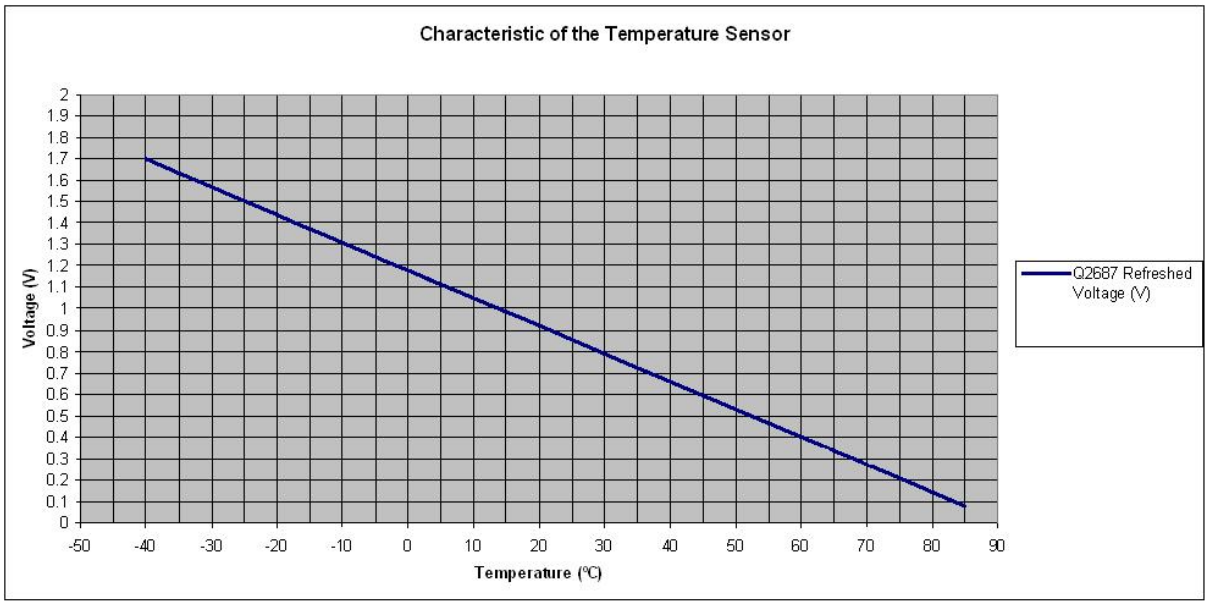


Figure 51. Temperature Sensor Characteristics

5. Signals and Indicators

5.1. ON/~OFF Signal

This input is used to switch the Q2687 Refreshed embedded module ON or OFF.

A HIGH level signal must be provided on the ON/~OFF pin to switch the Q2687 Refreshed embedded module ON. The voltage of this signal has to be maintained higher than 0.8 x VBATT for a minimum of 1500ms. This signal can be left at HIGH level until switched off.

To switch the Q2687 Refreshed embedded module OFF, the ON/~OFF signal must be reset and an **AT+CPOF** command must be sent to the embedded module.

5.1.1. Pin Description

Refer to the following table for the pin description of the ON/~OFF signal.

Table 51. ON/~OFF Signal Pin Description

Pin Number	Signal	I/O	I/O Type	Description
19	ON/~OFF	I	CMOS	Embedded Module Power-ON

Refer to section 4.2 Electrical Information for Digital I/O for open drain, 2V8 and 1V8 voltage characteristics and reset state definitions.

5.1.2. Electrical Characteristics

Refer to the following table for the electrical characteristics of the ON/~OFF signal.

Table 52. Electrical Characteristics of the ON/~OFF Signal

Parameter	I/O Type	Minimum	Maximum	Unit
V_{IL}	CMOS		VBATT x 0.2	V
V_{IH}	CMOS	VBATT x 0.8	VBATT	V

Caution: *All external signals must be inactive when the embedded module is OFF to avoid any damage when starting and to allow the embedded module to start and stop correctly.*

5.1.3. Power-ON

Once the embedded module is supplied through VBATT, the application must set the ON/OFF signal to high to start the embedded module power-ON sequence. The ON/OFF signal must be held high during a minimum delay of $\mathbf{T_{on/off\text{-}hold}}$ (minimum hold delay on the ON/~OFF signal) to power-ON. After this delay, an internal mechanism maintains the embedded module in power-ON condition.

During the power-ON sequence, an internal reset is automatically performed by the embedded module for 40ms (typical). During this phase, any external reset should be avoided.

Once initialization is completed (timing is SIM and network dependent), the AT interface answers the application with "OK". For further details, refer to document [2] Firmware 7.43 AT Commands Manual.

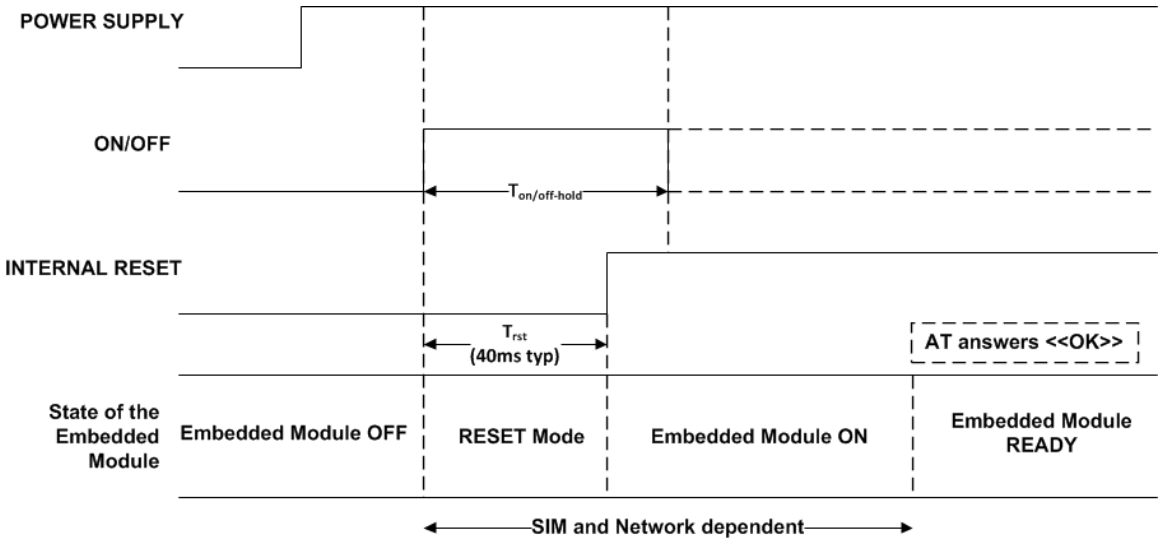


Figure 52. Power-ON Sequence (no PIN code activated)

The duration of the firmware power-ON sequence depends on the need to perform a recovery sequence if power has been lost during a flash memory modification.

Listed below are the other factors that have a minor influence on the power-ON sequence:

- The number of parameters stored in EEPROM by the AT commands received so far
- The ageing of the hardware components, especially the flash memory
- The temperature conditions

The *recommended* way to release the ON/~OFF signal is to use either an AT command or WIND indicators: the application has to detect the end of the power-up initialization and release the ON/~OFF signal afterwards.

To release the ON/~OFF signal, either of the following methods may be used:

- Using AT Command
  - An AT command is sent to the application. Once the initialization is complete, the AT interface will answer with «OK».

Note: If the application manages hardware flow control, the AT command can be sent during the initialization phase.

- Using WIND Indicators
  - If configured to do so, an unsolicited “+WIND: 3” message is returned after initialization. Note that the generation of this message is either enabled or disabled using AT command.

For more information on these commands, refer to document [2] Firmware 7.43 AT Commands Manual.

Proceeding thus, by software detection, will always prevent the application from releasing the ON/~OFF signal too early.

If WIND indicators are disabled or AT commands are unavailable or not used, it is still possible to release the ON/~OFF signal after a delay that is long enough (**$T_{on/off-hold}$**) to ensure that the firmware has already completed its power-up initialization.

The table below gives the minimum values of $T_{on/off-hold}$:

Table 53. $T_{on/off-hold}$ Minimum Values

Firmware	$T_{on/off-hold}$
	Safe Evaluations of the Firmware Power-Up Time
Firmware 7.43 (Open AT Application Framework 2.33)	8s

The value in the table above take the worst cases into account: power-loss recovery operations, slow flash memory operations in high temperature conditions, and so on. But they are safe because they are large enough to ensure that ON/~OFF is not released too early.

The typical power-up initialization time figures for best case conditions (no power-loss recovery, fast and new flash memory, etc.) is approximately 3.5 seconds in every firmware version. Note that releasing the ON/~OFF signal after this delay does not guarantee that the application will actually start-up (for example, the power plug has been pulled off during a flash memory operation, like a phone book entry update or an AT&W command).

The ON/~OFF signal can be left at a HIGH level until switched OFF. But this is not recommended as it will prevent the **AT+CPOF** command from performing a clean power-OFF.

When using a battery as power source, it is not recommended to let the ON/OFF signal high.

If the battery voltage is too low and the ON/~OFF signal is at LOW level, an internal mechanism switches the embedded module OFF. This automatic process prevents the battery from being over discharged and optimizes its life span.

During the power-ON sequence, an internal reset is automatically performed by the embedded module for 40 ms (typical). Any external reset should be avoided during this phase.

5.1.4. Power-OFF

Caution: *All external signals must be inactive when the embedded module is OFF to avoid any damage when starting.*

To properly power-OFF the embedded module, the application must reset the ON/OFF signal and then send the **AT+CPOF** command to unregister the module from the network and switch the embedded module OFF.

Once the response "OK" is returned by the embedded module, the external power supply can be switched OFF.

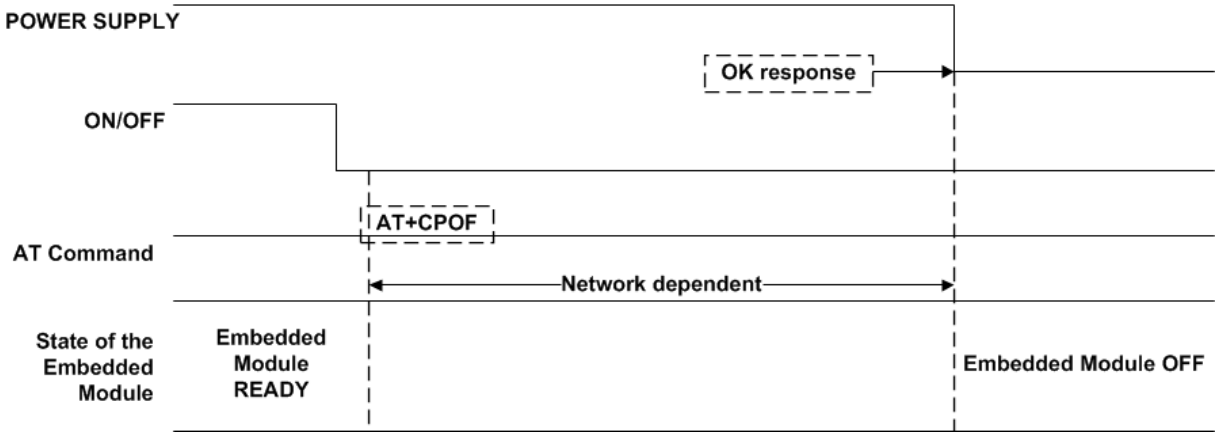


Figure 53. Power-OFF Sequence

If the ON/~OFF pin is maintained at ON (High Level), then the embedded module cannot be switched OFF.

Connecting a charger on the embedded module has exactly the same effect as connecting the ON/~OFF signal. Specifically, the embedded module will not power-OFF after the **AT+CPOF** command, unless the charger is disconnected.

5.1.5. Application

The ON/~OFF input (pin 19) is used to switch ON (ON/~OFF=1) or OFF (ON/~OFF=0) the Q2687 Refreshed embedded module.

A high level signal has to be provided on the ON/~OFF pin to switch the embedded module ON.

The level of the voltage of this signal has to be maintained at 0.8 x VBATT for a minimum of 2000ms.

This signal can be left at HIGH level until switched OFF.

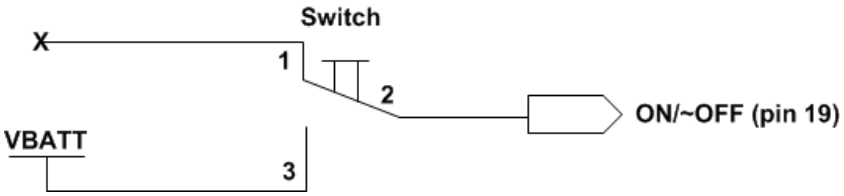


Figure 54. Example of ON/~OFF Pin Connection

5.1.6. When ON/~OFF is tied to VBATT

As shown in the power-ON sequence in Figure 52, the ON/~OFF signal must be set to High level after the power supply voltage is stable.

When the ON/~OFF signal is tied to VBATT, the VBATT ramp up (from 0V to 3.25V) must be made in less than 10ms. When the ramp up time is not achieved within a maximum of 10ms, power ON is not guaranteed unless one of the conditions listed in the table below is verified.

Table 54. Recommendations to Guarantee Power ON when ON/~OFF is tied to VBATT

Description	Implementation	Example
Supply power to BAT-RTC	Connect the power to the BAT-RTC pin of the module before and during power ON.	Connect the external power supply to BAT-RTC. Refer to the application example of BAT-RTC in section 5.4.3.
Delay in pulling the ON/OFF signal High	Apply High level on the ON/~OFF pin after VBATT reaches 3.25V.	• Use an external control signal to pull the ON/~OFF pin High at the appropriate time • Use a voltage detector IC to trigger the ON/~OFF signal when the VBATT voltage is more than or equal to 3.25V.
Hardware Reset	Once VBATT reaches 3.25V, issue an external hardware reset to the module.	Use an external control signal to trigger the hardware reset. Refer to the application example of Reset in section 5.2.4.

5.2. Reset Signal (~RESET)

This signal is used to force a reset procedure by providing the embedded module with a LOW level for at least 200µs. This signal must be considered as an emergency reset only. A reset procedure is already driven by the internal hardware during the power-up sequence.

This signal may also be used to provide a reset to an external device (at power-ON only). If no external reset is necessary, this input may be left open. If used (emergency reset), it must be driven either by an open collector or an open drain.

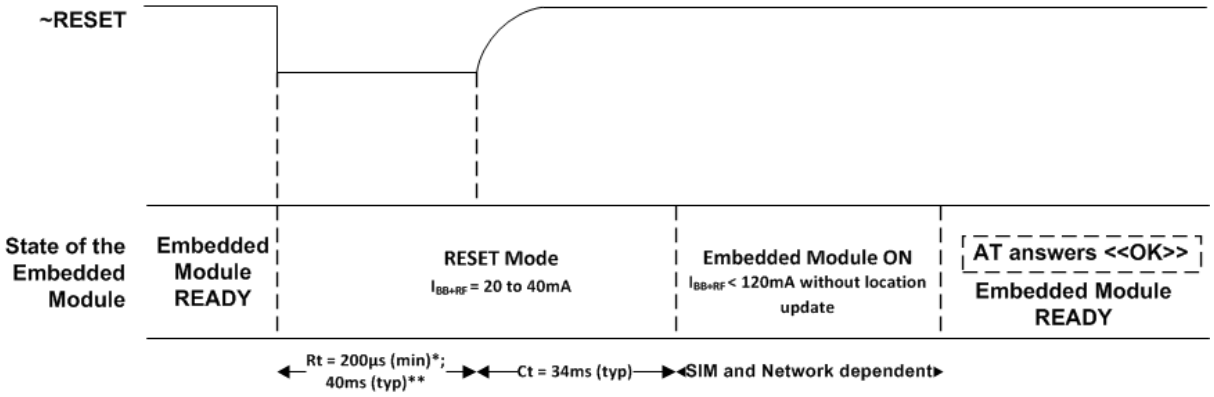
The embedded module remains in reset mode as long as the ~RESET signal is held LOW.

Note that an operating system reset is preferred to a hardware reset.

Caution: *This signal should only be used for EMERGENCY resets.*

5.2.1. Reset Sequence

To activate the "emergency" reset sequence, the ~RESET signal must be set to LOW for a minimum of 200µs. As soon as the reset is completed, the AT interface returns "OK" to the application.



* This reset time is the minimum time to be carried out on the ~RESET signal when the power supply is already stabilized.
** This reset time is internally carried out by the embedded module power supply supervisor only when the embedded module power supplies are powered ON.

Figure 55. Reset Sequence Waveform

At power-up, the ~RESET time (Rt) is carried out after switching the embedded module ON. It is generated by the internal voltage supervisor.

The ~RESET time is provided by the internal RC component. To keep the same time, it is not recommended to connect another R or C component <resistor or capacitor> on the ~RESET signal. Only a switch or an open drain gate is recommended.

Ct is the cancellation time required for the embedded module initialization. Ct is automatically carried out after hardware reset.

5.2.2. Pin Description

Refer to the following table for the pin description of the reset signal.

Table 55. Reset Signal Pin Description

Pin Number	Signal	I/O	I/O Type	Description
18	~RESET	I/O Open Drain	1V8	Embedded Module Reset

Refer to section 4.2 Electrical Information for Digital I/O for open drain, 2V8 and 1V8 voltage characteristics and reset state definitions.

5.2.3. Electrical Characteristics

Refer to the following table for the electrical characteristics of the reset signal.

Table 56. Electrical Characteristics of the Reset Signal

Parameter	Minimum	Typical	Maximum	Unit
Input Impedance (R)*		100		kΩ
Input Impedance (C)		10n		F
~RESET time (Rt)[1]	200			µs
~RESET time (Rt)[2] at power up only	20	40	100	ms
Cancellation time (Ct)		34		ms
V_H**	0.57			V
V_{IL}	0		0.57	V
V_{IH}	1.33			V

* Internal pull-up

** VH: Hysteresis Voltage

1 This reset time is the minimum to be carried out on the ~RESET signal when the power supply is already stabilized.

2 This reset time is internally carried out by the embedded module power supply supervisor only when the embedded module power supplies are powered ON.

5.2.4. Application

The ~RESET input (pin 18) is used to force a reset procedure by providing a LOW level for at least 200µs.

This signal has to be considered as an emergency reset only: a reset procedure is automatically driven by an internal hardware during the power-ON sequence.

This signal can also be used to provide a reset to an external device (it then behaves as an output).

If no external reset is necessary this input can be left open.

If used (emergency reset), it has to be driven by an open collector or an open drain output (due to the internal pull-up resistor embedded into the embedded module) as shown in the diagram below.

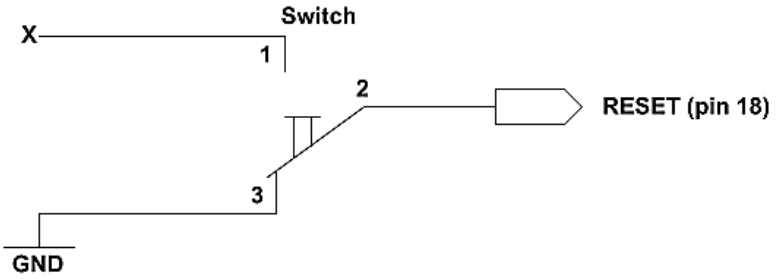


Figure 56. Example of ~Reset Pin Connection with Switch Configuration

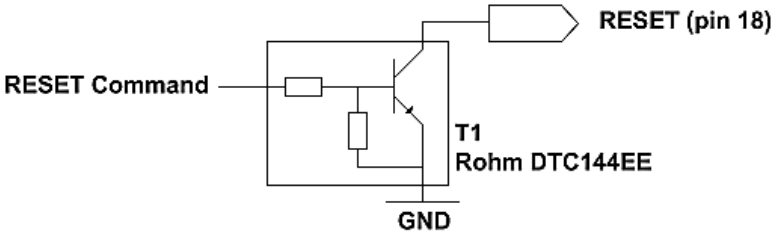


Figure 57. Example of ~Reset Pin Connection with Transistor Configuration

An open collector or open drain transistor can be used. If an open collector is chosen, T1 can be a ROHM DTC144EE.

Table 57. Reset Settings

Reset Command	~Reset (Pin 18)	Operating Mode
1	0	Reset activated
0	1	Reset inactive

5.3. BOOT Signal

A specific BOOT control pin is available to download to the Q2687 Refreshed embedded module (only if the standard XMODEM download, controlled with AT command, is not possible).

A specific PC software program, provided by Sierra Wireless, is needed to perform this specific download.

The BOOT pin must be connected to VCC_1V8 for this specific download.

Table 58. BOOT Settings

BOOT	Operating Mode	Comment
Leave open	Normal use	No download
Leave open	Download XMODEM	AT command for Download **AT+WDWL***
1	Download specific	Need Sierra Wireless PC software

* Refer to document [2] Firmware 7.43 AT Commands Manual for more information about this AT command.

5.3.1. Pin Description

Refer to the following table for the pin description of the Boot signal.

Table 59. Boot Signal Pin Description

Pin Number	Signal	I/O	I/O Type	Description
16	BOOT	I	1V8	Download mode selection

Refer to section 4.2 Electrical Information for Digital I/O for open drain, 2V8 and 1V8 voltage characteristics and reset state definitions.

For more information about using AT commands to manipulate this signal, refer to document [2] Firmware 7.43 AT Commands Manual.

Note that this BOOT pin must be left open for normal use or XMODEM download.

However, in order to render the development and maintenance phases easier, it is highly recommended to set a test point, either a jumper or a switch on the VCC_1V8 (pin 5) power supply.

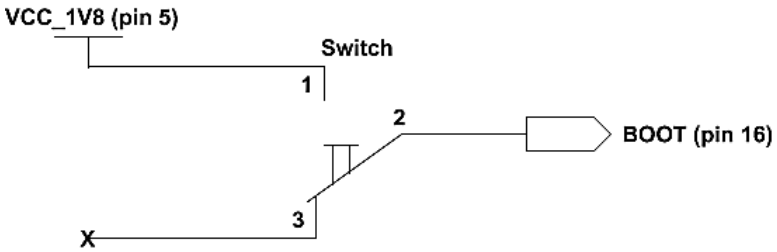


Figure 58. Example of BOOT Pin Implementation

5.4. BAT-RTC (Backup Battery)

The Q2687 Refreshed embedded module provides an input/output to connect a Real Time Clock power supply.

This pin is used as a back-up power supply for the internal Real Time Clock. The RTC is supported by the Q2687 Refreshed embedded module when VBATT is available, but a backup power supply is needed to save date and time when VBATT is switched off (VBATT = 0V).

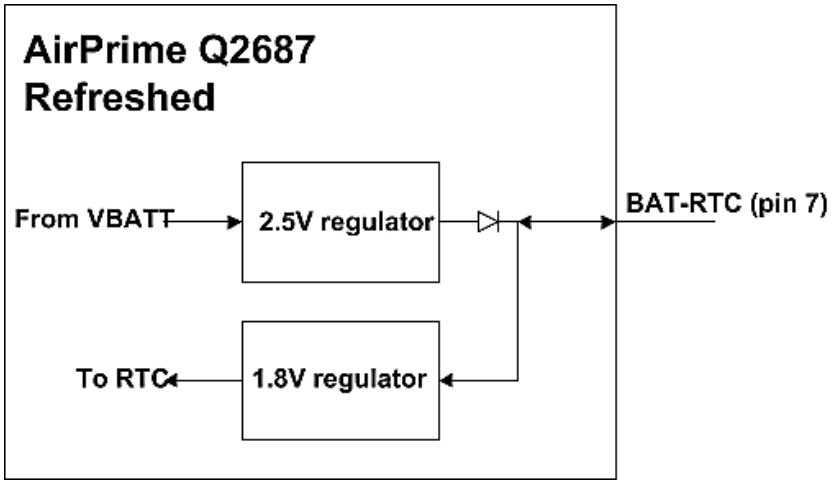


Figure 59. Real Time Clock Power Supply

If RTC is not used, this pin can be left open. If VBATT is available, the back-up battery can be charged by the internal 2.5V power supply regulator.

The back-up power supply can be provided by any of the following:

- A super capacitor
- A non-rechargeable battery
- A rechargeable battery

5.4.1. Pin Description

Refer to the following table for the pin description of the BAT-RTC interface.

Table 60. BAT-RTC Pin Description

Pin Number	Signal	I/O	I/O Type	Description
7	BAT-RTC	I/O	Supply	RTC Back-up supply

5.4.2. Electrical Characteristics

Refer to the following table for the electrical characteristics of the BAT-RTC interface.

Table 61. Electrical Characteristics of the BAT-RTC Interface (for non-ESIM modules)

Parameter	Minimum	Typical	Maximum	Unit
Input voltage	1.85		3.0	V
Input current consumption*	3.0	3.3	3.6	µA
Output voltage	2.40	2.45	2.50	V
Output current			2	mA

* Provided by an RTC back-up battery when the Q2687 Refreshed embedded module power supply is off (VBATT = 0V).

Table 62. Electrical Characteristics of the BAT-RTC Interface (for the Q26SM703RD)

Parameter	Minimum	Typical	Maximum	Unit
Input voltage	1.85	2.5	3.0	V
Input current consumption*		8	15	µA
Output voltage		2.45		V
Output current**			5	mA

* Provided by an RTC back-up battery when the Q2687 Refreshed ESIM (Q26SM703RD) embedded module power supply is off (VBATT = 0V).

** A series resistor is to be added to limit the charging current.

5.4.3. Application

5.4.3.1. Super Capacitor

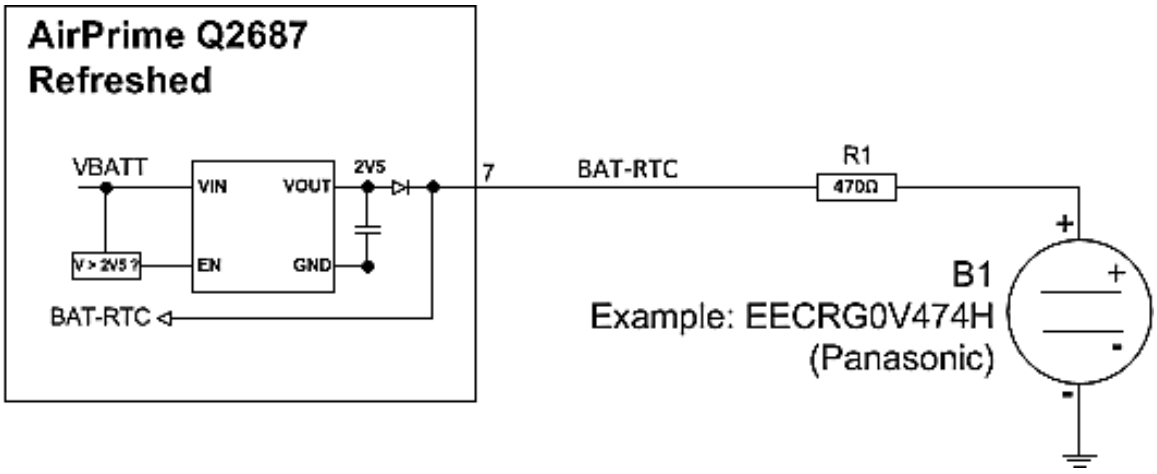


Figure 60. RTC Supplied by a Gold Capacitor

For non-ESIM versions of the Q2687 Refreshed, the typical discharge time with a 0.47Farad gold capacitor is 25 hours.

Note: The gold capacitor maximum voltage is 2.5V.

5.4.3.2. Non-Rechargeable Battery

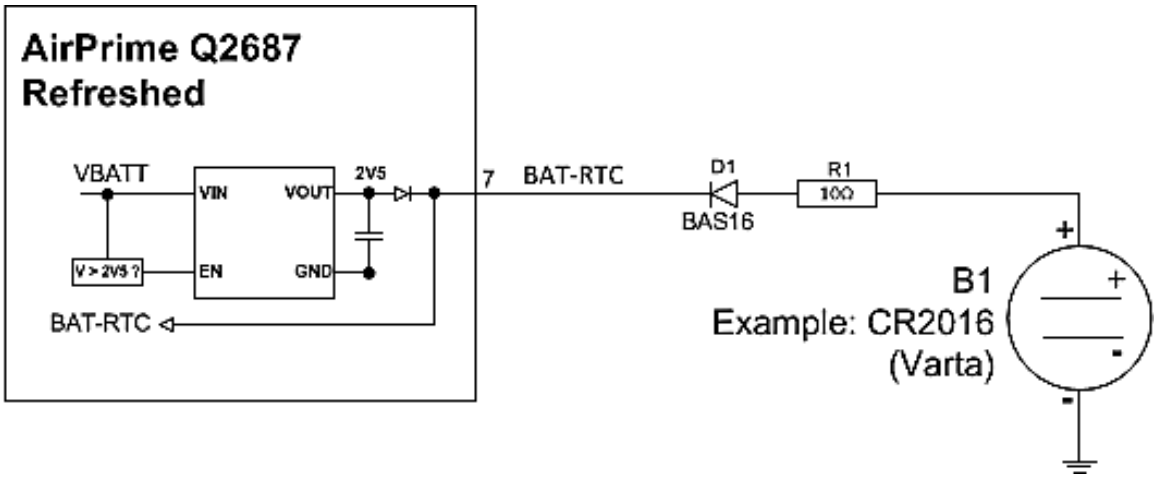


Figure 61. RTC Supplied by a Non-Rechargeable Battery

Diode D1 is mandatory to prevent the non-rechargeable battery from becoming damaged.

For non-ESIM versions of the Q2687 Refreshed, the typical discharge time with an 85mAh battery is 800H.

5.4.3.3. Rechargeable Battery

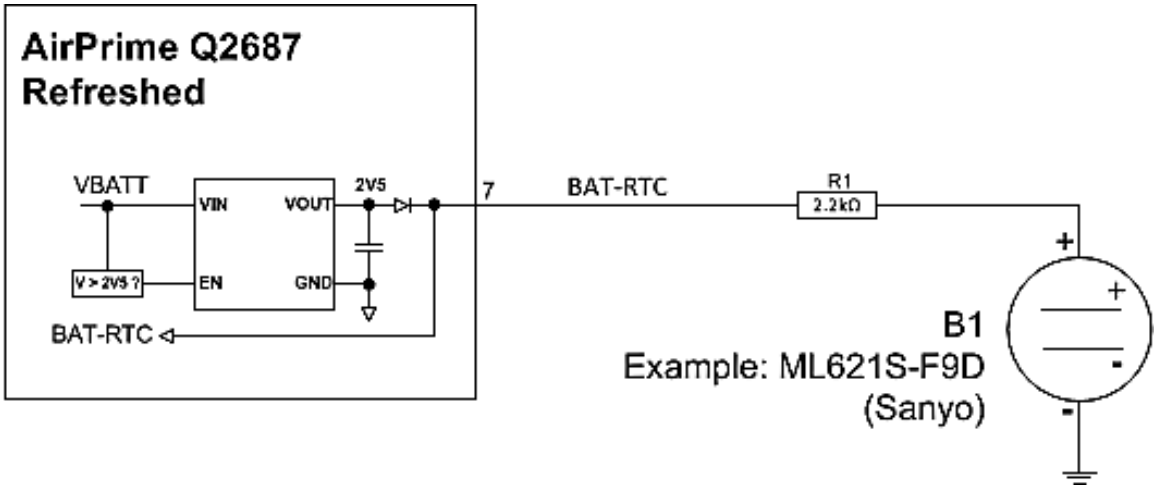


Figure 62. RTC Supplied by a Rechargeable Battery

For non-ESIM versions of the Q2687 Refreshed, the typical discharge time with a 2mAh rechargeable battery is 15H.

Caution: *Ensure that the cell voltage is lower than 2.75V before battery cell assembly to avoid damaging the Q2687 Refreshed embedded module.*

5.5. Buzzer Output

This digital output is controlled by a pulse-width modulation controller and is an open drain output. This signal may only be used in the implementation of a buzzer. The buzzer can be directly connected to this output signal and VBATT. The maximum current is 100mA (PEAK).

5.5.1. Pin Description

Refer to the following table for the pin description of the buzzer output.

Table 63. PWM/Buzzer Output Pin Description

Pin Number	Signal	I/O	I/O Type	Reset State	Multiplexed With
15	BUZZER0	O	Open drain	Z	Buzzer output

Refer to section 4.2 Electrical Information for Digital I/O for open drain, 2V8 and 1V8 voltage characteristics and reset state definitions.

5.5.2. Electrical Characteristics

Refer to the following table for the electrical characteristics of the buzzer output.

Table 64. Electrical Characteristics of the Buzzer Output

Parameter	Condition	Minimum	Maximum	Unit
$V_{OL\ on}$	Iol = 100mA		0.4	V
I_{PEAK}	VBATT = VBATTmax		100	mA
Frequency		1	50000	Hz

5.5.3. Application

The maximum peak current for this interface is 100mA and the maximum average current is 40mA. A transient voltage suppressor (TVS) diode, D1, must be added to the circuit as shown in the figure below.

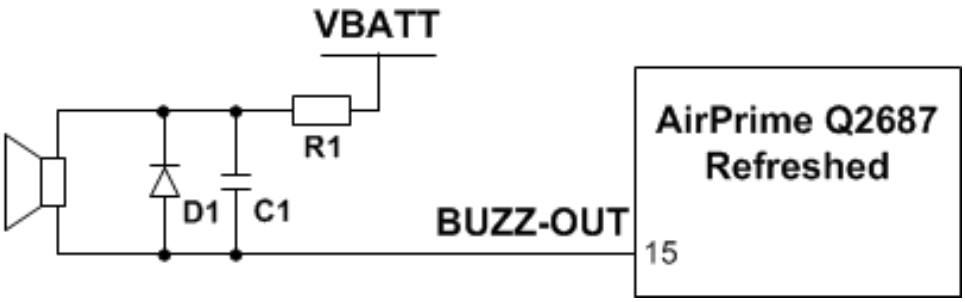


Figure 63. Example of a Buzzer Implementation

Take note of the following when implementing a buzzer:

- R1 must be chosen in order to limit the current at I_{PEAK} max
- C1 = 0 to 100nF (depending on the buzzer type)
- D1 = BAS16 (example)

The BUZZ-OUT output can also be used to drive an LED as shown in the following figure:

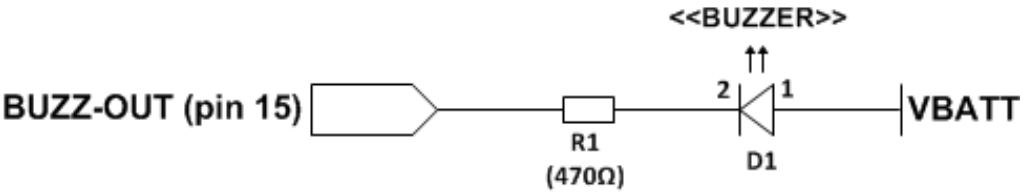


Figure 64. Example of an LED Driven by the Buzzer Output

The value of R1 should correspond with the characteristics of the LED (D1).

5.5.3.1. Recommended Characteristics

- Type :electro-magnetic
- Impedance :7Ω to 30Ω
- Sensitivity :90dB SPL minimum @ 10cm
- Current :60mA to 90mA

5.6. External Interrupt

The Q2687 Refreshed embedded module provides five external interrupt inputs with different voltages. These interrupt inputs can be activated on the:

- High to low level transition
- Low to high level transition
- Low to high and high to low level transitions

When used, the interrupt inputs must not be left open; and when they are not used, they must be configured as GPIOs.

5.6.1. Pin Description

Refer to the following table for the pin description of the external input/interrupt.

Table 65. External Interrupt Pin Description

Signal	Pin Number	I/O	I/O Type	Reset State	Description	Multiplexed With
INT0	50	I	1V8	Z	External Interrupt	GPIO3
INT1	49	I	2V8	Z	External Interrupt	GPIO25
INT2	73	I	2V8	1	External Interrupt	CT104/RXD1 / GPIO37
INT3	76	I	2V8	Z	External Interrupt	~CT108-2/DTR1 / GPIO41
INT4	30	I	1V8	0	External Interrupt	CT104/RXD2 / GPIO15

Refer to section 4.2 Electrical Information for Digital I/O for open drain, 2V8 and 1V8 voltage characteristics and reset state definitions.

5.6.2. Electrical Characteristics

Refer to the following table for the electrical characteristics of the external input/interrupt.

Table 66. Electrical Characteristics of the External Input/Interrupt

Parameter		Minimum	Maximum	Unit
INT0	V_{IL}		0.54	V
	V_{IH}	1.33		V

Parameter		Minimum	Maximum	Unit
INT1	V_{IL}		0.84	V
	V_{IH}	1.96		V
INT2	V_{IL}		0.84	V
	V_{IH}	1.96		V
INT3	V_{IL}		0.84	V
	V_{IH}	1.96		V
INT4	V_{IL}		0.54	V
	V_{IH}	1.33		V

5.6.3. Application

INT0, INT1, INT3 and INT4 are high impedance input types so it is important to set the interrupt input signals with pull-up or pull-down resistors if they are driven by an open drain, an open collector or by a switch. If the interrupt signals are driven by a push-pull transistor, then no pull-up or pull-down resistors are necessary.

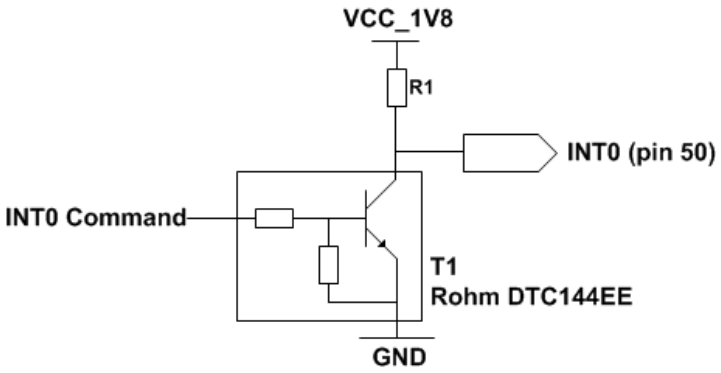


Figure 65. Example of INT0 Driven by an Open Collector

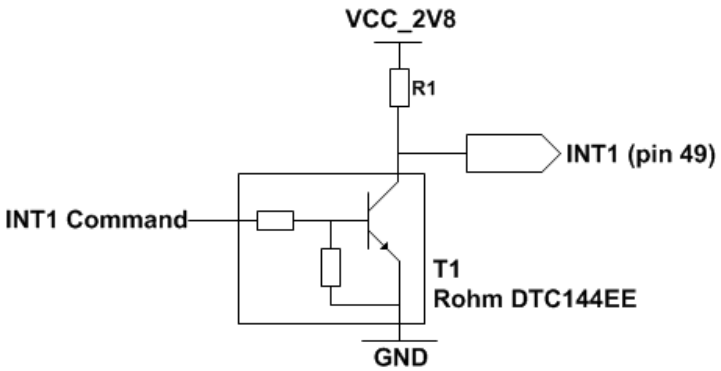


Figure 66. Example of INT1 Driven by an Open Collector

where:

- The value of R1 can be 47kΩ
- T1 can be a ROHM DTC144EE open collector transistor

5.7. VCC_2V8 and VCC_1V8 Output

These digital power supply outputs are mainly used to:

- Pull-up signals such as I/Os
- Supply the digital transistors driving LEDs
- Supply the SIMPRES signal
- Act as a voltage reference for the ADC interface AUX-ADC (VCC_2V8 only)

Each digital output has a maximum current of 15mA.

Both VCC_2V8 and VCC_1V8 are only available when the embedded module is ON.

5.7.1. Pin Description

Refer to the following table for the pin description of the VCC_2V8 and VCC_1V8 output.

Table 67. VCC_2V8 and VCC_1V8 Pin Description

Pin Number	Signal	I/O	I/O Type	Description
5	VCC_1V8	O	Supply	1.8V digital supply
10	VCC_2V8	O	Supply	2.8V digital supply

Refer to section 4.2 Electrical Information for Digital I/O for open drain, 2V8 and 1V8 voltage characteristics and reset state definitions.

5.7.2. Electrical Characteristics

Refer to the following table for the electrical characteristics of the VCC_2V8 and VCC_1V8 output signals.

Table 68. Electrical Characteristics of the VCC_2V8 and VCC_1V8 Signals

Parameter		Minimum	Typical	Maximum	Unit
VCC_2V8	Output voltage	2.74	2.8	2.86	V
	Output Current			15	mA
VCC_1V8	Output voltage	1.76	1.8	1.94	V
	Output Current			15	mA

5.8. FLASH-LED (LED0)

The FLASH-LED is the GSM activity status indicator signal of the Q2687 Refreshed embedded module and it can be used to drive an LED. This signal is an open drain output. An LED and a resistor can be directly connected between this output and VBATT.

When the Q2687 Refreshed embedded module is OFF, if 2.8V < VBATT < 3.2V and a charger is connected on the CHG-IN inputs, this output flashes (100 ms = ON; 900ms = OFF) to indicate the pre-charging phase of the battery.

When the Q2687 Refreshed embedded module is ON, this output is used to indicate the network status.

Table 69. FLASH-LED Status

Q2687 State	VBATT Status	FLASH-LED Status	Q2687 Refreshed Embedded Module Status
OFF	VBATT< 2.8V or VBATT > 3.2V (for non-ESIM modules)	OFF	OFF (no pre-charging)
	2.8V < VBATT < 3.2V (for non-ESIM modules)	Pre-charge flash LED ON for 100 ms, OFF for 900 ms	OFF; Pre-charging mode (charger must be connected on CHG-IN to activate this mode)
	VBATT< 1.2V or VBATT > 3.2V (for the Q26SM703RD)	OFF	OFF (no pre-charging)
	1.2V < VBATT < 3.2V (for the Q26SM703RD)	Pre-charge flash LED ON for 100 ms, OFF for 900 ms	OFF; Pre-charging mode (charger must be connected on CHG-IN to activate this mode)
ON	VBATT > 3.2V (3.25V for the Q26SM703RD)	Permanent	ON; not registered on the network
		Slow flash LED ON for 200 ms, OFF for 2 s	ON; registered on the network
		Quick flash LED ON for 200 ms, OFF for 600 ms	ON; registered on the network, communication in progress
		Very quick flash LED ON for 100 ms, OFF for 200 ms	ON; software downloaded is either corrupted or non-compatible ("BAD SOFTWARE")

5.8.1. Pin Description

Refer to the following table for the pin description of the FLASH-LED.

Table 70. FLASH-LED Pin Description

Pin Number	Signal	I/O	I/O Type	Reset State	Description
17	LED0	O	Open Drain Output	1 and Undefined	LED driving

Refer to section 4.2 Electrical Information for Digital I/O for open drain, 2V8 and 1V8 voltage characteristics and reset state definitions.

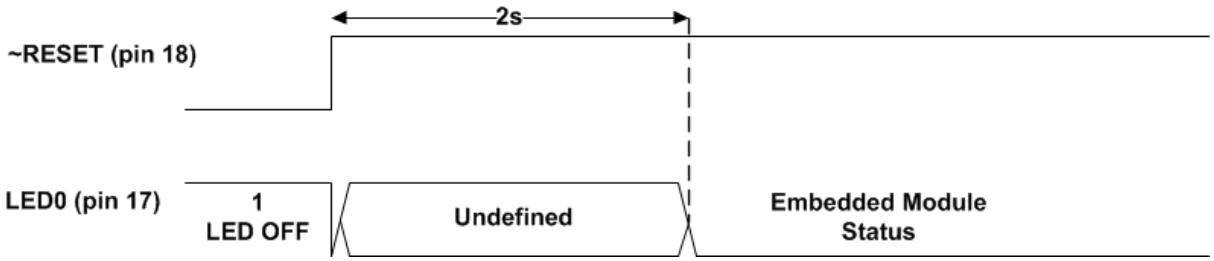


Figure 67. LED0 State During RESET and Initialization Time

LED0 state is HIGH during the RESET time and undefined during the software initialization time. During software initialization time, for a maximum of 2 seconds after RESET cancellation, the LED0 signal is toggling and does not provide the embedded module status. After the 2s period, the LED0 provides the true status of the embedded module.

5.8.2. Electrical Characteristics

Refer to the following table for the electrical characteristics of the FLASH-LED signal.

Table 71. Electrical Characteristics of the FLASH-LED Signal

Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{OL}				0.4	V
I_{OUT}				8	mA

5.8.3. Application

Figure 68. Example of FLASH-LED Implementation

R1 can be harmonized depending on the characteristics of the LED (D1).

5.9. Analog to Digital Converter

Two Analog to Digital Converter inputs, ADC1/BAT-TEMP and AUX-ADC/ADC2, are provided by the Q2687 Refreshed embedded module. These converters are 10-bit resolution ADCs ranging from 0V to 2V.

Typically, the BAT-TEMP/ADC1 input is used to monitor external temperature. This is very useful for monitoring the application temperature and can be used as an indicator to safely power OFF the application in case of overheating (for Li-Ion batteries). For more information on battery charging, refer to section 4.14 Battery Charging Interface.

The AUX-ADC/ADC2 input can be used for customer specific applications.

5.9.1. Pin Description

Refer to the following table for the pin description of the ADC.

Table 72. ADC Pin Description

Pin Number	Signal	I/O	I/O Type	Description	ADC index in AT Command AT+ADC**
20	ADC1/BAT-TEMP*	I	Analog	A/D converter	1
21	ADC2	I	Analog	A/D converter	2

* This input is reserved for the battery charging temperature sensor. For more information, refer to section 4.14 Battery Charging Interface.

** For example, to access ADC2, the ADC index is 2. Using AT command, "**AT+ADC=0,2**", the ADC2 measure expressed in analog mode will be returned. For more information about this AT command, refer to document [2] Firmware 7.43 AT Commands Manual.

5.9.2. Electrical Characteristics

Refer to the following table for the electrical characteristics of the ADC.

Table 73. Electrical Characteristics of the ADC

Parameter		Minimum	Typical	Maximum	Unit
Maximum output code			1635		LSBs
Sampling rate				138[1]	sps
Input signal range		0		2	V
INL (Integral non linearity)			15		mV
DNL (Differential non linearity)			2.5		mV
Input impedance	ADC1/BAT-TEMP		1M*		Ω
	ADC2		1M		Ω

* Internal pull-up to 2.8V

1 Sampling rate only for ADC2 and the Open AT Application Framework application

Note that ADC is calibrated on the production line to ensure the best performance from the module. Typical ADC performance is as follows:

- For input voltage in the range of 0V to 0.3V, accuracy is +/- 50mV
- For input voltage in the range of 0.3V to 2V, accuracy is +/- 70mV

5.10. Digital to Analog Converter

One Digital to Analog Converter output is provided by the Q2687 Refreshed embedded module. The converter is an 8-bit resolution DAC, ranging from 0V to 2.3V.

5.10.1. Pin Description

Refer to the following table for the pin description of the DAC.

Table 74. DAC Pin Description

Pin Number	Signal	I/O	I/O Type	Description
82	DAC0	O	Analog	D/A converter

Note: This output assumes a typical external load of 2kΩ and 50pF in parallel to GND.

5.10.2. Electrical Characteristics

Refer to the following table for the electrical characteristics of the DAC.

Table 75. Electrical Characteristics of the DAC

Parameter	Minimum	Typical	Maximum	Unit
Resolution		8		bits
Output signal range	0		2.3	V
Output voltage after reset		0		V
INL (Integral non linearity)	-5		+5	LSB
DNL (Differential non linearity)	-1		+1	LSB

6. Power Consumption

The power consumption values of the Q2687 Refreshed embedded module vary depending on the operating mode, RF band and software used (with or without Open AT Application Framework). The following power consumption values were obtained by performing measurements on Q2687 Refreshed embedded module samples at a temperature of 25°C with the assumption of a 50Ω RF output.

Three VBATT values were used to measure the power consumption of the Q2687 Refreshed Embedded Module:

- VBATT = 3.2V (3.25V for the Q26SM703RD)
- VBATT = 3.6V
- VBATT = 4.8V

The average current and the maximum current peaks were also measured for all three VBATT values.

For a more detailed description of the operating modes, refer to the appendix of document [2] Firmware 7.43 AT Commands Manual.

For more information on the consumption measurement procedure, refer to section 7 Consumption Measurement Procedure.

6.1. Power Consumption without Open AT Application Framework

The following measurement results are relevant when:

- there is no Open AT Application Framework application
- the Open AT Application Framework application is disabled
- no processing is required by an Open AT Application Framework application

Note: Power consumption performance is software related. The values listed below were based on Firmware 7.43, except for Table 76 Power Consumption Without Open AT Application Framework for non-ESIM modules; Typical Values which was based on Firmware 7.45.

$_{TX}$ means that the current peak is the RF transmission burst (Tx burst).

$_{RX}$ means that the current peak is the RF reception burst (Rx burst).

Table 76. Power Consumption Without Open AT Application Framework for non-ESIM modules; Typical Values

Operating Mode	Parameter	$I_{Average}$			I_{Peak}	Unit
		VBATT=3.2V	VBATT=3.6V	VBATT=4.8V		
ALARM Mode		10.57	11.10	12.80	N/A	µA
SLEEP Mode		0.46	0.44	0.45	1.88	mA
ACTIVE Mode		23.73	22.12	19.19	57.35	mA
SLEEP mode with telecom stack in Idle Mode *	Paging 9/Rx burst occurrence ~2s	1.95	1.86	1.67	251.30	mA
	Paging 2/Rx burst occurrence ~0,5s	5.98	5.58	4.86	266.09	mA

Operating Mode	Parameter	$I_{Average}$			I_{Peak}	Unit
		VBATT=3.2V	VBATT=3.6V	VBATT=4.8V		
ACTIVE mode with telecom stack in Idle Mode	Paging 9/Rx burst occurrence ~2s	23.87	22.30	19.28	143.86	mA
	Paging 2/Rx burst occurrence ~0,5s	24.76	23.89	20.64	143.57	mA
Peak current in GSM/GPRS Mode	850/900 MHz - PCL5/gam.3 (TX power 33dBm)	1704	1591	1548	1758.96	mA
	1800/1900 MHz - PCL0/gam.3 (TX power 30dBm)	1130	1101	1085	1212.69	mA
GSM Connected Mode (Voice)	850/900 MHz - PCL5 (TX power 33dBm)	256.4	249.3	239.9	1759.0	mA
	850/900 MHz - PCL19 (TX power 5dBm)	105.0	100.2	91.2	317.2	mA
	1800/1900 MHz - PCL0 (TX power 30dBm)	202.8	193.9	182.0	1212.7	mA
	1800/1900 MHz - PCL15 (TX power 0dBm)	101.0	96.0	86.8	282.3	mA
GPRS Transfer Mode class 10 (3Rx/2Tx)	850/900 MHz - gam.3 (TX power 30dBm)	435.2	426.2	418.0	1791.1	mA
EGPRS Transfer Mode class 10 (3Rx/2Tx)	850/900 MHz - gam.6 (TX power 24dBm)	380.7	375.6	371.7	2082.5	mA
	1800/1900 MHz - gam.5 (TX power 23dBm)	322.2	316.8	309.4	1694.9	mA

* Sleep Idle Mode consumption is dependent on the SIM card used. Some SIM cards respond faster than others; the longer the response time, the higher the consumption.

Note: The USB port must be deactivated to enter Sleep Mode.

Table 77. Power Consumption Without Open AT Application Framework for the Q26SM703RD; Typical Values

Operating Mode	Parameter	$I_{Average}$			I_{Peak}	Unit
		VBATT=3.25V	VBATT=3.6V	VBATT=4.8V		
ALARM Mode		16.6	17.6	21.0	N/A	µA
SLEEP Mode		0.49	0.49	0.49	59	mA
ACTIVE Mode		49.6	45.5	36.1	68	mA
SLEEP mode with telecom stack in Idle Mode	Paging 9/Rx burst occurrence ~2s	2.09	1.97	1.75	296	mA
	Paging 2/Rx burst occurrence ~0,5s	6.12	5.72	4.94	309	mA

Operating Mode	Parameter	$I_{Average}$			I_{Peak}	Unit
		VBATT=3.25V	VBATT=3.6V	VBATT=4.8V		
ACTIVE mode with telecom stack in Idle Mode	Paging 9/Rx burst occurrence ~2s	24.1	22.8	19.7	168	mA
	Paging 2/Rx burst occurrence ~0,5s	26.5	23.6	20.5	146	mA

Note: The USB port must be deactivated to enter Sleep Mode.

6.2. Power Consumption with Open AT Application Framework

The following consumption results were measured during the Dhrystone application run.

Note: Power consumption performance is software related. The values listed in the tables below were based on Firmware 7.43.

$_{TX}$ means that the current peak is the RF transmission burst (Tx burst).

$_{RX}$ means that the current peak is the RF reception burst (Rx burst).

Table 78. Power Consumption With the Application CPU @ 26MHz, Typical Values

Operating Mode	Parameter	$I_{Average}$			I_{Peak}	Unit
		VBATT=3.2V	VBATT=3.6V	VBATT=4.8V		
ALARM Mode		N/A			N/A	µA
SLEEP Mode		N/A			N/A	mA
ACTIVE Mode		45.4	41.5	33.9	89.7	mA
SLEEP mode with telecom stack in Idle Mode *	Paging 9/Rx burst occurrence ~2s	N/A			N/A	mA
	Paging 2/Rx burst occurrence ~0,5s	N/A			N/A	mA
ACTIVE mode with telecom stack in Idle Mode	Paging 9/Rx burst occurrence ~2s	44.3	40.5	33.1	144	mA
	Paging 2/Rx burst occurrence ~0,5s	45.1	41.3	33.9	146	mA
Peak current in GSM/GPRS Mode	850/900 MHz - PCL5/gam.3 (TX power 33dBm)	1727	1608	1559	1727	mA
	1800/1900 MHz - PCL0/gam.3 (TX power 30dBm)	1138	1108	1095	1138	mA

Operating Mode	Parameter	$I_{Average}$			I_{Peak}	Unit
		VBATT=3.2V	VBATT=3.6V	VBATT=4.8V		
GSM Connected Mode (Voice)	850/900 MHz - PCL5 (TX power 33dBm)	266	246	232	1719	mA
	850/900 MHz - PCL19 (TX power 5dBm)	100	95	87	301	mA
	1800/1900 MHz - PCL0 (TX power 30dBm)	196	189	180	1128	mA
	1800/1900 MHz - PCL15 (TX power 0dBm)	96	91	83	273	mA
GPRS Transfer Mode class 10 (3Rx/2Tx)	850/900 MHz - gam.3 (TX power 30dBm)	457	426	408	1727	mA
EGPRS Transfer Mode class 10 (3Rx/2Tx)	850/900 MHz - gam.6 (TX power 24dBm)	321	320	328	1398	mA
	1800/1900 MHz - gam.5 (TX power 23dBm)	270	269	270	1081	mA

Note: The USB port must be deactivated to enter Sleep Mode.

Table 79. Power Consumption With the Application CPU @ 104MHz, Typical Values

Operating Mode	Parameter	$I_{Average}$			I_{Peak}	Unit
		VBATT=3.2V	VBATT=3.6V	VBATT=4.8V		
ALARM Mode		N/A			N/A	µA
SLEEP Mode		N/A			N/A	mA
ACTIVE Mode		82.6	74.5	58.8	101.8	mA
SLEEP mode with telecom stack in Idle Mode *	Paging 9/Rx burst occurrence ~2s	N/A			N/A	mA
	Paging 2/Rx burst occurrence ~0,5s	N/A			N/A	mA
ACTIVE mode with telecom stack in Idle Mode	Paging 9/Rx burst occurrence ~2s	81.4	73.4	57.7	176	mA
	Paging 2/Rx burst occurrence ~0,5s	82.1	74.1	58.5	176	mA
Peak current in GSM/GPRS Mode	850/900 MHz - PCL5/gam.3 (TX power 33dBm)	1764	1650	1590	1764	mA
	1800/1900 MHz - PCL0/gam.3 (TX power 30dBm)	1178	1141	1121	1178	mA

Operating Mode	Parameter	$I_{Average}$			I_{Peak}	Unit
		VBATT=3.2V	VBATT=3.6V	VBATT=4.8V		
GSM Connected Mode (Voice)	850/900 MHz - PCL5 (TX power 33dBm)	301	279	257	1763	mA
	850/900 MHz - PCL19 (TX power 5dBm)	135	127	111	344	mA
	1800/1900 MHz - PCL0 (TX power 30dBm)	232	221	204	1178	mA
	1800/1900 MHz - PCL15 (TX power 0dBm)	131	122	107	310	mA
GPRS Transfer Mode class 10 (3Rx/2Tx)	850/900 MHz - gam.3 (TX power 30dBm)	491	459	432	1764	mA
EGPRS Transfer Mode class 10 (3Rx/2Tx)	850/900 MHz - gam.6 (TX power 24dBm)	352	351	354	1423	mA
	1800/1900 MHz - gam.5 (TX power 23dBm)	303	298	293	1109	mA

Note: The USB port must be deactivated to enter Sleep Mode.

7. Consumption Measurement Procedure

This chapter describes the consumption measurement procedure used to obtain the Q2687 Refreshed Embedded Module consumption specification.

7.1. Hardware Configuration

Consumption results are highly dependent on the hardware configuration used during measurement and this section describes the hardware configuration settings that must be used to obtain optimum consumption measurements.

The following hardware configuration includes both the measurement equipment used and the Q2687 Refreshed embedded module on the Q26 Series Development Kit board v3.

7.1.1. Equipment Used

Four devices were used to perform consumption measurement:

- Network Analyzer
- Current Measuring Power Supply
- Standalone Power Supply
- Computer, to control the embedded module and to save measurement data

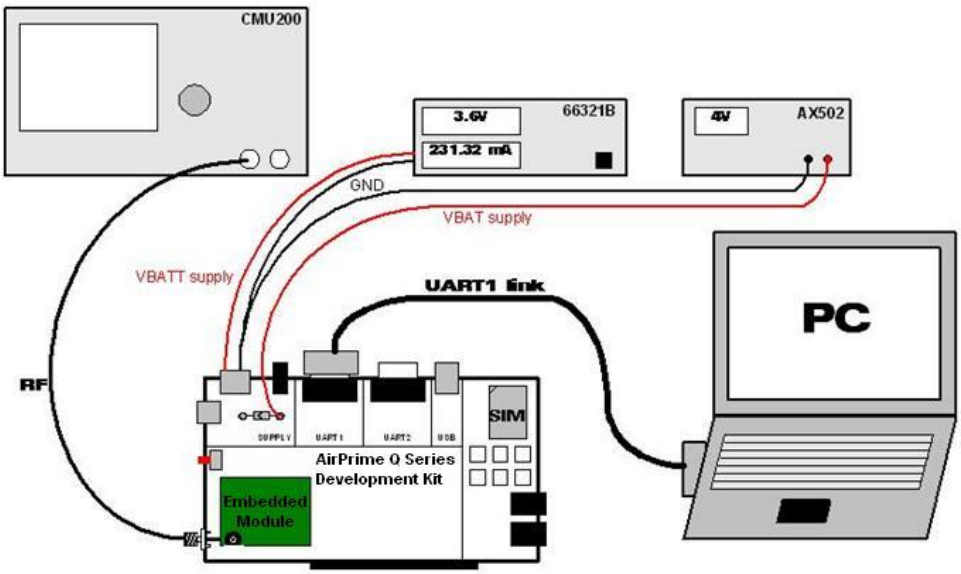


Figure 69. Typical Hardware Configuration

The **network analyzer** is a **CMU 200** from **Rhode & Schwartz**. This analyzer offers all GSM/GPRS/EGPRS network configurations required and allows a wide range of network configurations to be set.

The **AX502** standalone power supply is used to supply all development kit board components except the embedded module. The goal is to separate the development kit board consumption from the embedded module consumption which is measured by the other power supply, the **66321B** “current measuring power supply”.

The “current measuring power supply” is also connected and controlled by the computer (GPIB control not shown in the previous figure).

A SIM must be inserted in the Q26 Series Development Kit during all consumption measurements.

The following table lists the recommended equipments to use for the consumption measurement.

Table 80. Recommended Equipments

Device	Manufacturer	Reference	Notes
Network analyzer	Rhode & Schwartz	CMU 200	Quad Band GSM/DCS/GPRS/EGPRS
Current measuring power supply	Agilent	66321B	Used for VBATT
Standalone power supply	Metrix	AX502	Used for VBAT

7.1.2. Q26 Series Development Kit Board v3

The Q26 Series Development Kit Board v3 is used as a basis for the Q2687 Refreshed embedded module measurements using several settings. For more information about these settings, refer to document [8] AirPrime Q26 Series Development Kit User Guide.

The Q26 Series Development Kit board is powered by the standalone power supply VBAT; while the Q2687 Refreshed embedded module is powered by the current measuring power supply, VBATT. Because of this, the link between VBATT and VBAT (J103) must be opened (by removing the solder at the top of the board in the SUPPLY area).

- VBATT is powered by the current measuring power supply **66321B**
- VBAT is powered by the standalone power supply **AX502**

Also take note of the following additional configuration/settings:

- The R100 resistor (around the BAT-TEMP connector) must be removed.
- The UART2 link is not used; therefore, J501, J502, J503 and J504 must be opened (by removing the solder).
- UART2 R502 must be removed; R507 must be soldered with a 0Ω resistor.
- The USB link is not used; therefore, J801, J802 and J803 must be opened (by removing the solder).
- UART1 R408 must be removed; R406 must be soldered with a 0Ω resistor.
- The standalone power supply, VBAT, may be set to 4V.

The goal of the settings listed above is to eliminate all bias current from VBATT and to supply the entire board (except the embedded module) using only VBAT.

Note: When measuring the current consumption in alarm mode, it is necessary to remove D100, D103 and R103 from the Q26 Series Development Kit in order to have accurate results.

7.1.3. SIM Cards

Consumption measurement may be performed with either 3-Volt or 1.8-Volt SIM cards. However, all specified consumption values are for a 3-Volt SIM card.

Note: The SIM card's voltage is supplied by the embedded module's power supply. Consumption measurement results may vary depending on the SIM card used.

7.2. Software Configuration

The software configuration for the equipment(s) used and the Q2687 Refreshed embedded module settings are presented in the following sub-sections.

7.2.1. Embedded Module Configuration

The software configuration for the embedded module is done by selecting the operating mode to use in performing the measurement.

A description of the operating modes and the procedures used to change the operating mode are given in the appendix of document [2] Firmware 7.43 AT Commands Manual.

The available operating modes in the Q2687 Refreshed embedded module are as follows:

- Alarm Mode
- Active Idle Mode
- Sleep Idle Mode
- Active Mode
- Sleep Mode
- Connected Mode
- Transfer Mode class 8 (4Rx/1Tx)
- Transfer Mode class 10 (3Rx/2Tx)

Note: The USB port must be deactivated to enter Sleep Mode.

7.2.2. Equipment Configuration

The network analyzer is set according to the embedded module's operating mode.

Paging during Idle modes, TX burst power, RF band and GSM/DCS/GPRS/EGPRS may be selected on the network analyzer.

Refer to the following table for the network analyzer configuration according to operating mode.

Table 81. Operating Mode Configuration

Operating Mode	Network Analyzer Configuration
ALARM Mode	N/A
SLEEP Mode	N/A
ACTIVE Mode	N/A
SLEEP mode with telecom stack in Idle Mode	Paging 9/Rx burst occurrence ~2s
	Paging 2/Rx burst occurrence ~0,5s

Operating Mode	Network Analyzer Configuration
ACTIVE mode with telecom stack in Idle Mode	Paging 9/Rx burst occurrence ~2s
	Paging 2/Rx burst occurrence ~0,5s
Peak current in GSM/GPRS Mode	850/900 MHz - PCL5/gam.3 (TX power 33dBm)
	1800/1900 MHz - PCL0/gam.3 (TX power 30dBm)
GSM Connected Mode (Voice)	850/900 MHz - PCL5 (TX power 33dBm)
	850/900 MHz - PCL19 (TX power 5dBm)
	1800/1900 MHz - PCL0 (TX power 30dBm)
	1800/1900 MHz - PCL15 (TX power 0dBm)
GPRS Transfer Mode class 10 (3Rx/2Tx)	850/900 MHz - gam.3 (TX power 30dBm)
EGPRS Transfer Mode class 10 (3Rx/2Tx)	850/900 MHz - gam.6 (TX power 24dBm)
	1800/1900 MHz - gam.5 (TX power 23dBm)

The standalone power supply, VBAT, may be set from 3.2V to 4.8V.

The current measuring power supply, VBATT, may be set from 3.2V to 4.8V according to the Q2687 Refreshed embedded module VBATT specifications.

8. Reliability Compliance and Recommended Standards

8.1. Reliability Compliance

The Q2687 Refreshed embedded module connected on a development kit board application is compliant with the following requirements.

Table 82. Standards Conformity for the Q2687 Refreshed Embedded Module

Abbreviation	Definition
IEC	International Electro technical Commission
ISO	International Organization for Standardization

8.2. Applicable Standards Listing

The table hereafter gives the basic list of standards applicable to the Q2687 Refreshed Embedded Module.

Note: References to any features can be found from these standards.

Table 83. Applicable Standards and Requirements

Document	Current Version	Title
IEC6006826	7.0	Environmental testing - Part 2.6: Test FC: Sinusoidal Vibration.
IEC60068234	73	Basic environmental testing procedures part 2: Test FD: random vibration wide band - general requirements Cancelled and replaced by **IEC60068-2-64**. For reference only.
IEC60068264	2.0	Environmental testing - part 2-64: Test FH: vibration, broadband random and guidance.
IEC60068232	2.0	Basic environmental testing procedures - part 2: Test ED: (procedure 1) (withdrawn & replaced by IEC60068-2-31).
IEC60068231	2.0	Environmental testing part 2-31: Test EC: rough handling shocks, primarily for equipment-type specimens.
IEC60068229	2.0	Basic environmental testing procedures - part 2: Test EB and guidance: bump Withdrawn and replaced by **IEC60068-2-27**. For reference only.
IEC60068227	4.0	Environmental testing - part 2-27: Test EA and guidance: shock.
IEC60068214	6.0	Environmental testing - part 2-14: Test N: change of temperature.
IEC6006822	5.0	Environmental testing - part 2-2: Test B: dry heat.
IEC6006821	6.0	Environmental testing - part 2-1: Test A: cold.
IEC60068230	3.0	Environmental testing - part 2-30: Test DB: damp heat, cyclic (12 h + 12 h cycle).
IEC6006823	69 w/A1	Basic environmental testing procedures part 2: Test CA: damp heat, steady State Withdrawn and replaced by **IEC60068-2-78**. For reference only.

Document	Current Version	Title
IEC60068278	1.0	Environmental testing part 2-78: Test CAB: damp heat, steady state.
IEC60068238	2.0	Environmental testing - part 2-38: Test Z/AD: composite temperature/humidity cyclic test.
IEC60068240	1.0 w/A1	Basic environmental testing procedures - part 2: Test Z/AM combined cold/low air pressure tests.
ISO167501	2ND	Road vehicles - environmental conditions and testing for electrical and electronic equipment - part 1: general.
ISO167502	2ND	Road vehicles - environmental conditions and testing for electrical and electronic equipment - part 2: electrical loads.
ISO167503	2ND	Road vehicles - environmental conditions and testing for electrical and electronic equipment - part 3: mechanical loads.
ISO167504	2ND	Road vehicles - environmental conditions and testing for electrical and electronic equipment - part 4: climatic loads.
IEC60529	2.1 w/COR2	Degrees of protection provided by enclosures (IP code).
IEC60068217	4.0	Basic environmental testing procedures - part 2: Test Q: sealing.
IEC60068218	2.0	Environmental testing - part 2-18: Tests - R and guidance: water.
IEC60068270	1.0	Environmental testing - part 2: tests - test XB: abrasion of markings and letterings caused by rubbing of fingers and hands.
IEC60068268	1.0	Environmental testing - part 2: tests - test l: dust and sand.
IEC60068211	3.0	Basic environmental testing procedures, part 2: test KA: salt mist.
IEC60068260	2.0	Environmental testing - part 2: Test KE: flowing mixed gas corrosion test.
IEC60068252	2.0 w/COR	Environmental testing - part 2: Test KB: salt mist, cyclic (sodium chloride solution).

8.3. Environmental Specifications

The Q2687 Refreshed embedded module is compliant with the operating classes listed in the table below. The ideal temperature range of the environment for each operating class is also specified.

Table 84. Operating Class Temperature Range

Conditions	Temperature Range
Operating / Class A	-30 °C to +70°C
Operating / Class B	-40 °C to +85°C
Storage	-40 °C to +85°C

8.3.1. Function Status Classification

The classes reported below comply with the Annex “ISO Failure Mode Severity Classification”, ISO Standard 7637, and Section 1.

Note: The word “function” as used here concerns only the function performed by the Q2687 Refreshed embedded module.

Table 85. ISO Failure Mode Severity Classification

Class	Definition
CLASS A	The Q2687 Refreshed Embedded Module remains fully functional during and after environmental exposure; and shall meet the minimum requirements of 3GPP or appropriate wireless standards.
CLASS B	The Q2687 Refreshed Embedded Module remains fully functional during and after environmental exposure; and shall exhibit the ability to establish a voice, SMS or DATA call at all times even when one or more environmental constraint exceeds the specified tolerance. Unless otherwise stated, full performance should return to normal after the excessive constraint(s) have been removed.

8.4. Reliability Prediction Model

8.4.1. Life Stress Tests

The following tests the Q2687 Refreshed embedded module's product performance.

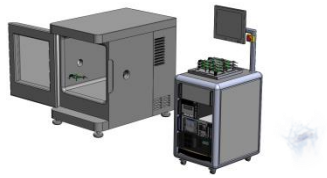
Table 86. Life Stress Tests

Designation	Condition
Performance Test PT3T° & PT 	Standard: N/A
	Special conditions: • Temperature: ▪ Class A: -30°C to +70°C ▪ Class B: -40°C to +85°C • Rate of temperature change: ± 3°C/min • Recovery time: 3 hours
	Operating conditions: Powered
	Duration: 14 days
Durability Test DT 	Standard: IEC 60068-2-2, Test Bb
	Special conditions: • Temperature: +85°C • Rate of temperature change: ± 3°C/min • Recovery time: 3 hours
	Operating conditions: Powered and Un-powered
	Duration: 156 days

8.4.2. Environmental Resistance Stress Tests

The following tests the Q2687 Refreshed embedded module's resistance to extreme temperature.

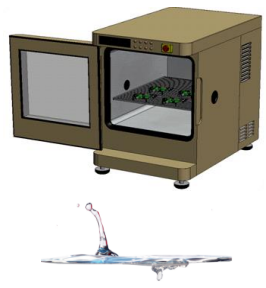
Table 87. Environmental Resistance Stress Tests

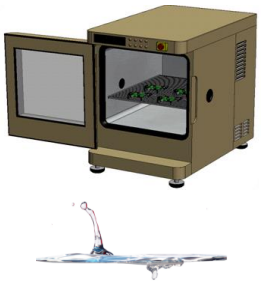
Designation	Condition
Cold Test COT 	Standard: IEC 680068-2-1, Test Ab
	Special conditions: • Temperature: -40°C • Rate of temperature change: dT/dt >= ± 3°C/min • Recovery time: 3 hours
	Operating conditions: Un-powered
	Duration: 72 hours
Resistance to Heat Test RH 	Standard: IEC 680068-2-2, Test Bb
	Special conditions: • Temperature: +85°C • Rate of temperature change: dT/dt >= ± 3°C/min • Recovery time: 3 hours
	Operating conditions: The DUT is switched ON for 1 minute and then OFF for 1 minute
	Duration: 60 days
Dry Heat Test DHT 	Standard: IEC 680068-2-2, Test Bb
	Special conditions: • Temperature: +85°C • Rate of temperature change: dT/dt >= ± 3°C/min • Recovery time: 3 hours
	Operating conditions: Un-powered
	Duration: 72 hours

8.4.3. Corrosive Resistance Stress Tests

The following tests the Q2687 Refreshed embedded module's resistance to corrosive atmosphere.

Table 88. Corrosive Resistance Stress Tests

Designation	Condition
Humidity Test HT 	Standard: IEC 60068-2-3
	Special conditions: • Temperature: +65°C • RH: 95% • Rate of temperature change: dT/dt >= ± 3°C/min • Recovery time: 3 hours
	Operating conditions: The DUT is switched ON for 5 minutes and then OFF for 15 minutes
	Duration: 10 days

Designation	Condition
Moist Heat Cyclic Test MHCT 	Standard: IEC 60068-2-30, Test Db
	Special conditions: • Upper temperature: +55 ± 2°C • Lower temperature: +25°C ± 2°C • RH: ▪ Upper temperature: 93% ▪ Lower temperature: 95% • Number of cycles: 21 (1 cycle/24 hours) • Rate of temperature change: dT/dt >= ± 3°C/min • Recovery time: 3 hours
	Operating conditions: Un-powered
	Duration: 21 days

8.4.4. Thermal Resistance Cycle Stress Tests

The following tests the Q2687 Refreshed embedded module's resistance to extreme temperature cycling.

Table 89. Thermal Resistance Cycle Stress Tests

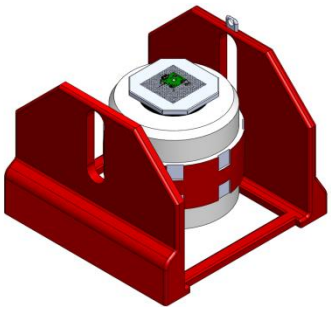
Designation	Condition
Thermal Shock Test TSKT 	Standard: IEC 60068-2-14
	Special conditions: • Upper temperature: +90°C • Lower temperature: -40°C • Rate of temperature change: 30s • Number of cycles: 200 • Duration of exposure: 30 minutes • Recovery time: 3 hours
	Operating conditions: Un-powered
	Duration: 72 hours
Temperature Change TCH 	Standard: IEC 60068-2-14, Test Nb
	Special conditions: • Upper temperature: +85°C • Lower temperature: -40°C • Rate of temperature change: dT/dt >= ± 3°C/min • Number of cycles: 400 • Duration of exposure: 30 minutes • Recovery time: 3 hours
	Operating conditions: Un-powered

8.4.5. Mechanical Resistance Stress Tests

The following tests the Q2687 Refreshed embedded module's resistance to vibrations and mechanical shocks.

Table 90. Mechanical Resistance Stress Tests

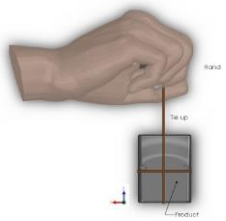
Designation	Condition
Sinusoidal Vibration Test SVT1 	Standard: IEC 60068-2-6, Test Fc
	Special conditions: • Frequency range: 10Hz to 1000Hz ▪ Displacement: ±5mm (peak) • Frequency range: 16Hz to 62Hz ▪ Acceleration: 5G • Frequency range: 62Hz to 200Hz ▪ Acceleration: 3G • Frequency range: 200Hz to 1000Hz ▪ Acceleration: 1G • Sweep rate: 1 oct/min. • Test duration: 20 cycles • Sweep directions: X, Y and Z
	Operating conditions: Un-powered
	Duration: 72 hours
Random Vibration Test RVT 	Standard: IEC 60068-2-64
	Special conditions: • Density spectrum: 0.96m^2/s3 • Frequency range: ▪ 0.1 g2/Hz at 10Hz ▪ 0.01 g2/Hz at 250Hz ▪ 0.0005 g2/Hz at 1000Hz ▪ 0.0005 g2/Hz at 2000Hz • Slope: -3dB/octave • Acceleration: 0.9gRMS • Number of axis: 3
	Operating conditions: Un-powered
	Duration: 16 hours

Designation	Condition
Mechanical Shock Test MST 	Standard: IEC 60068-2-27, Test Ea
	Special conditions: • Shock Test 1: ▪ Wave form: Half sine ▪ Peak acceleration: 30G ▪ Duration: 11ms ▪ Number of shocks: 8 per direction ▪ Number of directions: 6 (±X, ±Y, ±Z) • Shock Test 2: ▪ Wave form: Half sine ▪ Peak acceleration: 200G ▪ Duration: 3ms ▪ Number of shocks: 3 per direction ▪ Number of directions: 6 (±X, ±Y, ±Z) • Shock Test 3: ▪ Wave form: Half sine ▪ Peak acceleration: 100G ▪ Duration: 6ms ▪ Number of shocks: 3 per direction ▪ Number of directions: 6 (±X, ±Y, ±Z)
	Operating conditions: Un-powered
	Duration: 72 hours

8.4.6. Handling Resistance Stress Tests

The following tests the Q2687 Refreshed embedded module's resistance to handling malfunctions and damage.

Table 91. Handling Resistance Stress Tests

Designation	Condition
ESD Test 	Standard: IEC 1000-4-2
	Special conditions: • Contact discharges: 10 positive and 10 negative applied • Voltage: ±2kV, ±4kV, ±6kV
	Operating conditions: Powered
	Duration: 24 hours
Free Fall Test FFT 	Standard : IEC 60068-2-32, Test Ed
	Special conditions: • Drop: 2 samples for each direction • Equivalent drop height: 1m • Number of directions: 6 (±X, ±Y, ±Z) • Number of drops/face: 2
	Operating conditions: Un-powered
	Duration: 24 hours

9. Design Guidelines

This section provides general design guidelines for the Q2687 Refreshed embedded module.

9.1. General Rules and Constraints

Clock and other high frequency digital signals (e.g. serial buses) should be routed as far as possible from the Q2687 Refreshed embedded module analog signals.

If the application design makes it possible, all analog signals should be separated from digital signals by a ground line on the PCB.

Tip:	*It is recommended to avoid routing any signals under the embedded module on the application board.*

9.2. Power Supply

The power supply is one of the key issues in the design of a GSM terminal.

A weak power supply design could, in particular, affect:

- EMC performance
- The emission spectrum
- The phase error and frequency error

When designing the power supply, careful attention should be paid to the following:

- The quality of the power supply – low ripple, PFM or PSM systems should be avoided; linear regulation or PWM converters are preferred for low noise.
- The capacity to deliver high current peaks in a short time (pulsed radio emission).
- The VBATT line must support peak currents with an acceptable voltage drop which guarantees a minimal VBATT value of 3.2V (lower limit of VBATT).

For PCB design constraints related to power supply tracks, ground planes and shielding, refer to section 9.5 Routing Constraints.

9.3. Antenna

Another key issue in the design of a GSM terminal is the mechanical and electrical antenna adaptation. Sierra Wireless strongly recommends working with an antenna manufacturer either to develop an antenna adapted to the application or to adapt an existing solution to the application.

For more information on routing constraints for the RF circuit, refer to section 9.5.5 RF Circuit.

9.4. Layout/Pads Design

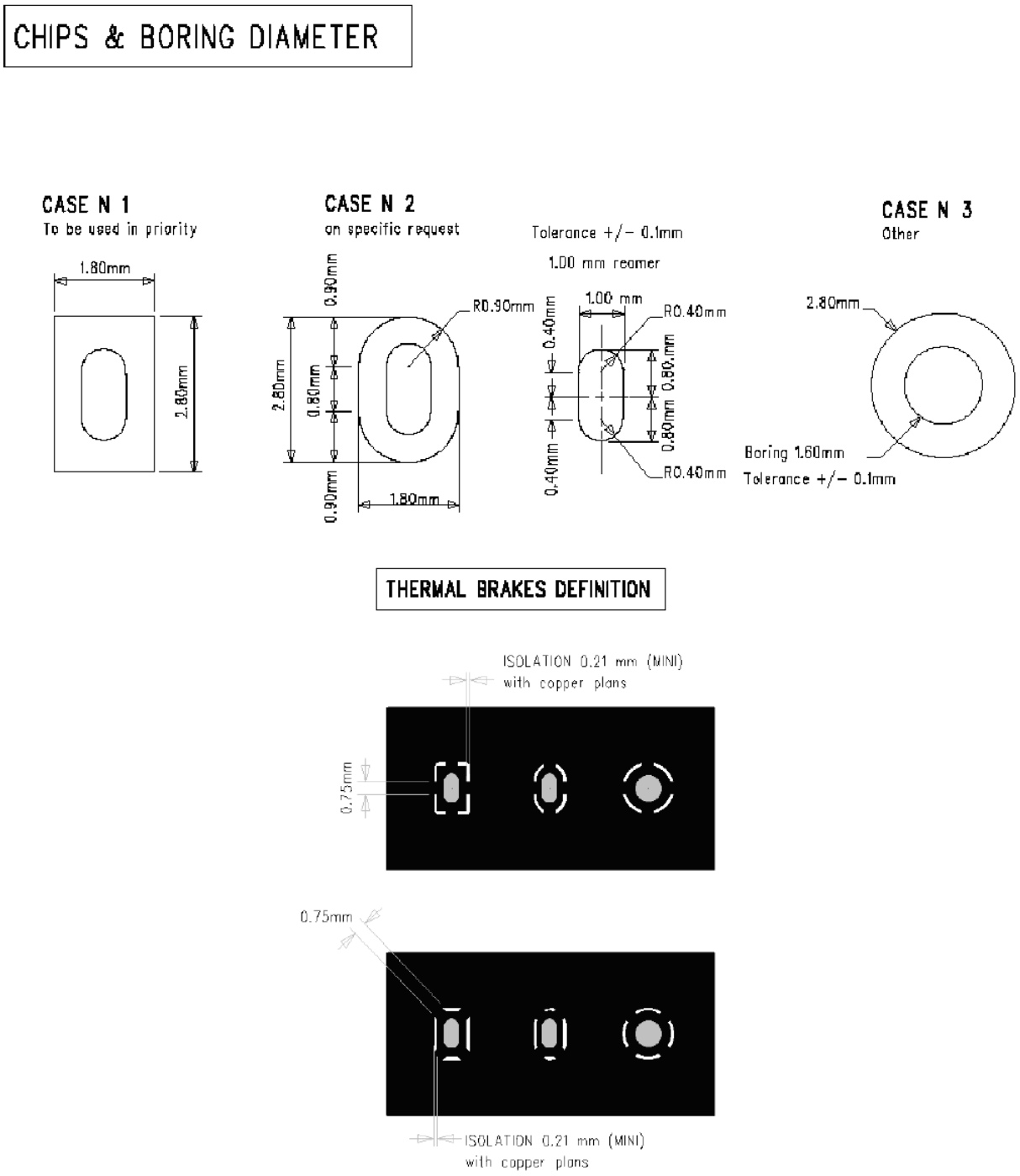


Figure 70. Layout Requirement

It is strongly recommended to use through-hole pads for the 4 legs of the Q2687 Refreshed embedded module. If the holes are connected internally to the ground plane, use thermal brakes.

9.5. Routing Constraints

9.5.1. System Connector

Refer to section 11.1 General Purpose Connector for references to the 100-pin GPC. More information is also available at http://www.naisweb.com/e/connecte/con_eng/.

9.5.2. Power Supply

Since the maximum peak current can reach 2A, Sierra Wireless strongly recommends having a large width for the layout of the power supply signal (to avoid voltage loss between the external power supply and the Q2687 Refreshed embedded module supply).

Pins 1, 2, 3 and 4 of the embedded module should be gathered in the same piece of copper, as shown in the figure below.

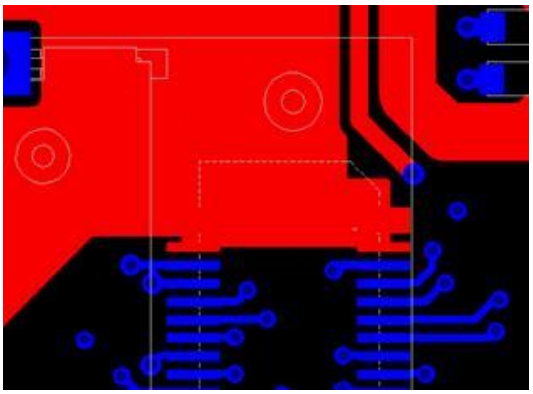


Figure 71. Power Supply Routing Example

Filtering capacitors near the Q2687 Refreshed embedded module power supply are also recommended (22µF to 100µF).

Attention should be paid to the ground track or the ground plane on the application board for the power supply which supplies the embedded module. The ground track or the ground plane on the application board must support current peaks as well as with the VBATT track.

If the ground track between the embedded module and the power supply is a ground plane, it must not be parceled out.

The routing must be done in such a way that the total line impedance could be ≤ 10mΩ @ 217Hz. This impedance must include the bias impedances.

The same care should be taken when routing the ground supply.

If these design rules are not followed, phase error (peak) and power loss could occur.

In order to test the supply tracks, a burst simulation circuit is given below. This circuit simulates burst emissions, equivalent to bursts generated when transmitting at full power.

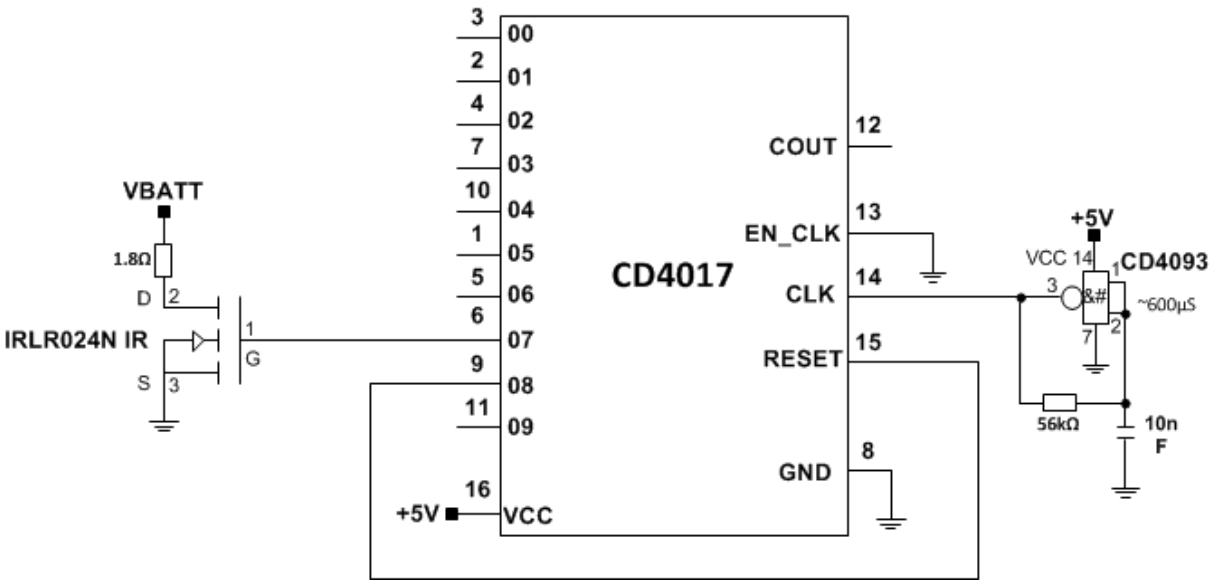


Figure 72. Burst Simulation Circuit

9.5.2.1. Ground Plane and Shielding Connection

The Q2687 Refreshed embedded module shielding case is linked to the ground. The ground has to be connected to the Q26 Series Development Kit board through a complete layer on the PCB.

A ground plane must be available on the application board to provide efficient connection to the Q2687 Refreshed embedded module shielding. The bottom side shielding of the Q2687 Refreshed embedded module is achieved through the top folded tin cover connected to the internal ground plane of the Q2687 Refreshed embedded module. This is connected through the shielding to the application ground plane.

The best shielding performance is achieved when the application ground plane is a complete layer of the application PCB. To ensure good shielding of the Q2687 Refreshed embedded module, a complete ground plane layer on the application board must be available, with no trade-offs. Connections between other ground planes should be done with bias.

Without this ground plane, external spurious TX or RX blockings could appear.

9.5.3. SIM Interface

The length of the tracks between the Q2687 Refreshed embedded module and the SIM socket should be as short as possible. Maximum recommended length is 10cm.

ESD protection is mandatory on the SIM lines if access from outside of the SIM socket is possible.

The capacitor on SIM_VCC signal (100nF) must be placed as close as possible to the DALC208SC6 component on the PCB (refer to section 4.9 SIM Interface).

9.5.4. Audio Circuit

To get better acoustic performances, the basic recommendations are as follows:

- The speaker lines (SPKxx) must be routed in parallel without any wires in between
- The microphone lines (MICxx) must be routed in parallel without any wires in between

All the filtering components (RLC) must be placed as close as possible to the associated MICxx and SPKxx pins.

9.5.5. RF Circuit

If RF signals need to be routed on the application board, the RF signals must be routed using tracks with a 50Ω characteristic impedance.

Basically, the characteristic impedance depends on the dielectric, the track width and the ground plane spacing.

In order to respect this constraint, Sierra Wireless recommends using MicroStrip or StripLine structure and computing the Tracks width with a simulation tool (like AppCad shown in the Figure below and that is available free of charge at http://www.agilent.com).

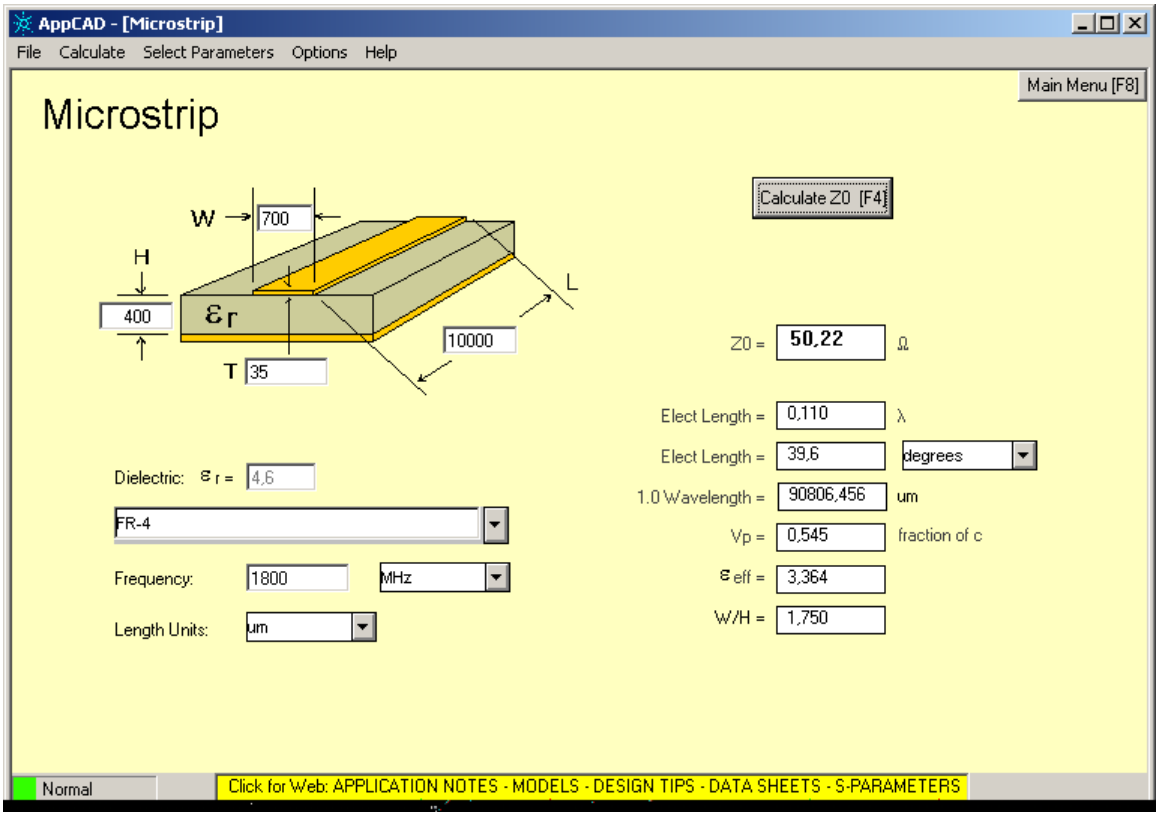


Figure 73. AppCad Screenshot for MicroStrip Design

If a multi-layered PCB is used, the RF path on the board must not cross any signal (digital, analog or supply).

If necessary, use StripLine structure and route the digital line(s) “outside” the RF structure as shown in the figure below.

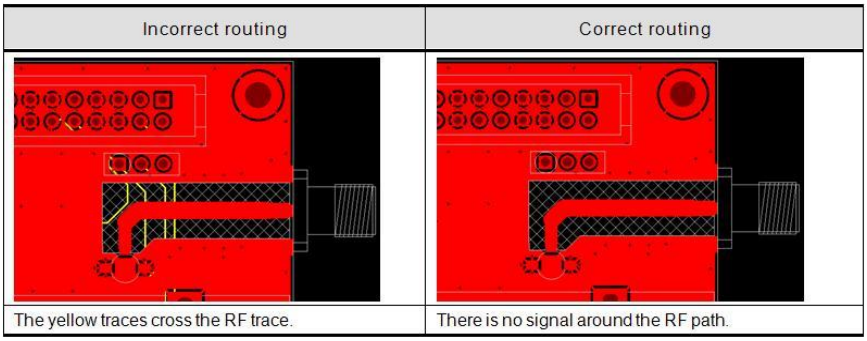


Figure 74. Routing Examples

Stripline and Coplanar design requires having a correct ground plane at both sides. Consequently, it is necessary to add some bias along the RF path.

It is recommended to use Stripline design if the RF path is fairly long (more than 3cm), since MicroStrip design is not shielded. Consequently, the RF signal (when transmitting) may interfere with neighboring electronics (AF amplifier, etc.). In the same way, the neighboring electronics (micro-controllers, etc.) may degrade the reception performances.

The GSM/GPRS connector is intended to be directly connected to a 50Ω antenna and no matching is needed.

If the GSM/GPRS/EGPRS RF connections need to be implemented on the application board (for mechanical purposes, for instance), there are four main possible connections:

- via UFL/SMA connector
- via Coaxial cable
- via Precidip connector

9.5.5.1. UFL/SMA Connector

The antenna can be connected to the Q2687 Refreshed embedded module through the UFL connector present on the embedded module by inserting the plug in the receptacle. This step is done **prior** to the Q2687 Refreshed embedded module mounting.

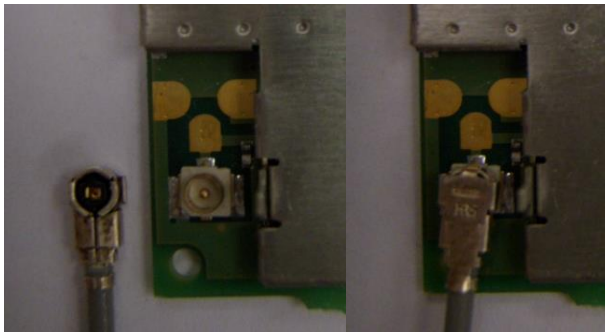


Figure 75. UFL/SMA Connector

9.5.5.2. Coaxial Cable

The antenna can also be connected to the Q2687 Refreshed embedded module through a coaxial cable. The coaxial cable is connected to both the “RF pad” (Round pad) and the “Ground pad”. It is recommended to use an **RG178** coaxial cable with the following characteristics:

- Static curvature radius :10mm
- Dynamic curvature radius :20mm

The cable must be soldered as follows:

- The shielding of the antenna cable must be soldered on the “Ground pad”.
- The antenna cable core must be soldered only once positioned in line with the “RF pad” and “Ground pad”.

Tip:	*It is highly recommended to use a template to adjust the antenna cable to the “RF pad” and “Ground pad” before soldering.*

When soldering the antenna cable, the temperature of the iron must not exceed 350°C for 3 seconds.

Note:	*The coaxial cable can be soldered in any direction. It can also be soldered on the “opposite direction”. In this case, it is necessary to solder it in a curve.*

This step is done **after** the Q2687 Refreshed embedded module mounting.

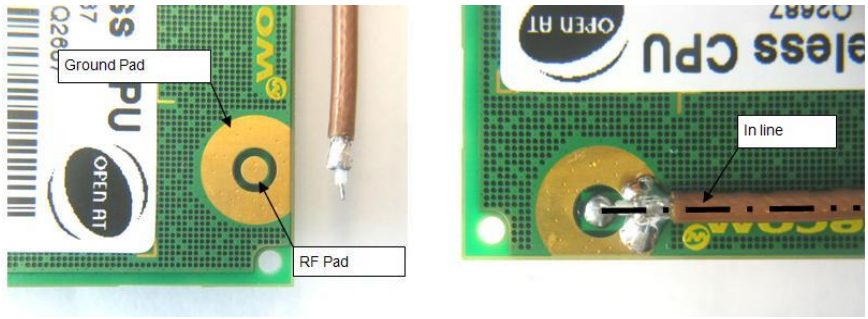


Figure 76. Antenna Connection to both RF pad and Ground pad

9.5.5.3. Precidip Connector

Lastly, the Q2687 Refreshed embedded module can also be connected through the Precidip connecter. For more information on the contact pad available on the Q2687 Refreshed embedded module, refer to section 9.4 Layout/Pads Design.

For more information on the mounting, assembling and handling of this component, contact your Precidip supplier directly (Preci-dip SA at http://www.precidip.com). Sierra Wireless cannot support customers regarding the use of this connector.

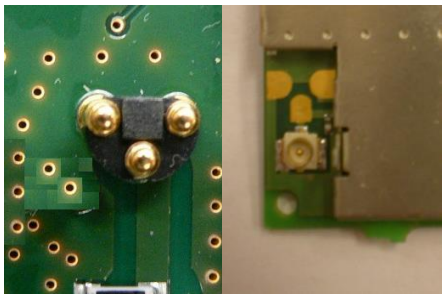


Figure 77. Precidip Connector

9.6. EMC and ESD Recommendations

EMC tests have to be performed on the application as soon as possible to detect any potential problems.

When designing, special attention should be paid to:

- Possible spurious emissions radiated by the application to the RF receiver in the receiver band

- ESD protection is mandatory on all signals which are externally accessible
  - Typically, ESD protection is mandatory for the:
    - SIM (if accessible from outside)
    - Serial link
- Length of the SIM interface lines (preferably <10cm)
- EMC protection on audio input/output (filters against 900MHz emissions)
- Biasing of the microphone inputs
- Ground plane: Sierra Wireless recommends a common ground plane for analog/digital/RF grounds
- A metallic case or plastic casing with conductive paint are recommended, except area around the antenna

Note: *The Q2687 Refreshed embedded module does not include any protection against over voltage.*

9.7. Mechanical Integration

Attention should be paid to:

- Antenna cable integration (bending, length, position, etc)
- Leads of the Embedded Module to be soldered to the Ground plane

9.8. Operating System Upgrade

The Q2687 Refreshed Embedded Module Operating System is stored in flash memory and can be easily upgraded.

Important: *In order to follow regular changes in the GPRS standard and to offer a state-of-the-art operating system, Sierra Wireless recommends that the application designed around an Embedded Module (or Embedded Module–based product) should allow easy operating system upgrades on the Embedded Module via the standard XMODEM protocol. Therefore, the application shall either allow a direct access to the Embedded Module serial link through an external connector or implement any mechanism allowing the Embedded Module operating system to be downloaded via XMODEM.*

The operating system file can be downloaded to the embedded module using the XMODEM protocol. The **AT+WDWL** command allows the downloading process to be launched. For more details, refer to document [2] Firmware 7.43 AT Commands Manual.

The serial signals required to proceed with XMODEM downloading are:

- RXD
- TXD
- RTS
- CTS
- GND

The Operating System file can also be downloaded to the embedded module using the DOTA (download over the air) feature. This feature is available with the Open AT Application Framework interface. For more details, refer to the list of documents in section 13.2 Reference Documents.

10. Embedded Testability

10.1. Serial Link Access

Direct access to UART1 serial link is very useful for:

- Testability operations
- Firmware download (for more information on firmware upgrade, refer to section 3.3 Firmware Upgrade)

To allow that access, the following serial link access designs are recommended.

10.1.1. Using an RS232 Transceiver

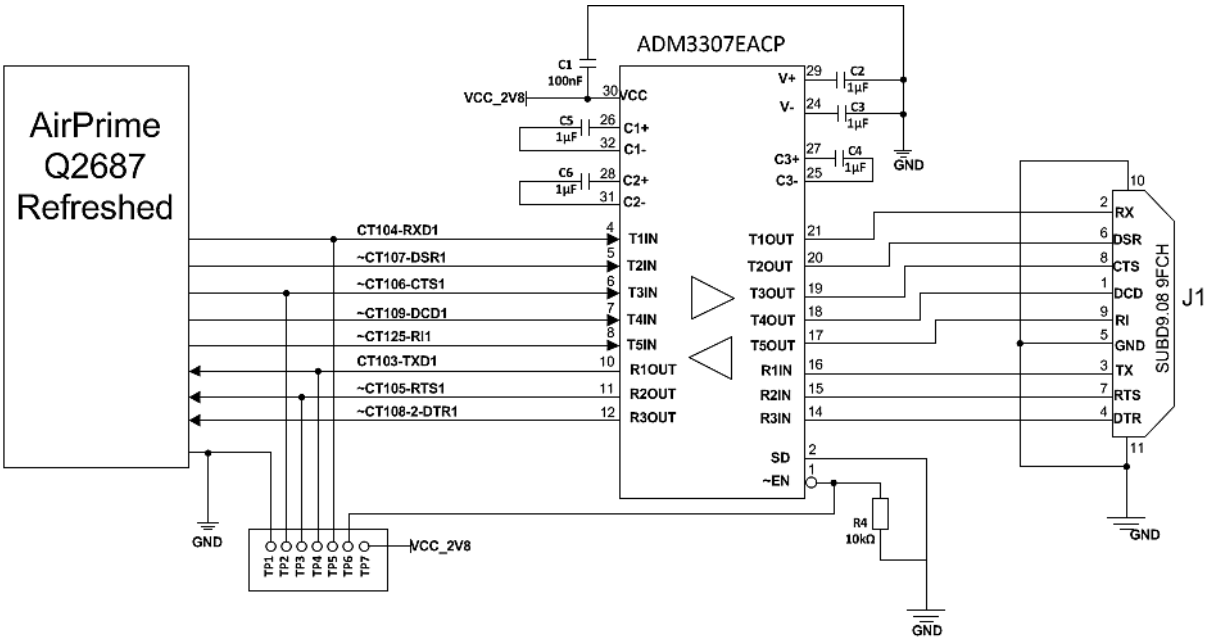


Figure 78. Main Serial Link (UART1) Debug Access with an RS232 Transceiver

When it is necessary to download firmware into the Q2687 Refreshed embedded module without going through the RS232 interface, access to the embedded module is forced via the debug connector. In such cases, input signals coming from this connector masks the input signals coming from the **ADM3307** device.

VCC_2V8 and GND are available on the debug connector to allow the powering of an external RS232 transceiver in order to communicate with a PC via a COM (COM1 or COM2) port, for example.

It is also possible to trace the signals on the serial link through the debug connector.

Note: R4 is used to have the possibility to disable the R1OUT, R2OUT and R3OUT of the ADM3307 by the enable signal (~EN) when the debug connector is used. For debug connector use, TP6 must be connected to VCC_2V8. For normal use, TP6 must be left open.

An economical solution consists of making the debug connection using 7 test points (TP) and placing these points on the edge of the application board.

Caution: *If communications on UART1 above the baud rate of 720kbps is needed, an external power supply source (3.0V typical) should be used.*

10.1.2. Using an 8-wire Design (with a Level Shifter)

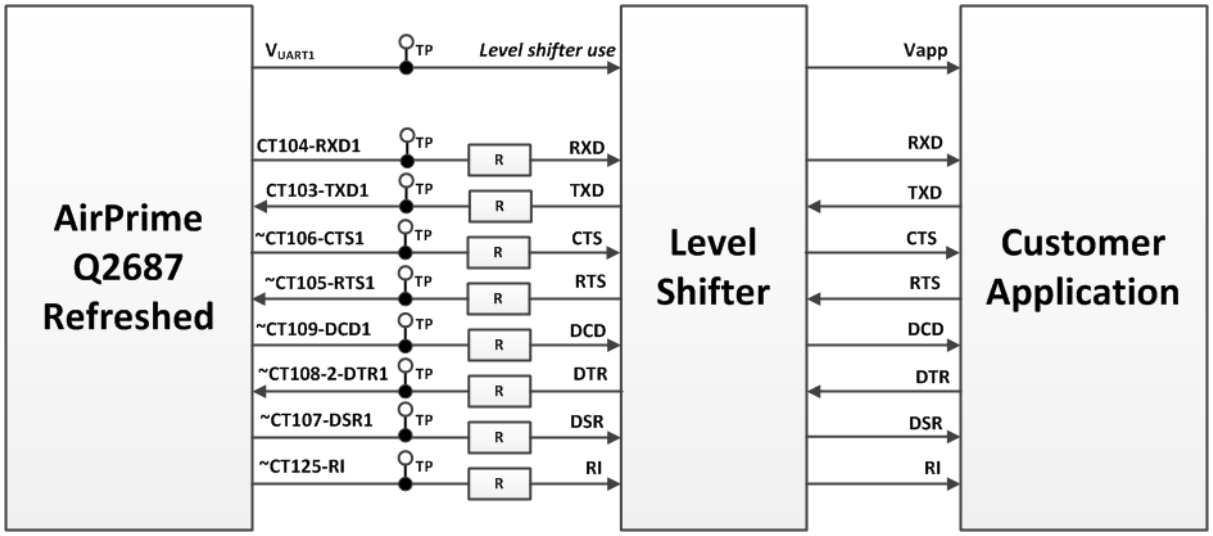


Figure 79. Main Serial Link (UART1) Debug Access using an 8-wire Design

Resistor R aims to separate the AirPrime module and the customer application or level shifter for firmware upgrade or debug. A 0 Ω resistor is usually used.

Note: *V_{UART1} may be required for the level shifter.*

10.1.3. Using a 4-wire Design (with a Level Shifter)

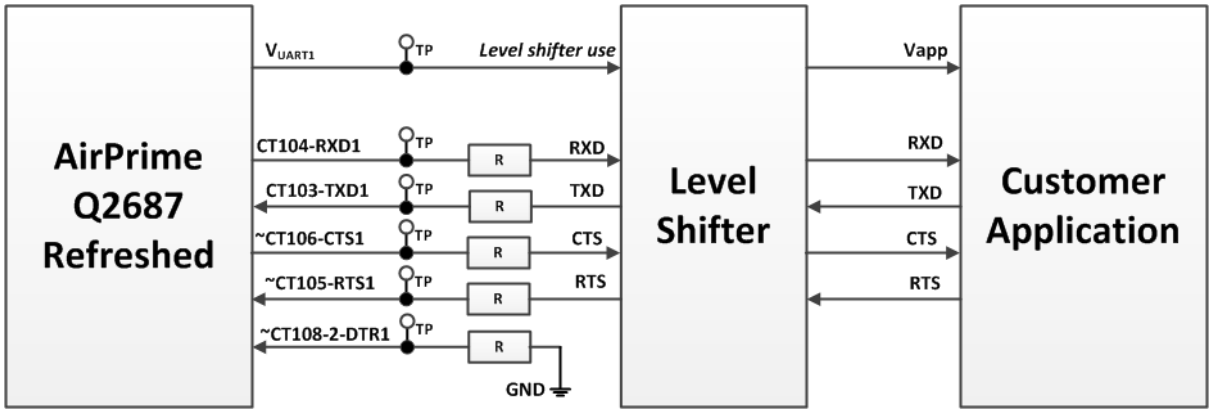


Figure 80. Main Serial Link (UART1) Debug Access using a 4-wire Design

Resistor R aims to separate the AirPrime module and the customer application or level shifter for firmware upgrade or debug. A 0 Ω resistor is usually used.

Note: *V_{UART1} may be required for the level shifter.*

10.2. RF Output Accessibility

During the integration phase of the Q2687 Refreshed embedded module, it can be helpful to connect the Q2687 Refreshed embedded module to a GSM/GPRS simulator in order to check critical RF TX parameters and power behaviour.

Although the Q2687 Refreshed embedded module has been certified, some parameters may have degraded due to some basic precautions not having been followed (poor power supply, for example). This will not affect the functionality of the product, but the product will not comply with GSM specifications.

The following TX parameters can be checked using a GSM/GSM simulator:

- Phase & Frequency Error
- Output Power and GSM Burst Time
- Output Spectrum (Modulation and Switching)

Listed below are available typical GSM/GPRS simulators:

- CMU200 from Rhode & Schwarz
- 8960 from Agilent

Because of the high prices associated with GSM/GPRS simulators and the necessary GSM know-how to perform simulations, customers can check their applications in the Sierra Wireless laboratories. Contact the Sierra Wireless support team for more information.

11. Connector and Peripheral Device References

This section contains a list of recommended manufacturers or suppliers for the peripheral devices to be used with the Q2687 Refreshed embedded module.

11.1. General Purpose Connector

The GPC is a 100-pin connector with 0.5mm pitch from the from PANASONIC Group's P5K series, with the following reference:

- AXK600347BN1

The mating connector has the following reference:

- AXK500147BN1J

The stacking height is 3.0 mm.

Sierra Wireless recommends that the **AXK500147BN1J** connector be used for applications to benefit from Sierra Wireless prices. For more information, contact Panasonic and quote the Sierra Wireless connector reference: **WM18868**.

For more information about the recommended GPC, refer to the GPC data sheets available from Panasonic (see http://www.panasonic.com/host/industrl.html).

11.2. SIM Card Reader

- ITT CANNON CCM03 series (see http://www.ittcannon.com)
- AMPHENOL C707 series (see http://www.amphenol.com)
- JAE (see http://www.jae.com)

Drawer type:

- MOLEX (see http://www.molex.com)
  - Connector: MOLEX 99228-0002
  - Holder: MOLEX 91236-0002

11.3. Microphone

The microphone selected must comply with GSM recommendations in terms of frequency response.

Possible suppliers:

- HOSIDEN (see http://www.hosiden.co.jp/)
- PANASONIC (see http://www.panasonic/com/industrial/components/)
- PEIKER

11.4. Speaker

The speaker selected must comply with GSM recommendations in terms of frequency response.

Possible suppliers:

- SANYO (see http://www.sanyo.com/industrial/components/)
- HOSIDEN (see http://www.hosiden.co.jp/)
- PRIMO (see http://www.primo.com.sg/)
- PHILIPS (see http://www.semiconductors.philips.com/)

11.5. Antenna Cable

A wide variety of cables fitted with UFL connectors is offered by HIROSE (refer to the UFL datasheet in document [7] AirPrime Q2687 Product Technical Specification for more information):

- UFL pigtails, Ex: Ref = U.FL-2LP(V)-04-A-(100)
- UFL Ref = U.FL-R-SMT
- UFL cable assemblies,
- Between series cable assemblies.

More information is also available from http://www.hirose-connectors.com/.

A coaxial cable can also be soldered on the RF pad. The following references have been certified for mounting on the Q2687 Refreshed embedded module:

- RG178
- RG316

11.6. RF board-to-board connector

The supplier for the Precidip connector is Preci-dip SA (see http://www.precidip.com), with the following reference:

- 9PM-SS-0003-02-248//R1

11.7. GSM antenna

GSM antennas and support for antenna adaptation can be obtained from manufacturers such as:

- ALLGON (see http://www.allgon.com)
- IRSCHMANN (see http://www.hirschmann.com/)
- MOTECO (see http://www.moteco.com)
- GALTRONICS (see http://www.galtronics.com)

The following table lists the contact details for other GSM antenna providers.

Table 92. Contact Information of GSM Antenna Providers

Provider	Reference	Address	Contact
Mat Equipment	MA112VX00	Z.I. La Boitardière Chemin du Roy 37400 Amboise FRANCE	Laurent.LeClainche@matequipement.com Tel: +33 2 47 30 69 70 Fax: +33 2 47 57 35 06
ProComm	MU 901/1801/UMTS-MMS + 2M FME	Europarc 121, Chemin des Bassins F-94035 CRETEIL CEDEX	Tel: +33 1 49 80 32 00 Fax: +33 1 49 80 12 54 procom@procom.fr

11.8. Buzzer

One possible Buzzer supplier is:

- SAMBU (see http://www.sambuco.co.kr)

12. Certification Compliance and Recommended Standards

12.1. Certification Compliance

The Q2687 Refreshed Embedded Module connected on a development kit board application is compliant with the following requirements.

Table 93. Standards Conformity for the Q2687 Refreshed Embedded Module

Domain	Applicable Standard
Safety standard	EN 60950-1 (ed.2006)
Health standard (EMF Exposure Evaluation)	EN 62311 (ed. 2008)
Efficient use of the radio frequency spectrum	EN 301 511 (V 9.0.2)
EMC	EN 301 489-1 (v1.8.1) EN 301 489-7 (v1.3.1)
FCC	FCC Part 15 FCC Part 22, 24
IC	RSS-132 Issue 2 RSS-133 Issue 5

12.2. Applicable Standards Listing

The table hereafter gives the basic list of standards applicable for the Q2687 Refreshed Embedded Module (2G (R99/Rel. 4)).

Note: References to any features can be found from these standards.

Table 94. Applicable Standards and Requirements for the Q2687 Refreshed Embedded Module

Document	Current Version	Title
GCF-CC	3.37.0	GSM Certification Forum - Certification Criteria
NAPRD.03	5.2	Overview of PCS Type certification review board (PTCRB) Mobile Equipment Type Certification and IMEI control
TS 51.010-1	9.0.1	3rd Generation Partnership Project; Technical Specification Group GSM/EDGE Radio Access Network; Digital cellular telecommunications system (Phase 2+); Mobile Station (MS) conformance specification; Part 1: Conformance specification
TS 51.010-2	9.0.1	3rd Generation Partnership Project; Technical Specification Group GSM/EDGE Radio Access Network; Mobile Station (MS) conformance specification; Part 2: Protocol Implementation Conformance Statement (PICS) proforma specification
TS 51.010-4	4.14.1	3rd Generation Partnership Project; Technical Specification Group GSM/EDGE Radio Access Network; Digital cellular telecommunications system (Phase 2+); Mobile Station (MS) conformance specification; Part 4: SIM Application Toolkit Conformance specification

Document	Current Version	Title
EN 301 511	9.0.2	Global System for Mobile Communications (GSM); Harmonized standard for mobile stations in the GSM 900 and DCS 1800 bands covering essential requirements under article 3.2 of the R&TTE directive (1999/5/EC)
ETSI 102.230	3.9.0	Smart cards; UICC-Terminal interface; Physical, electrical and logical test specification(Release 99)
EN 301 908-2	3.2.1	Global System for Mobile Communications (GSM); Harmonized standard for mobile stations in the GSM 900 and DCS 1800 bands covering essential requirements under article 3.2 of the R&TTE directive (1999/5/EC)

Federal Communications Commission (FCC) rules and Regulations: Power listed on the Grant is conducted for Part 22 and conducted for Part 24.

This device is to be used only for mobile and fixed applications. The antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter.

Users and installers must be provided with antenna installation instructions and transmitter operating conditions for satisfying RF exposure compliance.

Antennas used for this OEM module must not exceed a gain of 8.4dBi (850 MHz) and 3.5dBi (1900 MHz) for mobile and fixed operating configurations. This device is approved as a module to be installed in other devices.

Installed in other portable devices, the exposure condition requires a separate equipment authorization.

The licensed module has an FCC ID label on the module itself. The FCC ID label must be visible through a window or it must be visible when an access panel, door or cover is easily removed.

If not, a second label must be placed on the outside of the device that contains the following text:

Contains FCC ID: N7NQ2687

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. this device may not cause harmful interference,
2. this device must accept any interference received, including interference that may cause undesired operation.

IMPORTANT:

Manufacturers of mobile or fixed devices incorporating the Q2687 Refreshed Embedded Module are advised to:

- clarify any regulatory questions,
- have their completed product tested,
- have product approved for FCC compliance, and
- include instructions according to the above mentioned RF exposure statements in the end product user manual.

Please note that changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

13. References

13.1. Web Site Support

Check the Sierra Wireless Developer Zone at http://developer.sierrawireless.com for the latest documentation available.

Content	Web Site
General information about the Q Series Intelligent Embedded Module	http://www.sierrawireless.com/productsandservices/AirPrime/Embedded_Modules/Q_Series.aspx
Open AT Application Framework Introduction	http://www.sierrawireless.com/en/productsandservices/AirPrime/Application_Framework.aspx
Developer forum	http://forum.sierrawireless.com/

13.2. Reference Documents

For more details, several reference documents can be consulted. The Sierra Wireless documents referenced herein are provided in the Sierra Wireless documentation package; however, the general reference documents which are not Sierra Wireless owned are not provided in the documentation package.

13.2.1. Software and Firmware Documentation

[1] ADL User Guide for Open AT Framework OS 6.37

Reference: 4111704

[2] Firmware 7.43 AT Commands Manual

Reference: WM_DEV_OAT_UGD_079 (Version 14)

[3] Firmware 7.43 Customer Release Note

Reference: 4111910

13.2.2. Hardware Documentation

[4] AirPrime Q2687 Classic Product Technical Specification
Reference: WM_DEV_Q2687_PTS_001

[5] AirPrime Q26xx Process Customer Guidelines
Reference: WM_PRJ_Q2686_PTS_004

[6] AirPrime Q2687 Customer Design Guidelines
Reference: WA_DEV_Q2687_PTS_007

[7] AirPrime Q2687 Product Technical Specification
Reference: WA_ENG_Q2687_PTS_001

[8] AirPrime Q26 Series Development Kit User Guide
Reference: 4112192

[9] AirPrime Q2687 Refreshed Migration Guide
Reference: WA_DEV_Q26RD_UGD_001

[10] AirPrime Q2686 Product Technical Specification
Reference: WM_PRJ_Q2686_PTS_001

[11] AirPrime Q2686 Customer Design Guideline
Reference: WM_PRJ_Q2686_PTS_003

13.2.3. Other Related Documentation

[12] "I^2C Bus Specification", Version 2.0, Philips Semiconductor 1998

[13] ISO 7816-3 Standard

13.3. List of Abbreviations

Abbreviation	Definition
AC	Alternative Current
ADC	Analog to Digital Converter
A/D	Analog to Digital conversion
AF	Audio-Frequency
AT	ATtention (prefix for modem commands)
AUX	AUXiliary
CAN	Controller Area Network
CB	Cell Broadcast
CEP	Circular Error Probable
CLK	CLocK
CMOS	Complementary Metal Oxide Semiconductor
CS	Coding Scheme
CTS	Clear To Send
DAC	Digital to Analogue Converter

Abbreviation	Definition
dB	Decibel
DC	Direct Current
DCD	Data Carrier Detect
DCE	Data Communication Equipment
DCS	Digital Cellular System
DR	Dynamic Range
DSR	Data Set Ready
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
EDGE	Enhance Data rates for GSM Evolution
EFR	Enhanced Full Rate
E-GSM	Extended GSM
EGPRS	Enhance GPRS
EMC	ElectroMagnetic Compatibility
EMI	ElectroMagnetic Interference
EMS	Enhanced Message Service
EN	ENable
ESD	ElectroStatic Discharges
FIFO	First In First Out
FR	Full Rate
FTA	Full Type Approval
GND	GrouND
GPI	General Purpose Input
GPC	General Purpose Connector
GPIO	General Purpose Input Output
GPO	General Purpose Output
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile communications
HR	Half Rate
I/O	Input / Output
LED	Light Emitting Diode
LNA	Low Noise Amplifier
MAX	MAXimum
MIC	MICrophone
MIN	MINimum
MMS	Multimedia Message Service
MO	Mobile Originated
MT	Mobile Terminated
na	Not Applicable
NF	Noise Factor
NMEA	National Marine Electronics Association
NOM	NOMinal

Abbreviation	Definition
NTC	Negative Temperature Coefficient
PA	Power Amplifier
Pa	Pascal (for speaker sound pressure measurements)
PBCCH	Packet Broadcast Control CHannel
PC	Personal Computer
PCB	Printed Circuit Board
PDA	Personal Digital Assistant
PFM	Power Frequency Modulation
PSM	Phase Shift Modulation
PWM	Pulse Width Modulation
RAM	Random Access Memory
RF	Radio Frequency
RFI	Radio Frequency Interference
RHCP	Right Hand Circular Polarization
RI	Ring Indicator
RST	ReSeT
RTC	Real Time Clock
RTCM	Radio Technical Commission for Maritime services
RTS	Request To Send
RX	Receive
SCL	Serial CLock
SDA	Serial DAta
SIM	Subscriber Identification Module
SMS	Short Message Service
SPI	Serial Peripheral Interface
SPL	Sound Pressure Level
SPK	SPeaKer
SRAM	Static RAM
TBC	To Be Confirmed
TDMA	Time Division Multiple Access
TP	Test Point
TVS	Transient Voltage Suppressor
TX	Transmit
TYP	TYPical
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus
USSD	Unstructured Supplementary Services Data
VSWR	Voltage Standing Wave Ratio

14. Safety Recommendations (For Information Only)

For the efficient and safe operation of your GSM application based on the Q2687 Refreshed Embedded Module, please read this information carefully.

14.1. RF Safety

14.1.1. General

Your GSM terminal is based on the GSM standard for cellular technology. The GSM standard is spread all over the world. It covers Europe, Asia and some parts of America and Africa. This is the most used telecommunication standard.

Your GSM terminal is actually a low power radio transmitter and receiver. It sends out as well as receives radio frequency energy. When you use your GSM application, the cellular system which handles your calls controls both the radio frequency and the power level of your cellular modem.

14.1.2. Exposure to RF Energy

There has been some public concern about possible health effects of using GSM terminals. Although research on health effects from RF energy has focused on the current RF technology for many years, scientists have begun research regarding newer radio technologies, such as GSM. After existing research had been reviewed, and after compliance to all applicable safety standards had been tested, it has been concluded that the product was fitted for use.

If you are concerned about exposure to RF energy, there are things you can do to minimize exposure. Obviously, limiting the duration of your calls will reduce your exposure to RF energy. In addition, you can reduce RF exposure by operating your cellular terminal efficiently by following the guidelines below.

14.1.3. Efficient Terminal Operation

For your GSM terminal to operate at the lowest power level, consistent with satisfactory call quality:

If your terminal has an extendable antenna, extend it fully. Some models allow you to place a call with the antenna retracted. However your GSM terminal operates more efficiently with the antenna when it is fully extended.

Do not hold the antenna when the terminal is "IN USE". Holding the antenna affects call quality and may cause the modem to operate at a higher power level than needed.

14.1.4. Antenna Care and Replacement

Do not use the GSM terminal with a damaged antenna. If a damaged antenna comes into contact with the skin, a minor burn may result. Replace a damaged antenna immediately. You may repair antenna to yourself by following the instructions provided to you. If so, use only a manufacturer-approved antenna. Otherwise, have your antenna repaired by a qualified technician.

Buy or replace the antenna only from the approved suppliers list. Using unauthorized antennas, modifications or attachments could damage the terminal and may contravene local RF emission regulations or invalidate type approval.

14.2. General Safety

14.2.1. Driving

Check the laws and the regulations regarding the use of cellular devices in the area where you have to drive as you always have to comply with them. When using your GSM terminal while driving, please:

- give full attention to driving,
- pull off the road and park before making or answering a call if driving conditions so require.

14.2.2. Electronic Devices

Most electronic equipment, for example in hospitals and motor vehicles is shielded from RF energy. However, RF energy may affect some improperly shielded electronic equipment.

14.2.3. Vehicle Electronic Equipment

Check with your vehicle manufacturer representative to determine if any on-board electronic equipment is adequately shielded from RF energy.

14.2.4. Medical Electronic Equipment

Consult the manufacturer of any personal medical devices (such as pacemakers, hearing aids, etc...) to determine if they are adequately shielded from external RF energy.

Turn your terminal **OFF** in health care facilities when any regulations posted in the area instruct you to do so. Hospitals or health care facilities may be using RF monitoring equipment.

14.2.5. Aircraft

Turn your terminal OFF before boarding any aircraft.

- Use it on the ground only with crew permission.
- Do not use it in the air.

To prevent possible interference with aircraft systems, Federal Aviation Administration (FAA) regulations require you should have prior permission from a crew member to use your terminal while the aircraft is on the ground. To prevent interference with cellular systems, local RF regulations prohibit using your modem while airborne.

14.2.6. Children

Do not allow children to play with your GSM terminal. It is not a toy. Children could hurt themselves or others (by poking themselves or others in the eye with the antenna, for example). Children could damage the modem, or make calls that increase your modem bills.

14.2.7. Blasting Areas

To avoid interfering with blasting operations, turn your unit OFF when you are in a "blasting area" or in areas posted: "turn off two-way radio". Construction crew often uses remote control RF devices to set off explosives.

Note: *This is not applicable for final products that are ATEX compliant. For final products that are ATEX compliant, the condition of use depends on specific ATEX requirements instead.*

14.2.8. Potentially Explosive Atmospheres

Turn your terminal **OFF** when in any area with a potentially explosive atmosphere. Though it is rare, but your modem or its accessories could generate sparks. Sparks in such areas could cause an explosion or fire resulting in bodily injuries or even death.

Areas with a potentially explosive atmosphere are often, but not always, clearly marked. They include fuelling areas such as petrol stations; below decks on boats; fuel or chemical transfer or storage facilities; and areas where the air contains chemicals or particles, such as grain, dust, or metal powders.

Do not transport or store flammable gas, liquid, or explosives, in the compartment of your vehicle which contains your terminal or accessories.

Before using your terminal in a vehicle powered by liquefied petroleum gas (such as propane or butane) ensure that the vehicle complies with the relevant fire and safety regulations of the country in which the vehicle is used.

Note: *This is not applicable for final products that are ATEX compliant. For final products that are ATEX compliant, the condition of use depends on specific ATEX requirements instead.*

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