

# P8B10SB

Power MOSFETs  
100V, 8A, N-channel

### Feature

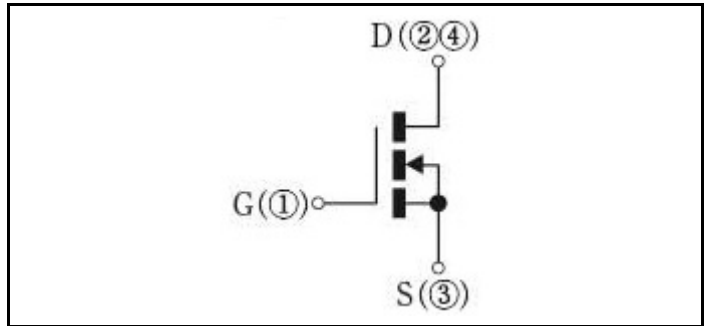
- N-channel
- SMD
- Low Ron
- 4.5V Gate Drive
- Low Capacitance
- Pb free terminal
- RoHS:Yes

### OUTLINE

Package (House Name): FB  
Package (JEDEC Code): TO-252AA



### Equivalent circuit



### Absolute Maximum Ratings (unless otherwise specified : Tc=25°C)

Item	Symbol	Conditions	Ratings	Unit
Storage temperature	T <sub>stg</sub>		-55 to 150	°C
Channel temperature	T <sub>ch</sub>		150	°C
Drain-source voltage	V <sub>DSS</sub>		100	V
Gate-source voltage	V <sub>GSS</sub>		±20	V
Continuous drain current(DC)	I <sub>D</sub>		8	A
Continuous drain current(Peak)	I <sub>DP</sub>	Pulse width 10μs, duty=1/100	24	A
Total power dissipation	P <sub>T</sub>		20	W
Single avalanche current	I <sub>AS</sub>	Starting T <sub>ch</sub> =25°C T <sub>ch</sub> ≤150°C	8	A
Single avalanche energy	E <sub>AS</sub>	Starting T <sub>ch</sub> =25°C T <sub>ch</sub> ≤150°C	6.9	mJ

\* :See the original Specifications

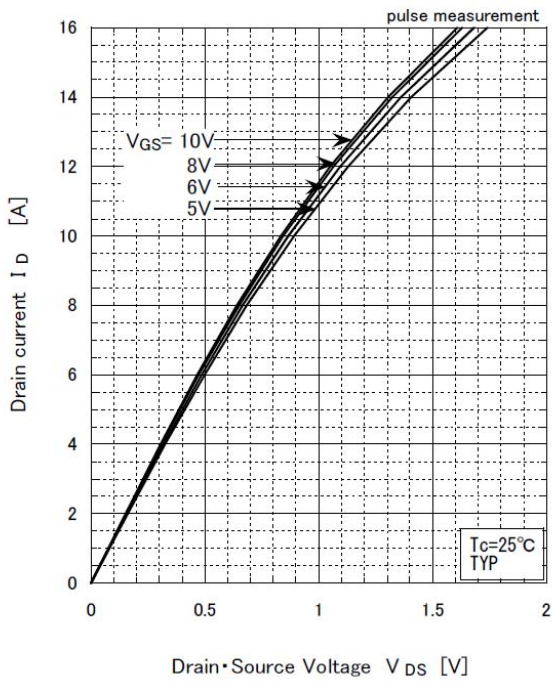
**Electrical Characteristics** (unless otherwise specified : Tc=25°C)

Item	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Drain-Source breakdown voltage	$V_{(BR)DSS}$	ID=1mA, VGS=0V	100			V
Zero gate voltage drain current	$I_{DSS}$	VDS=100V, VGS=0V			1	μA
Gate-source leakage current	$I_{GSS}$	VGS=±20V, VDS=0V			±10	μA
Forward transconductance	$g_{fs}$	ID=4A, VDS=10V	4			S
Static drain-source on-state resistance	$R_{DS(ON)}$	ID=4A, VGS=10V		0.075	0.094	Ω
Static drain-source on-state resistance	$R_{DS(ON)}$	ID=4A, VGS=4.5V		0.081	0.108	Ω
Gate threshold voltage	$V_{th}$	ID=1mA, VDS=10V	1.5	2	2.5	V
Source-drain diode forward voltage	$V_{SD}$	IS=8A, VGS=0V			1.5	V
Thermal resistance	$R_{th(j-c)}$	Junction to case			6.28	°C/W
Total gate charge	$Q_g$	VDD=80V, VGS=10V, ID=8A		16.5		nC
Gate to source charge	$Q_{gs}$	VDD=80V, VGS=10V, ID=8A		4.2		nC
Gate to drain charge	$Q_{gd}$	VDD=80V, VGS=10V, ID=8A		3.8		nC
Input capacitance	$C_{iss}$	VDS=25V, VGS=0V, f=1MHz		665		pF
Reverse transfer capacitance	$C_{rss}$	VDS=25V, VGS=0V, f=1MHz		26		pF
Output capacitance	$C_{oss}$	VDS=25V, VGS=0V, f=1MHz		64		pF
Turn-on delay time	$t_{d(on)}$	ID=4A, RL=12.5Ω, VDD=50V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		4.5		ns
Rise time	$t_r$	ID=4A, RL=12.5Ω, VDD=50V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		5.5		ns
Turn-off delay time	$t_{d(off)}$	ID=4A, RL=12.5Ω, VDD=50V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		14.5		ns
Fall time	$t_f$	ID=4A, RL=12.5Ω, VDD=50V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		4.5		ns
Diode reverse recovery time	$t_{rr}$	IF=8A, VGS=0V, di/dt=100A/μs		49		ns
Diode reverse recovery charge	$Q_{rr}$	IF=8A, VGS=0V, di/dt=100A/μs		78		nC

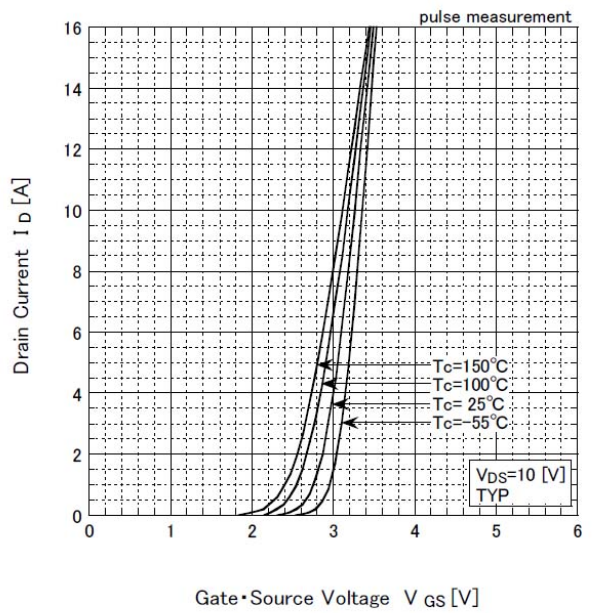
\* : See the original Specifications

# CHARACTERISTIC DIAGRAMS

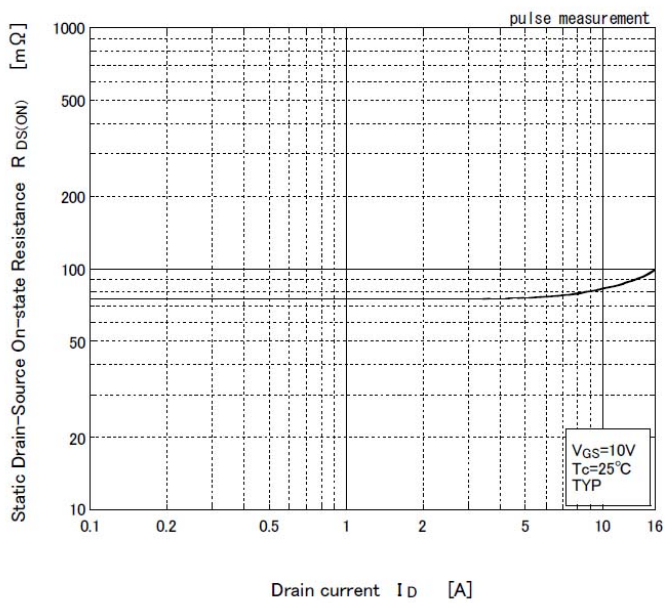
Typical Output Characteristics



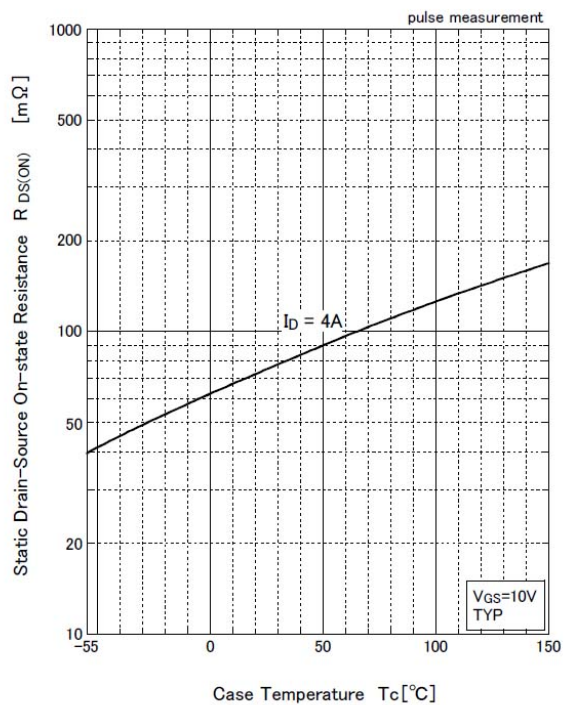
Transfer Characteristics

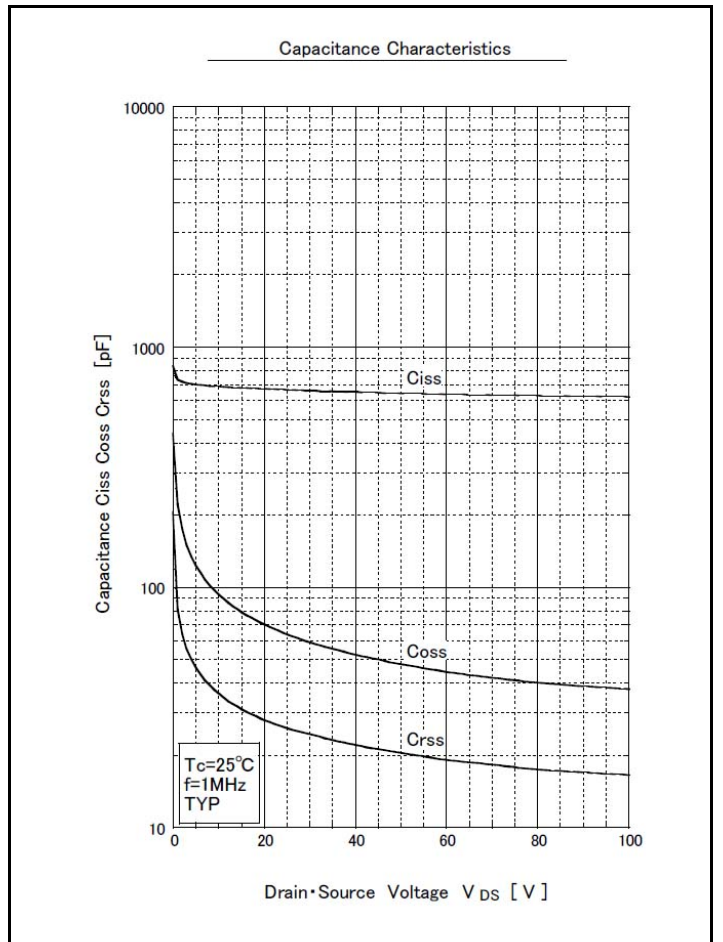
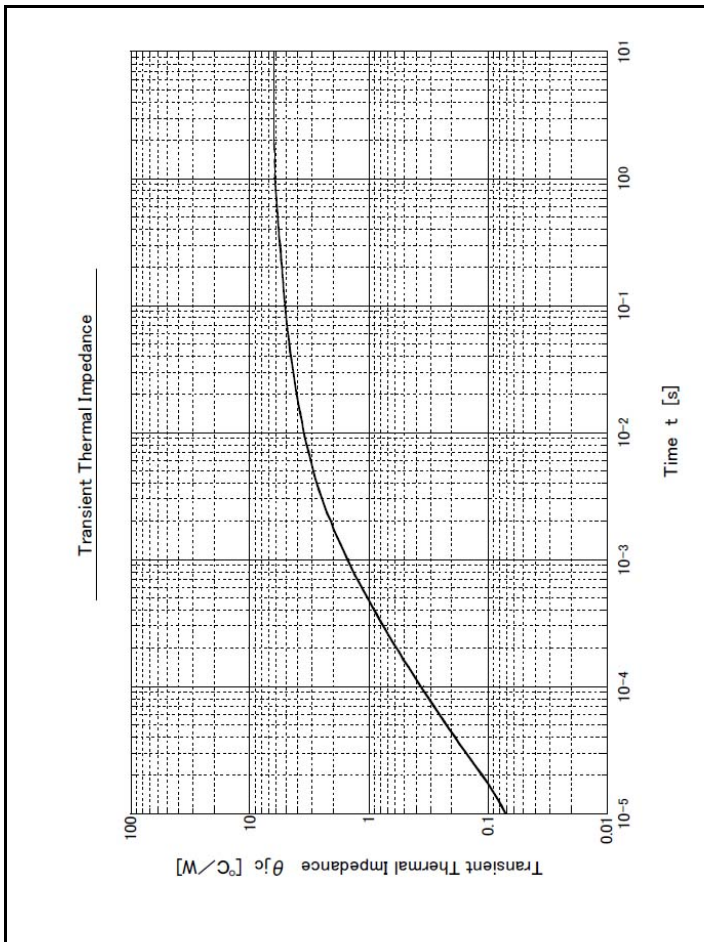
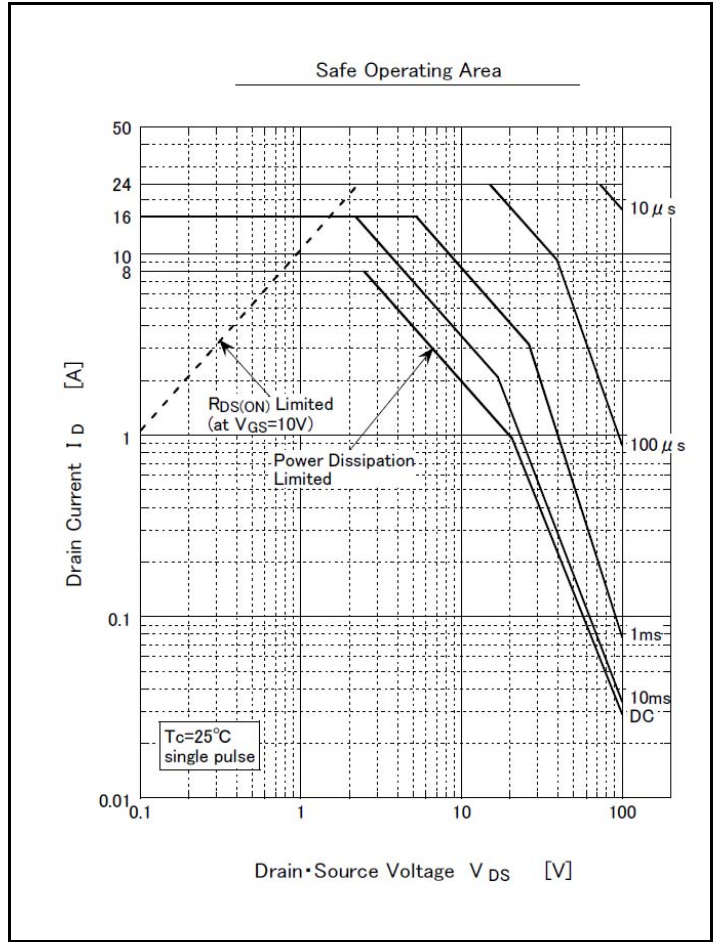
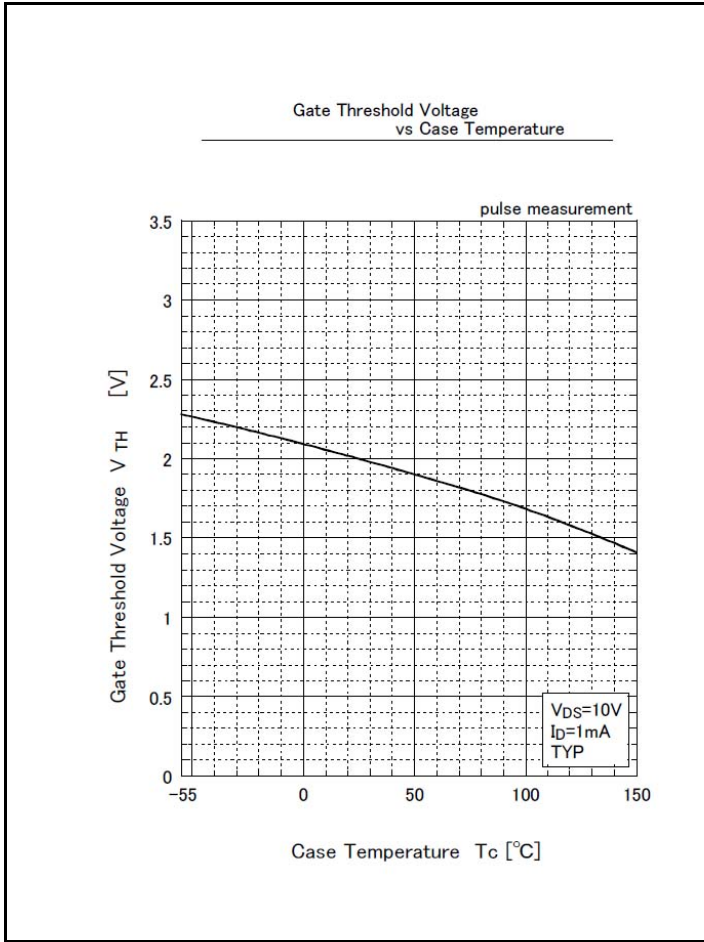


Static Drain-Source On-state Resistance vs Drain Current

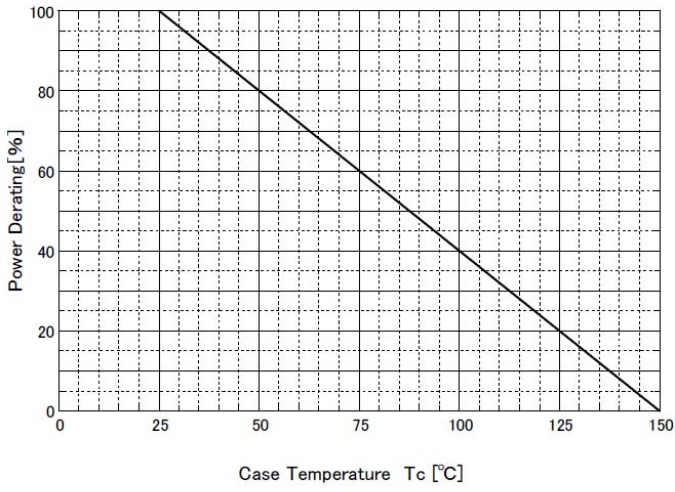


Static Drain-Source On-state Resistance vs Case Temperature

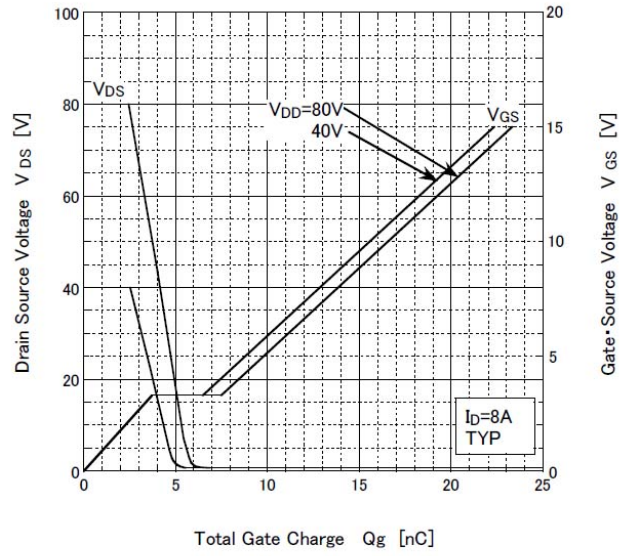




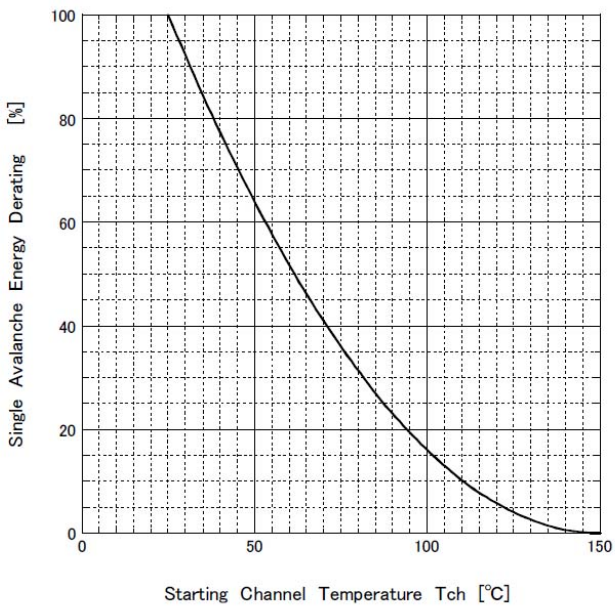
Power Derating - Case Temperature



Gate Charge Characteristics

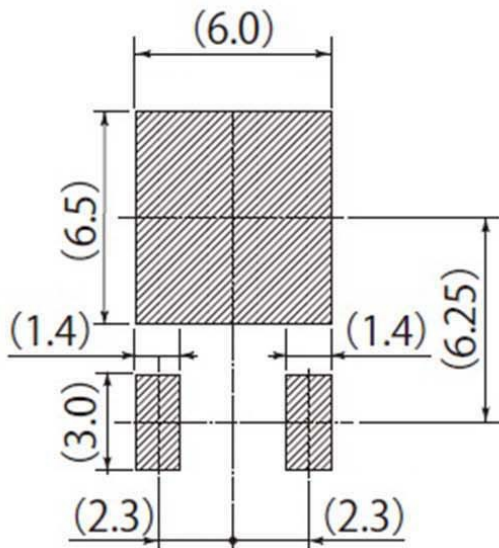
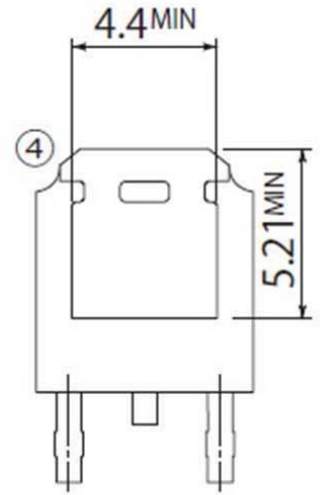
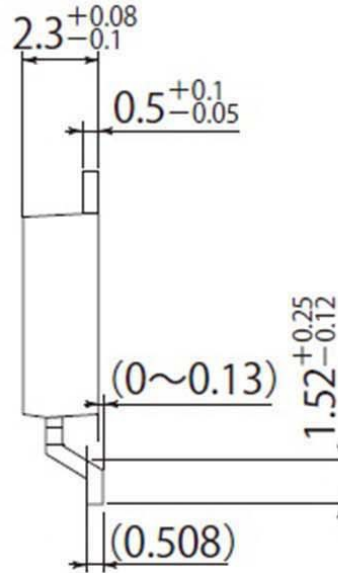
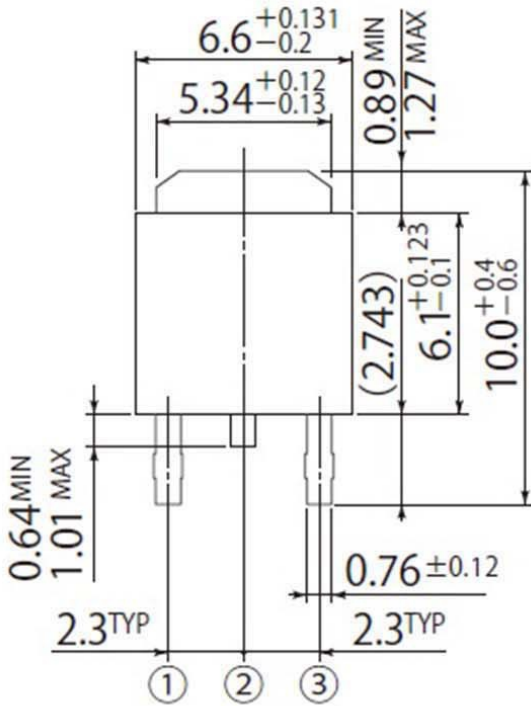


Single Avalanche Energy Derating vs Channel Temperature



G2

JEDEC Code	TO-252AA
JEITA Code	-
House Name	FB



Referential Soldering Pad

• Optimize soldering pad to the board design and soldering condition.

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