

# P80FG7R5EN

## Power MOSFETs

75V, 80A, N-channel

### Feature

- N-channel
- SMD
- Low Ron
- 10V Gate Drive
- Low Capacitance
- Pb free terminal
- RoHS:Yes

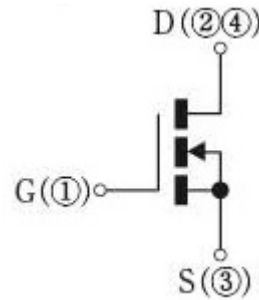
### OUTLINE

Package (House Name): FG

Package (JEDEC Code): TO-263AB



### Equivalent circuit



### Absolute Maximum Ratings (unless otherwise specified : Tc=25°C)

Item	Symbol	Conditions	Ratings	Unit
Storage temperature	T <sub>stg</sub>		-55 to 150	°C
Channel temperature	T <sub>ch</sub>		150	°C
Drain-source voltage	V <sub>DSS</sub>		75	V
Gate-source voltage	V <sub>GSS</sub>		±20	V
Continuous drain current(DC)	I <sub>D</sub>		80	A
Continuous drain current(Peak)	I <sub>DP</sub>	Pulse width 10μs, duty=1/100	320	A
Total power dissipation	P <sub>T</sub>		128	W
Single avalanche current	I <sub>AS</sub>	Starting T <sub>ch</sub> =25°C T <sub>ch</sub> ≤150°C	44	A
Single avalanche energy	E <sub>AS</sub>	Starting T <sub>ch</sub> =25°C T <sub>ch</sub> ≤150°C	175	mJ

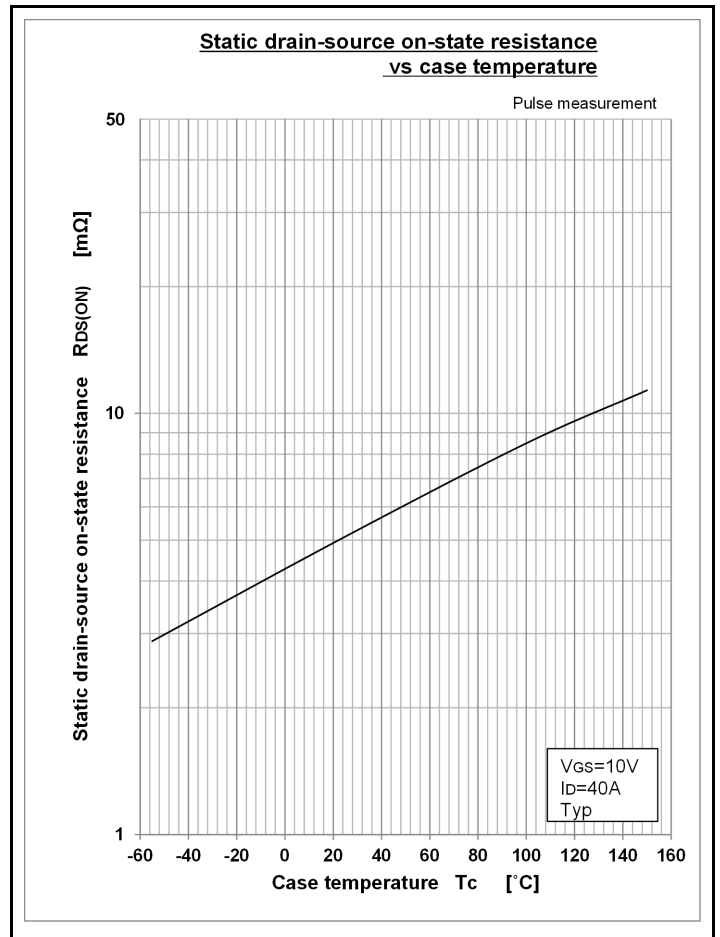
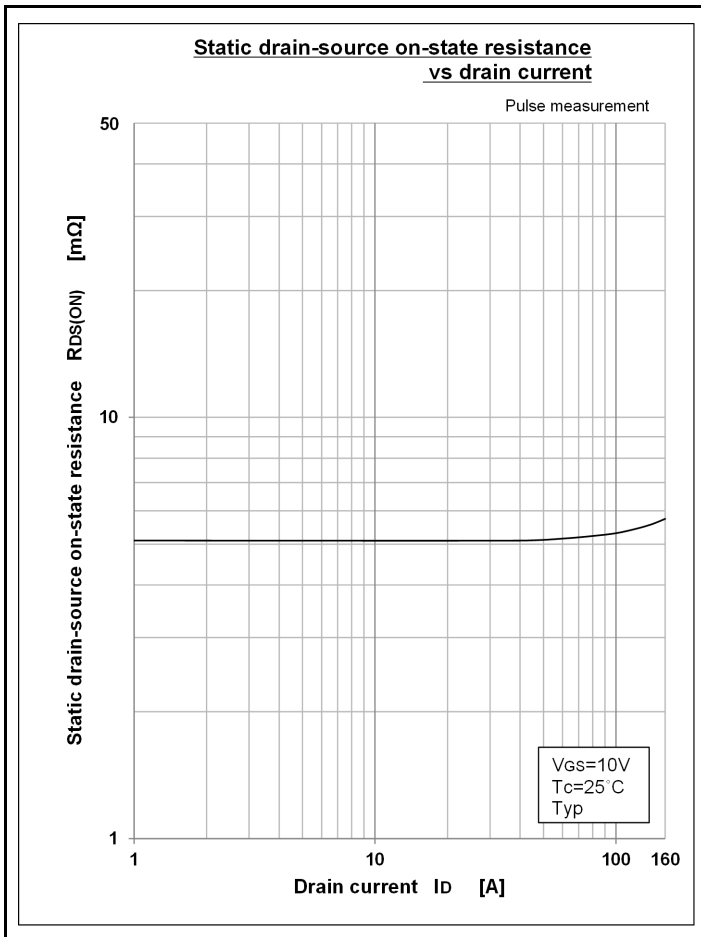
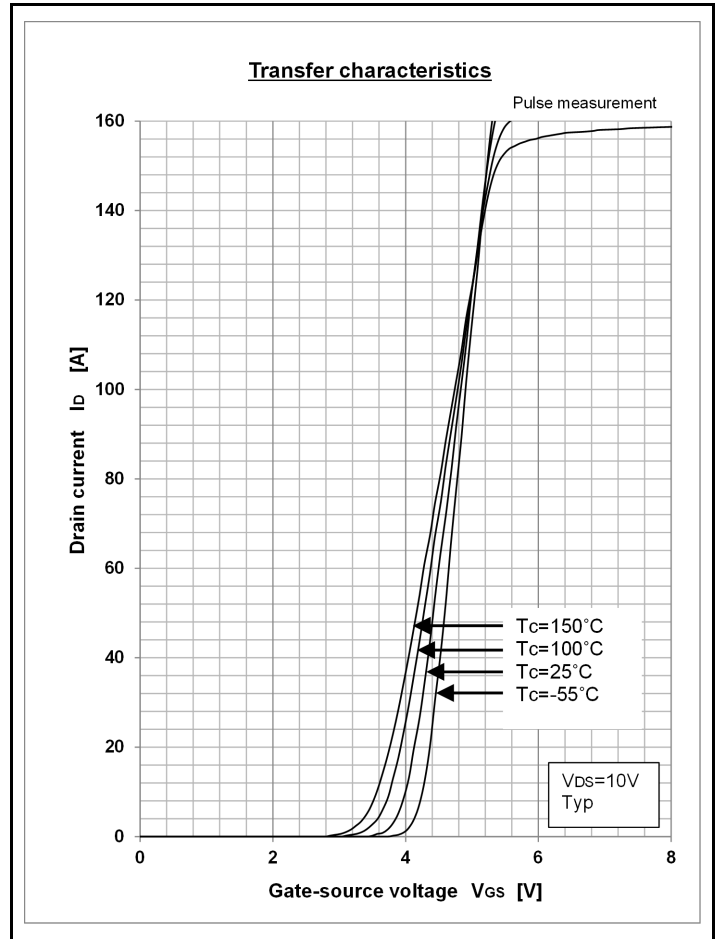
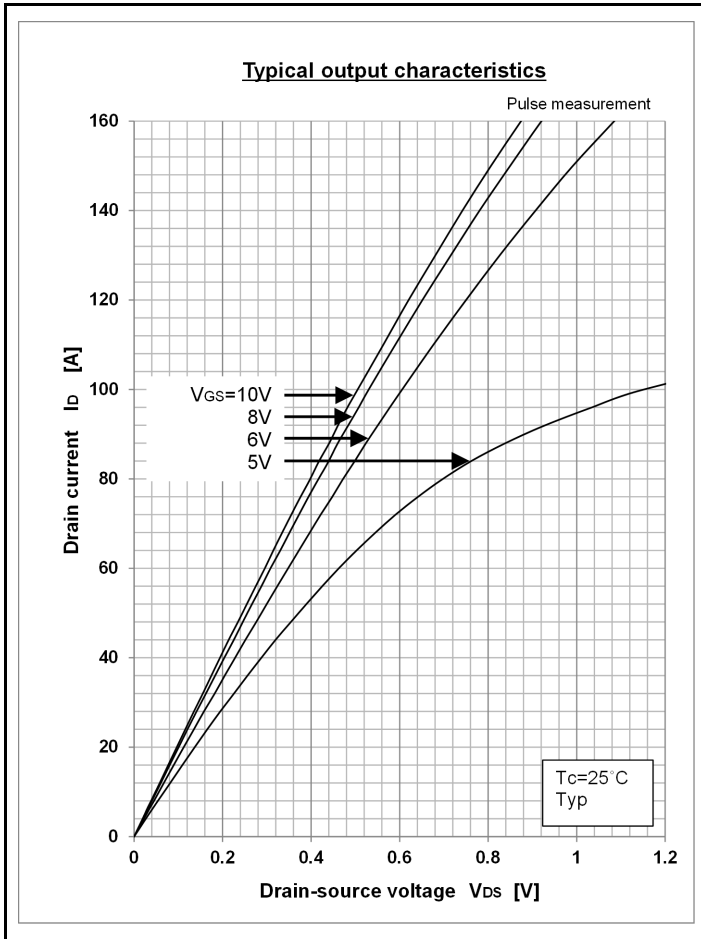
※ :See the original Specifications

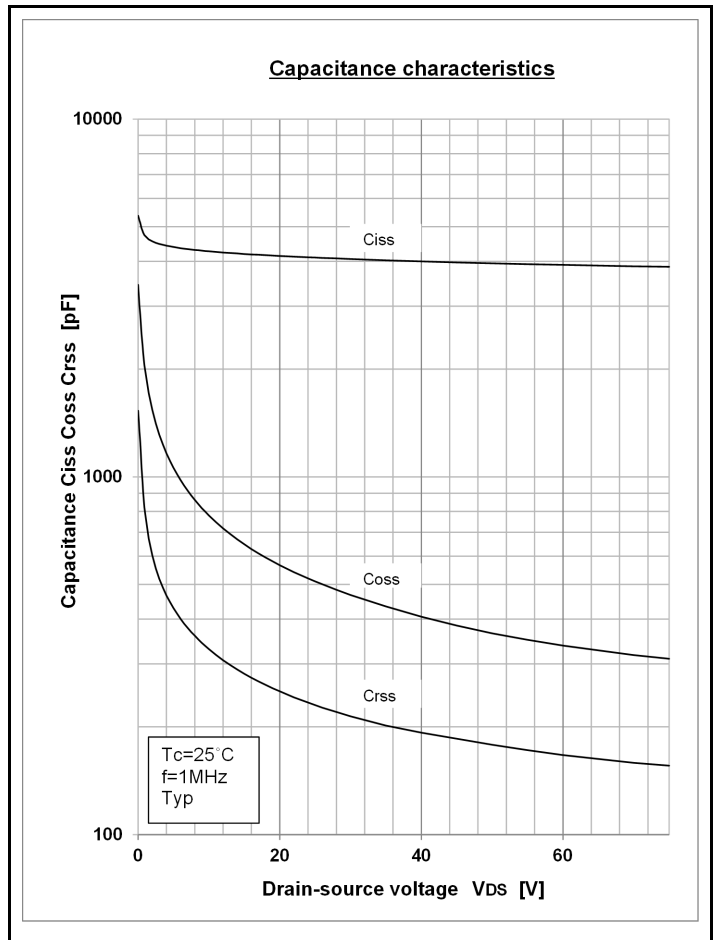
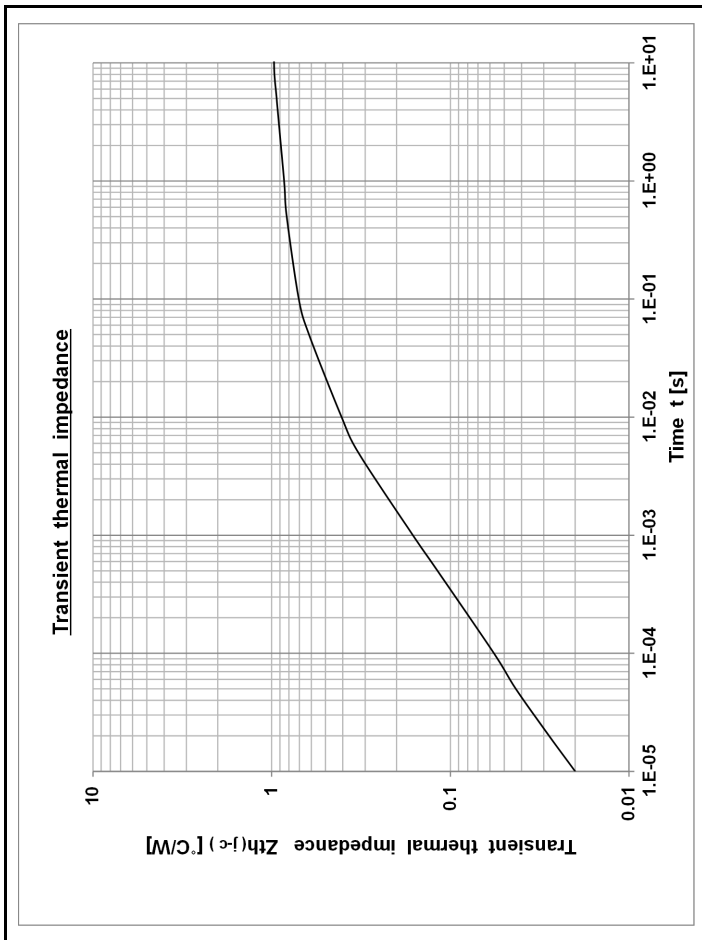
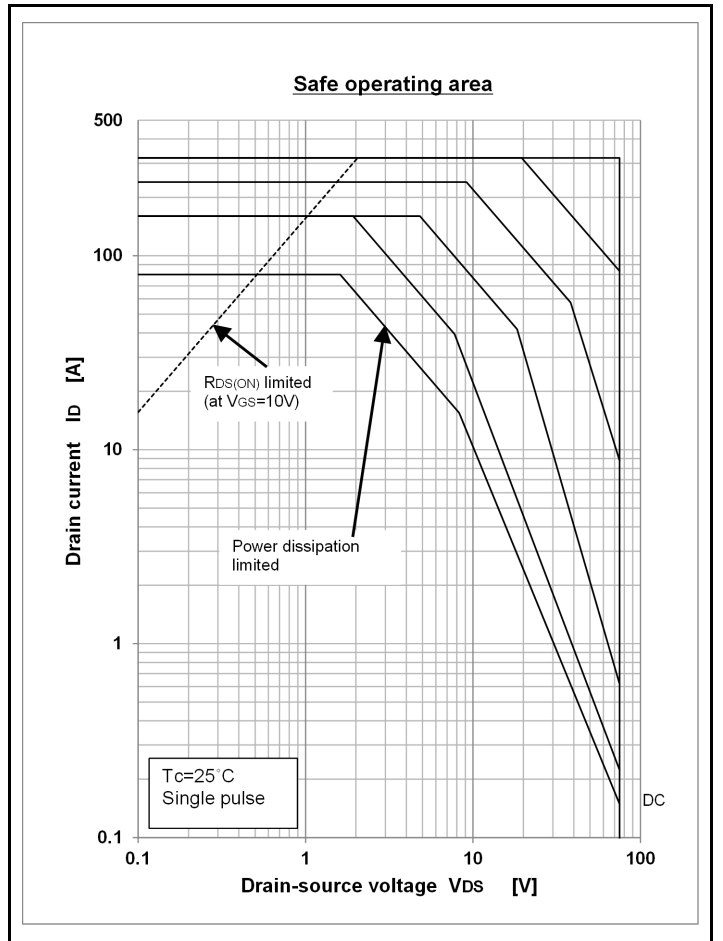
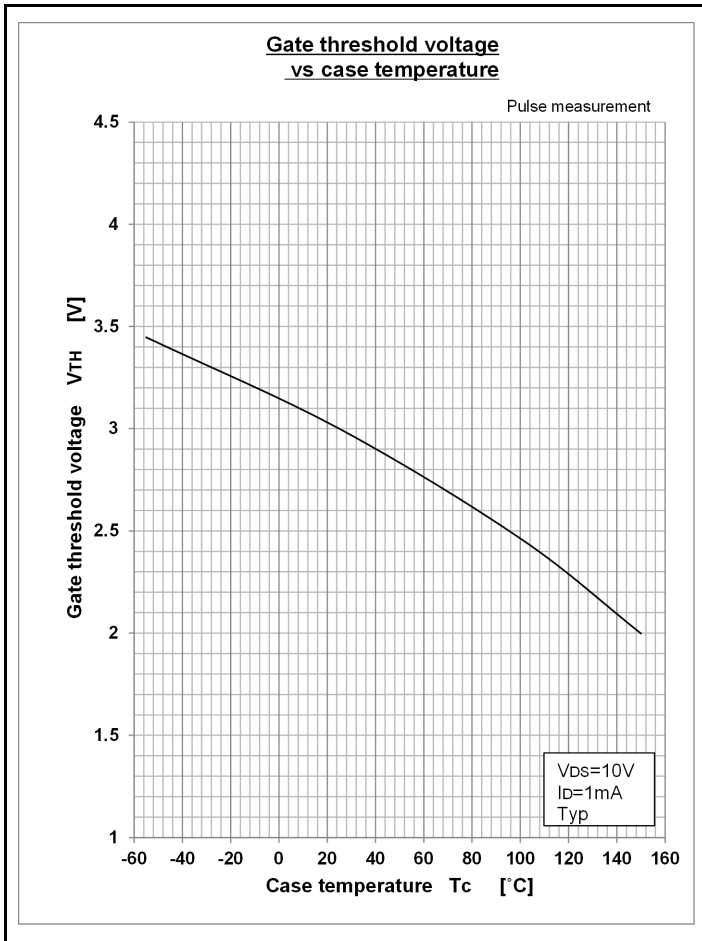
**Electrical Characteristics** (unless otherwise specified : Tc=25°C)

Item	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Drain-Source breakdown voltage	$V_{(BR)DSS}$	ID=1mA, VGS=0V	75			V
Zero gate voltage drain current	$I_{DSS}$	VDS=75V, VGS=0V			1	μA
Gate-source leakage current	$I_{GSS}$	VGS=±20V, VDS=0V			±0.1	μA
Forward transconductance	$g_{fs}$	ID=40A, VDS=10V	20	40		S
Static drain-source on-state resistance	$R_{DS(ON)}$	ID=40A, VGS=10V		0.0051	0.0064	Ω
Gate threshold voltage	$V_{th}$	ID=1mA, VDS=10V	2	3	4	V
Source-drain diode forward voltage	$V_{SD}$	IS=80A, VGS=0V			1.5	V
Thermal resistance	$R_{th(j-c)}$	Junction to case			0.97	°C/W
Total gate charge	$Q_g$	VDD=60V, VGS=10V, ID=80A		67		nC
Gate to source charge	$Q_{gs}$	VDD=60V, VGS=10V, ID=80A		19		nC
Gate to drain charge	$Q_{gd}$	VDD=60V, VGS=10V, ID=80A		24		nC
Input capacitance	$C_{iss}$	VDS=25V, VGS=0V, f=1MHz		4100		pF
Reverse transfer capacitance	$C_{rss}$	VDS=25V, VGS=0V, f=1MHz		230		pF
Output capacitance	$C_{oss}$	VDS=25V, VGS=0V, f=1MHz		510		pF
Turn-on delay time	$t_{d(on)}$	ID=40A, RL=0.94Ω, VDD=37.5V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		13		ns
Rise time	$t_r$	ID=40A, RL=0.94Ω, VDD=37.5V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		30		ns
Turn-off delay time	$t_{d(off)}$	ID=40A, RL=0.94Ω, VDD=37.5V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		25		ns
Fall time	$t_f$	ID=40A, RL=0.94Ω, VDD=37.5V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		5		ns
Diode reverse recovery time	$t_{rr}$	IF=80A, VGS=0V, di/dt=100A/μs		51		ns
Diode reverse recovery charge	$Q_{rr}$	IF=80A, VGS=0V, di/dt=100A/μs		95		nC

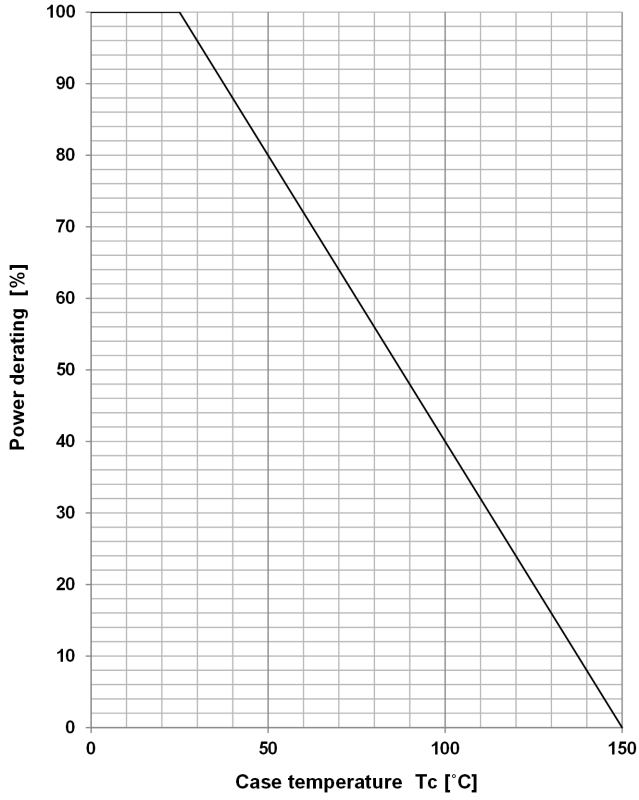
※ : See the original Specifications

# CHARACTERISTIC DIAGRAMS

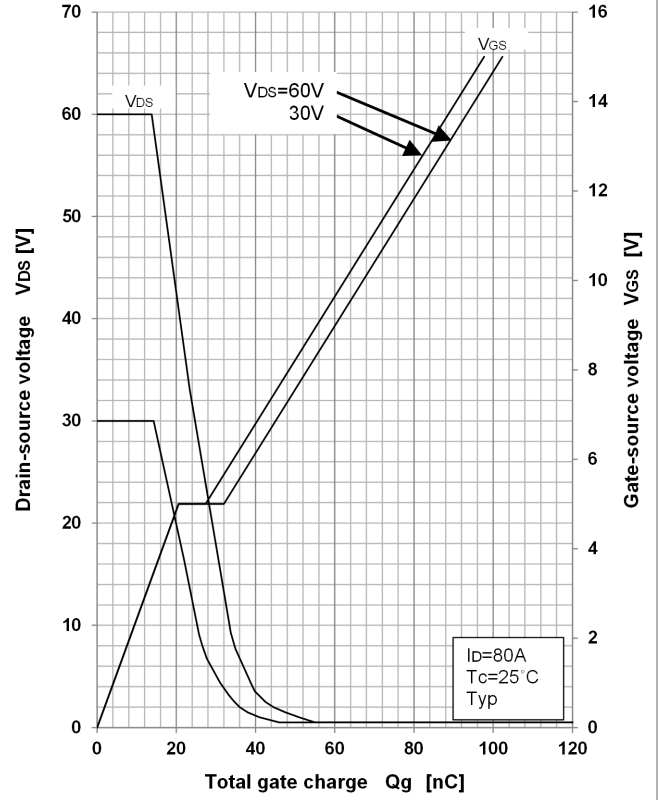




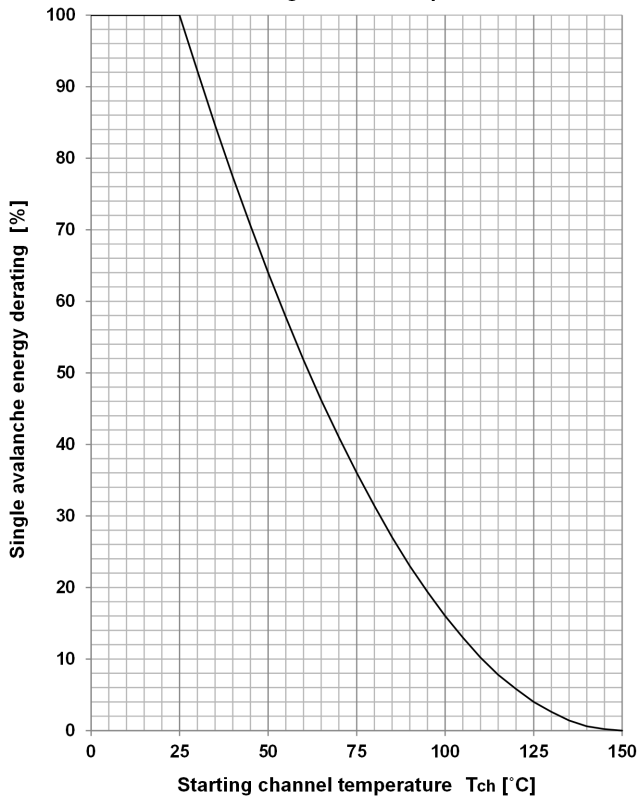
**Power derating vs case temperature**



**Gate charge characteristics**

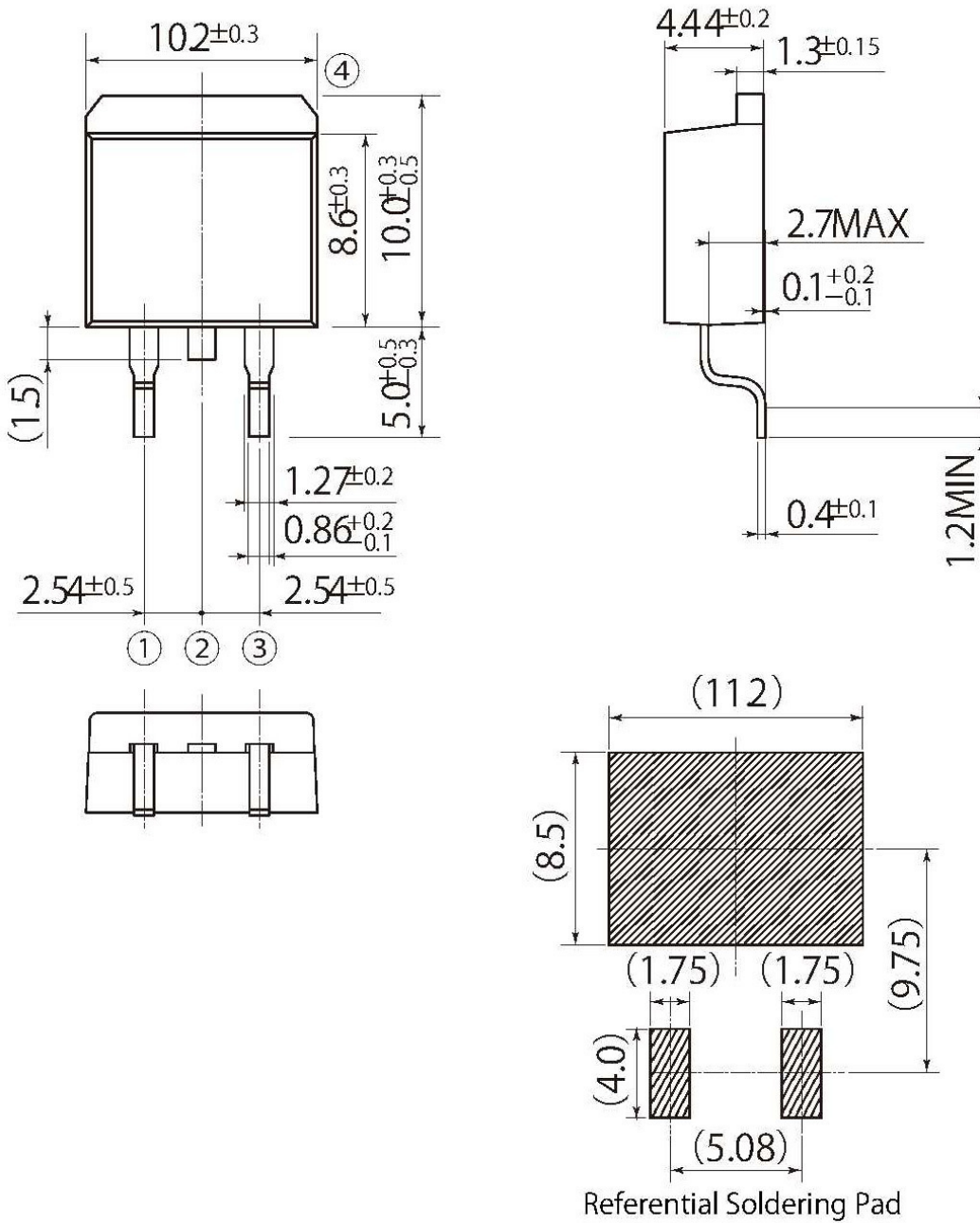


**Single avalanche energy derating vs starting channel temperature**



H4

JEDEC Code	TO-263AB
JEITA Code	-
House Name	FG



• Optimize soldering pad to the board design and soldering condition.

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