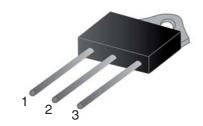
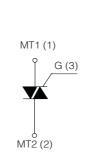


### **INSULATED TO3P**





#### **On-State Current**

#### **Gate Trigger Current**

40 Amp

≤ 50 mA (16) ≤ 35 mA (14)

Off-State Voltage

600 V ÷ 800 V

#### **FEATURES**

- Provides voltage insulated tab (rated at 2500V RMS)
- Glass/passivated die junctions
- High current Triac
- Low thermal resistance
- High commutation
- High surge current capability
- Low forward voltaje drop
- Solder dip 260 °C, 10s
- Component in accordance to RoHS 2011/65/EU and WEEE 2002/96/EC
- Certified compliance of UL 1557 Standard for Electrically Isolated Semiconductors, Fille reference E320541, Vol. 3





• Polarity: As marked on the body.

•Terminals: Matte tin plated leads, solderable per MIL-STD-750 Method 2026, J-STD-002 and JESD22-B102. Consumer grade, meets JESD 201 class 1A whisker test.

#### TYPICAL APPLICATIONS

 Used on inductive loads, thanks to their high commutation performances.

# Maximun Ratings and Electrical Characteristics at 25°C

SYMBOL	PARAMETER	CONDITIONS	Value	Unit
I <sub>T(RMS)</sub>	RMS On-state Current (full sine wave)	All Conduction Angle, T <sub>c</sub> = 80 °C	40	А
I <sub>TSM</sub>	Non-repetitive On-State Current	Full Cycle, 60 Hz (t = 16.7 ms)	420	А
I <sub>TSM</sub>	Non-repetitive On-State Current	Full Cycle, 50 Hz (t = 20 ms)	400	А
l <sup>2</sup> t	Fusing Current	tp = 10 ms, Half Cycle	1000	A <sup>2</sup> s
I <sub>GM</sub>	Peak Gate Current	20 μs max. Tj = 125 °C	8	А
$P_{G(AV)}$	Average Gate Power Dissipation	Tj = 125 °C	1	W
dl/dt	Critical rate of rise of on-state current	$I_G = 2x I_{GT}, t_r \le 100 \text{ns}$ $f = 120 \text{ Hz}, T_j = 125 ^{\circ}\text{C}$	50	A/µs
T <sub>j</sub>	Operating Temperature		(-40 +125)	°C
$T_{stg}$	Storage Temperature		(-40 +125)	°C
T <sub>sld</sub>	Soldering Temperature	10s max	260	°C
$V_{\rm iso}$	R.M.S. isolation voltage 50/60 Hz sinusoidal waveform		2.500	Vac

SYMBOL		PARAMETER	VOL	Unit	
		. ,	M	N	Onne
	$V_{DRM}/V_{RRM}$	Repetitive Peak Off State Voltage	600	800	V

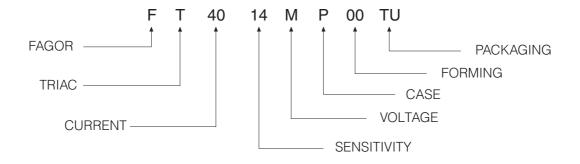


### Electrical Characteristics at Tamb = 25 °C

CVMDOL	DADAMETED	CONDITIONS		Ouedrant		SENSITIVITY		I I m i h
SYMBOL	PARAMETER	CONDITIO	NS	Quadrant		14	16	Unit
I <sub>GT</sub> <sup>(1)</sup>	Gate Trigger Current	$V_D = 12 V_{DC}, R_L = 339$	$\Omega$ , $T_j = 25  ^{\circ}C$	Q1÷Q3	MAX	35	50	mA
V <sub>GT</sub>	Gate Trigger Voltage	$V_D = 12 V_{DC}, R_L = 339$	$\Omega$ , $T_j = 25  ^{\circ}C$	Q1÷Q3	MAX	1.3		V
$V_{GD}$	Gate Non Trigger Voltage	$V_D = V_{DRM}, R_L = 3.3 \text{ Kg}$	$Ω, T_j = 125 °C$	Q1÷Q3	MIN	0.2		V
I <sub>H</sub> <sup>(2)</sup>	Holding Current	$I_T$ =500 mA,Gate ope	en, $T_j = 25$ °C		MAX	60	80	mA
IL	Latching Current	I <sub>G</sub> = 1.2 I <sub>GT</sub> , T <sub>j</sub> = 25 °C		Q1,Q3	MAX	50	70	mA
				Q2	MAX	160	160	mA
dV/dt (2)	Critical Rate of Voltage Rise	$V_D = 0.67 \times V_{DRM}$ , Gate open			MIN	400	500	V/µs
		T <sub>j</sub> = 125 °C						
(dV/dt)c (2)	Critical Rate of Commutating off-state voltage	(dl/dt)c = 20 A/ms	$T_j = 125  ^{\circ}\text{C}$		MIN	1	0	V/ms
V <sub>TM</sub> <sup>(2)</sup>	On-state Voltage	$I_T = 60 \text{ Amp, tp} = 380$	$\mu$ s, $T_j = 25$ °C		MAX	1.	55	V
V <sub>t (0)</sub> (2)	Threshold Voltage	T <sub>j</sub> = 125 °C			MAX	0.	85	V
r <sub>d</sub> <sup>(2)</sup>	Dynamic resistance	T <sub>j</sub> = 125 °C			MAX	1	0	mΩ
I <sub>DRM</sub> /I <sub>RRM</sub>	Off-State Leakage Current	$V_D = V_{DRM}$	T <sub>j</sub> = 125 °C		MAX	į	5	mA
		$V_R = V_{RRM}$	$T_j = 25  ^{\circ}C$		MAX	2	0	μΑ
R <sub>th(j-c)</sub>	Thermal Resistance	for AC 360° conduction angle				0.9		°C/W
	Junction-Case							
R <sub>th(j-a)</sub>	Thermal Resistance					5	0	°C/W
	Junction-Ambient							

<sup>(1)</sup> Minimum  $I_{GT}$  is guaranted at 5% of  $I_{GT}$  max.

#### **Part Number Information**



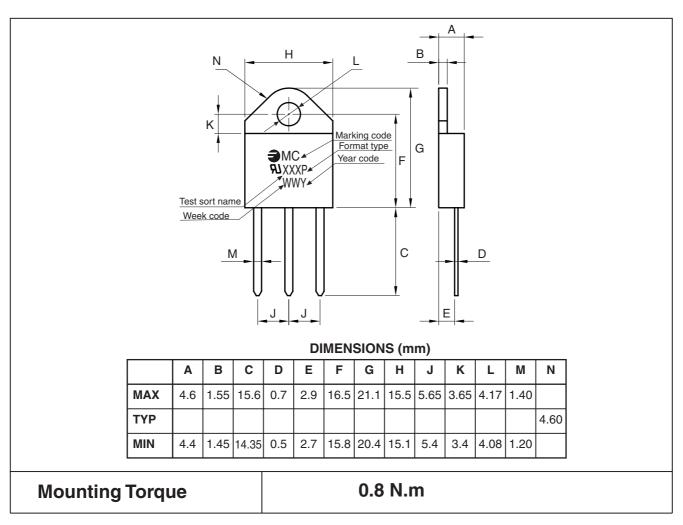
 $<sup>\</sup>ensuremath{\text{(2)}}\xspace For either polarity of electrode \ensuremath{\text{MT2}}\xspace voltage \ensuremath{\text{with reference to electrode MT1}}\xspace.$ 



# **Ordering information**

PREFERRED P/N	PACKAGE CODE	DELIVERY MODE	BASE QUANTITY	UNIT WEIGHT (g)
FT4014MP 00TU	TU	TUBE	450	4.50

# Package Outline Dimensions: (mm) INSULATED TO3P





## Ratings and Characteristics (Ta 25 °C unless otherwise noted)

Fig. 1: Maximum power dissipation versus RMS on-state current (full cycle).

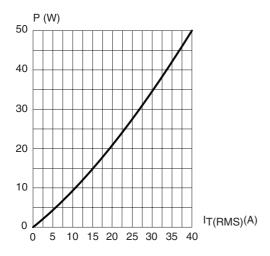


Fig. 3: On-state characteristics (maximum values)

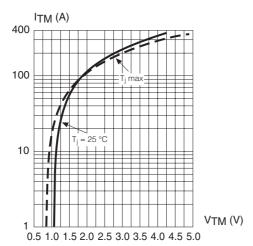


Fig. 5: Non repetitive surge peak on-state current for a sinusoidal pulse with width: tp < 10 ms, and corresponding value of  $l^2t$ .

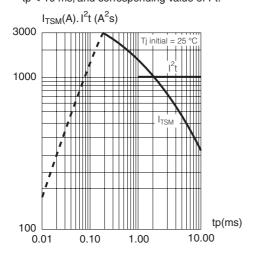


Fig. 2: RMS on-state current versus case temperature (full cycle).

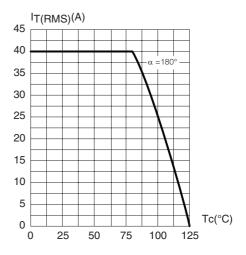


Fig. 4: Surge peak on-state current versus number of cycles

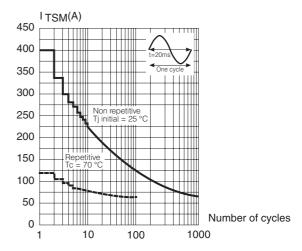
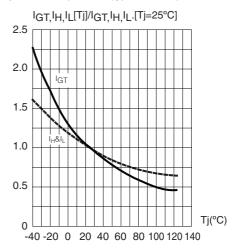


Fig. 7: Relative variation of gate trigger current, holding current and latching versus junction temperature (typical values)





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