



Future Technology Devices International Ltd.

TN_183 FT232RN / FT245RN Errata Technical Note

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The intention of this errata technical note is to give a detailed description of known functional or electrical issues with the FTDI FT232RN / FT245RN devices.

The current revision of the FT232RN / FT245RN is **revision B**.

Use of FTDI devices in life support and/or safety applications is entirely at the user's risk, and the user agrees to defend, indemnify, and hold harmless FTDI from any and all damages, claims, suits, or expense resulting from such use.

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1 FT232RN / FT245RN Revision

FT232RN / FT245RN part numbers are listed in Table 1. The letter at the end of date code on the device markings identifies the device revision as shown in Section 5.

The current revision of the FT232RN / FT245RN is **revision B**. At the time of releasing this Technical Note there is one known minor issue with this silicon revision. A workaround is provided for this issue.

Part Number	Package
FT232RNL / FT245RNL	28 Pin SSOP
FT232RNQ / FT245RNQ	32 Pin QFN

Table 1 FT232RN / FT245RN Part Numbers

This erratum technical note covers the revisions of FT232RN / FT245RN listed in Table 2.

Revision	Notes
A	First device revision
B	Second device revision

Table 2 FT232RN / FT245RN Revisions

2 Errata History Table – Functional Issues

Functional Problem	Short description	Errata occurs in device revision
PLL	PLL cannot sync with USB traffic at internal clock mode	A

Table 3 Functional Errata

2.1 Errata History Table – Electrical Specification Deviations

Deviations	Short description	Errata occurs in device revision
Input voltage applying to OSCI cannot be higher than 1.98V	FT232RN / FT245RN OSCI input voltage is 1.98V (max). This is incompatible with the original FT232R / FT245 OSCI input voltage which is 3.63V (max).	A, B

Table 4 Electrical Errata

3 Functional Issues of FT232RN / FT245RN

3.1 Revision A

3.1.1 PLL cannot sync with USB traffic at internal clock mode

Introduction:

The PLL cannot sync with USB traffic at internal clock mode.

Issue:

At internal clock mode, the device's PLL cannot sync with USB traffic to produce accurate 48MHz clock during the USB enumeration process. This USB host cannot detect the device at internal clock mode.

Workaround:

Configure the device to use external clock mode instead of internal clock mode. At external clock mode, the device's PLL can sync with the external clock to produce accurate 48MHz clock.

This issue is corrected at silicon revision B.

Package specific:

The effected packages are listed in Table 5.

Package	Applicable (Yes/No)
FT232RNL / FT245RNL	Y
FT232RNQ / FT245RNQ	Y

Table 5 Effected Packages

3.2 Revision B

There are no known new functional issues specific to revision B.

4 Electrical specification deviations of FT232RN / FT245RN

4.1 Revision A

4.1.1 Input voltage applying to OSCI cannot be higher than 1.98V

Introduction:

FT232RN / FT245RN OSCI input voltage is 1.98V (max). This is incompatible with the original FT232R / FT245R OSCI input voltage which is 3.63V (max).

Issue:

The OSCI input of FT232RN / FT245RN is powered by the internal 1.8V circuit. If the input voltage applying to OSCI is higher than 1.98V, then it will induce back current to the device and rise the internal power to higher than 1.98V. This would cause the device operates abnormally.

Workaround:

Adjust the external clock source with input level below 1.98V or use an external crystal.

Package specific:

The effected packages are listed in Table 6.

Package	Applicable (Yes/No)
FT232RNL / FT245RNL	Y
FT232RNQ / FT245RNQ	Y

Table 6 Effected Packages

4.2 Revision B

4.2.1 Input voltage applying to OSCI cannot be higher than 1.98V

Introduction:

FT232RN / FT245RN OSCI input voltage is 1.98V (max). This is incompatible with the original FT232R / FT245R OSCI input voltage which is 3.63V (max).

Issue:

The OSCI input of FT232RN / FT245RN is powered by the internal 1.8V circuit. If the input voltage applying to OSCI is higher than 1.98V, then it will induce back current to the device and rise the internal power to higher than 1.98V. This would cause the device to operate abnormally.

Workaround:

Configure the device to use internal clock mode (factory default) instead of external clock mode and leave OSCI unconnected.

FT232RN / FT245RN internal clock can be operated normally with wider VCC range from 5.25V down to 3.3V. This is unlike the original FT232R / FT245R where external clock should be used if VCC is below 4V. Therefore, it is highly recommended to use internal clock mode instead of external clock mode in FT232RN / FT245RN.

On the other hand, in case if using external clock is preferable in some specific application, please adjust the external clock source with input level below 1.98V or use an external crystal.

Package specific:

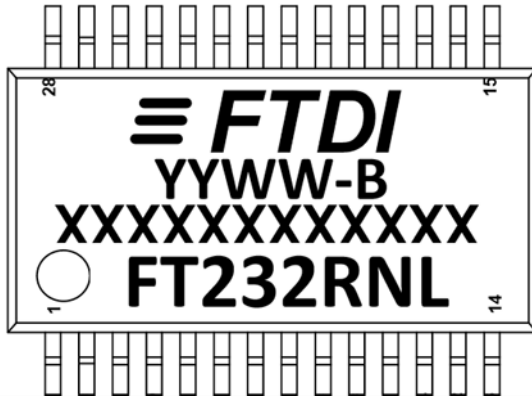
The effected packages are listed in Table 7.

Package	Applicable (Yes/No)
FT232RNL / FT245RNL	Y
FT232RNQ / FT245RNQ	Y

Table 7 Effected Packages

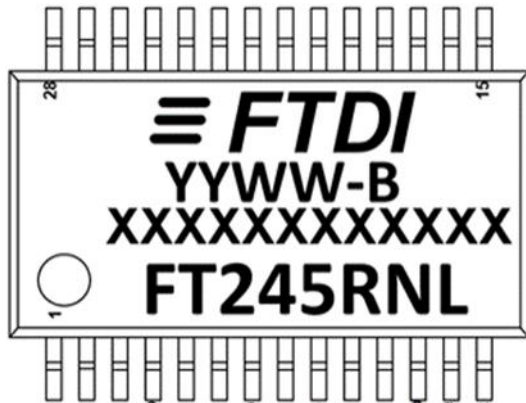
5 FT232RN / FT245RN Package Markings

FT232RN / FT245RN is available in a RoHS Compliant packages, 28 pin SSOP and 32 pin QFN. An example of the markings on the package is shown in Figure 5-1 to 5-4.



- Line 1 – FTDI Logo
- Line 2 – Date Code and Revision
- Line 3 – Wafer Lot Number
- Line 4 – FTDI Part Number

Figure 5-1 Package Markings – FT232RNL



- Line 1 – FTDI Logo
- Line 2 – Date Code and Revision
- Line 3 – Wafer Lot Number
- Line 4 – FTDI Part Number

Figure 5-2 Package Markings – FT245RNL



- Line 1 – FTDI Logo
- Line 2 – Date Code and Revision
- Line 3 – Wafer Lot Number
- Line 4 – FTDI Part Number

Figure 5-3 Package Markings – FT232RNQ



- Line 1 – FTDI Logo
- Line 2 – Date Code and Revision
- Line 3 – Wafer Lot Number
- Line 4 – FTDI Part Number

Figure 5-4 Package Markings – FT245RNQ

6 Contact Information

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Distributor and Sales Representatives

Please visit the Sales Network page of the [FTDI Web site](#) for the contact details of our distributor(s) and sales representative(s) in your country.

Appendix A - References

Document References

NA

Acronyms and Abbreviations

Terms	Description
SSOP	Shrink Small-Outline Package
QFN	Quad Flat No-Lead Package
RoHS	Restriction of Hazardous Substances
USB	Universal Serial Bus
PLL	Phase-Locked Loop

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Appendix C – Revision History

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1.0	Initial Release	26-08-2022