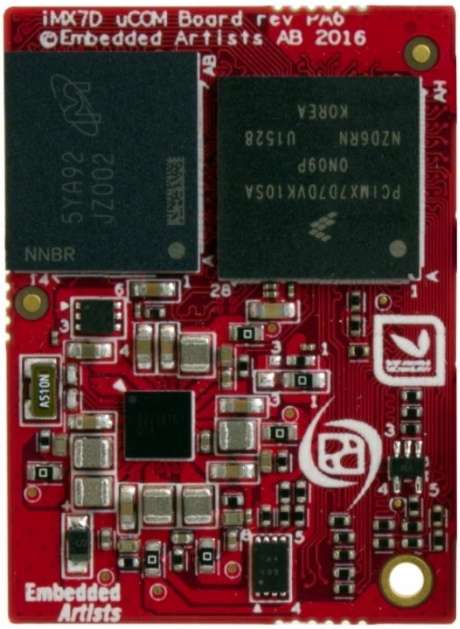
iMX7 Dual uCOM Board Datasheet



Get Up-and-Running Quickly and
Start Developing Your Application On Day 1!

Embedded Artists

Embedded Artists AB
Davidshallsgatan 16
211 45 Malmö
Sweden

http://www.EmbeddedArtists.com

Disclaimer

Embedded Artists AB makes no representation or warranties with respect to the contents hereof and specifically disclaim any implied warranties or merchantability or fitness for any particular purpose. The information has been carefully checked and is believed to be accurate, however, no responsibility is assumed for inaccuracies.
Information in this publication is subject to change without notice and does not represent a commitment on the part of Embedded Artists AB.

Feedback

We appreciate any feedback you may have for improvements on this document.

Trademarks

All brand and product names mentioned herein are trademarks, services marks, registered trademarks, or registered service marks of their respective owners and should be treated as such.

Table of Contents

1 Document Revision History 6

2 Introduction 7

2.1 Hardware 7

2.2 Software 8

2.3 Features and Functionality 8

2.4 Reference Documents 10

3 Board Pinning 12

3.1 Pin Numbering 12

3.2 Pin Assignment 13

4 Pin Mapping 21

4.1 Functional Multiplexing on I/O Pins 21

4.1.1 Alternative I/O Function List 21

4.2 I/O Pin Control 21

5 Interface Description 22

5.1 Camera Interfaces 23

5.1.1 Parallel Camera Interface 23

5.1.2 Serial Camera Interface 25

5.2 Display Interfaces 26

5.2.1 Parallel RGB LCD Interface 27

5.2.2 MIPI-DSI Interface 28

5.3 Digital Audio Interfaces: Synchronous Audio Interfaces (SAI) 29

5.4 Digital Audio Interface: Medium Quality Speaker (MQS) 32

5.5 Ethernet 33

5.6 FlexCAN 35

5.7 GPIOs 36

5.8 I2C 37

5.9 JTAG 39

5.10 PCI Express 40

5.11 Power Management 41

5.12 Power Supply Signals 41

5.13 PWM 43

5.14 SD/MMC 43

5.15 ECSPI / SPI 45

5.16 UART 47

5.17 USB 50

6 Powering and PMIC Integration 52

6.1 Available Power Rails 52

6.2 Integration Without Battery 53
6.3 Integration With Li-ion Rechargeable Battery 53

7 uCOM Adapter Board 55
7.1 Pin Numbering 55
7.2 Pin Assignment 56
7.3 Interface Overview 66
7.4 I/O voltage 68

8 Boot Options 70

9 Power Modes 73
9.1 Power Mode: OFF 74
9.2 Power Mode: SNVS (RTC only) 74
9.3 Power Mode: LPSR 74
9.4 Power Modes: Low Power 74
9.5 Power Mode: RUN 75

10 Technical Specification 76
10.1 Absolute Maximum Ratings 76
10.2 Recommended Operating Conditions 76
10.3 Power Ramp-Up Time Requirements 76
10.4 Electrical Characteristics 76
10.4.1 Reset Output Voltage Range 77
10.4.2 PMIC Reset Input 77
10.5 Power Consumption 77
10.6 Mechanical Dimensions 77
10.6.1 DF40C Socket 80
10.6.2 Module Assembly Hardware 80
10.7 Environmental Specification 81
10.7.1 Operating Temperature 81
10.7.2 Relative Humidity (RH) 81
10.8 Thermal Design Considerations 81
10.8.1 Thermal Parameters 82
10.9 Product Compliance 82

11 Functional Verification and RMA 83

12 Things to Note 84
12.1 Shared Pins and Multiplexing 84
12.2 I2C Pull-up Resistors Missing on uCOM Adapter Board, rev PA2 84
12.3 Entering USB OTG Boot-mode (Manufacturing Tool), rev A 84
12.4 Cannot Access Some Memory Cards 85
12.5 Be Careful when Mounting/Detaching the uCOM Board 85
12.6 Only Use EA Board Support Package (BSP) 86

12.7 OTP Fuse Programming 86
12.8 Write Protect on Parameter Storage E2PROM 86
12.9 Integration - Contact Embedded Artists 86
12.10 ESD Precaution when Handling iMX7 Dual uCOM Board 87
12.11 EMC / ESD 87
13 Custom Design 89
14 Disclaimers 90
14.1 Definition of Document Status 91

1 Document Revision History

Revision	*Date*	*Description*
PA1	2016-06-18	First version.
PA2	2016-09-23	Clarify the 'Powering and PMIC Integration' chapter. Added 'Things to Note' about *I2C pull-ups missing* and *USB OTG boot-mode*. Added information about extra wire connection to enter USB OTG boot mode. Added information about connector placement on carrier board.
PA3	2017-04-24	Added information about peripheral interfaces. Added mounting instruction.
PA4	2017-05-03	Corrected measurement for mounting hole. Corrected J2/J3 expansion connector pin numbering.
PA5	2017-05-23	Corrected CPU version for industrial version.
PA6	2017-10-18	Added information about current consumption and corrected information about signals BATTP/BATTM/TS.

2 Introduction

This document is a datasheet that specifies and describes the *iMX7 Dual uCOM Board* mainly from a hardware point of view. Some basic software related issues are also addressed, like booting and functional verification, but there are separate software development manuals that should also be consulted.

2.1 Hardware

The *iMX7 Dual uCOM Board* is a Computer-on-Module (COM) based on NXP's dual-core ARM Cortex-A7 / M4 i.MX 7Dual System-on-Chip (SoC) application processor. The board provides a quick and easy solution for implementing a high-performance ARM dual-core Cortex-A7 / M4 based design. The two Cortex-A7 cores runs at up to 1GHz and the Cortex-M4 core at up to 200 MHz.

The heterogeneous core architecture enables the system to run an OS like Linux on the two Cortex-A7 cores and a Real-Time OS (RTOS) on the Cortex-M4. This architecture is ideal for real time applications where Linux cannot be used for all time critical task. The Cortex-M4 can handle (real time) critical tasks and can also be used to lower the power consumption.

The *iMX7 Dual uCOM Board* delivers high computational and graphical performance at very low power consumption. The on-board PMIC, supporting DVFS (Dynamic Voltage and Frequency Scaling), together with a LPDDR3 memory sub-system reduce the power consumption to a minimum.

The *iMX7 Dual uCOM Board* has an ultra small form factor and shields the user from a lot of complexity of designing a high performance system. It is a robust and proven design that allows the user to focus the product development, shorten time to market and minimize the development risk.

The *iMX7 Dual uCOM Board* targets a wide range of applications, such as:

- Portable systems
- HMI/GUI solutions
- Portable medical and health care
- Connected vending machines
- Point-of-Sale (POS) applications
- Access control panels
- Audio
- IP phones
- Smart appliances
- eReaders
- Wearables
- Home energy management systems
- Industrial automation
- HVAC Building and Control Systems
- Smart Grid and Smart Metering
- Smart Toll Systems
- Data acquisition
- Communication gateway solutions
- Connected real-time systems
- ...and much more

The picture below illustrates the block diagram of the *iMX7 Dual uCOM Board*.

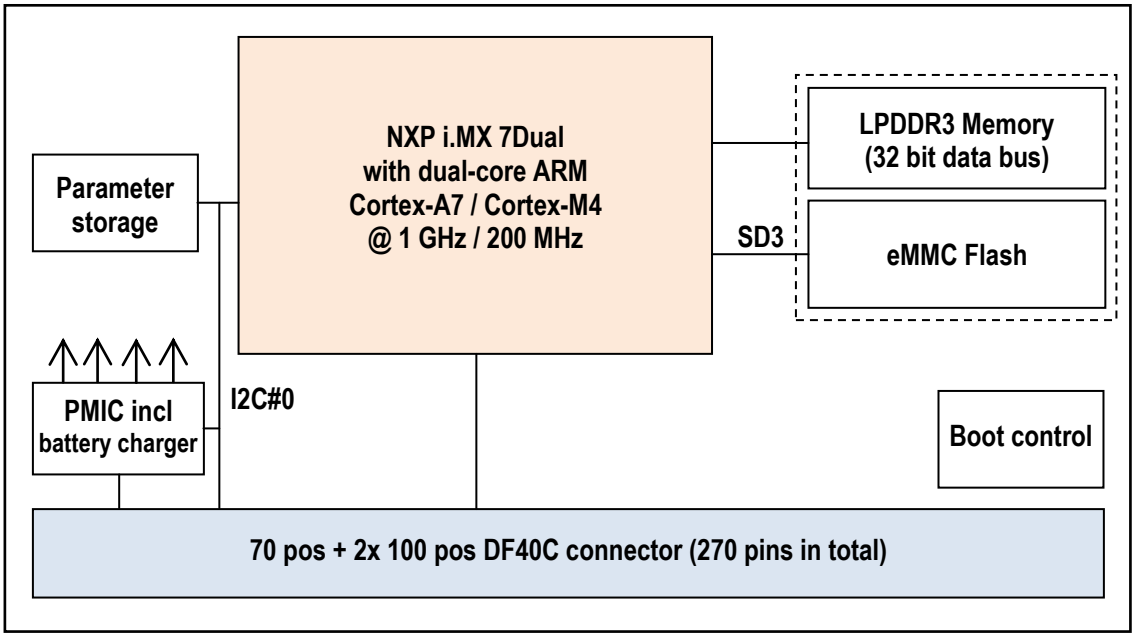


Figure 1 – iMX7 Dual uCOM Board Block Diagram

2.2 Software

The *iMX7 Dual uCOM Board* has Board Support Packages (BSPs) for Embedded Linux and Android. Precompiled images are available. Embedded Artists works with partners that can provide support for other operating systems (OS). For more information contact Embedded Artists support.

This document has a hardware focus and does not cover software development. See other documents related to the *iMX7 Dual uCOM Board* for more information about software development.

2.3 Features and Functionality

The i.MX 7Dual is a powerful SoC. The full specification can be found in NXP's *i.MX 7Dual Datasheet* and *i.MX 7Dual Reference Manual*. The table below lists the main features and functions of the *iMX7 Dual uCOM board* - which represents Embedded Artists integration of the i.MX 7Dual SoC. Due to pin configuration some functions and interfaces of the i.MX7 Dual many not be available at the same time. See i.MX 7Dual SoC datasheet and reference manual for details.

Group	Feature	iMX7 Dual uCOM Board
CPUs	NXP SoC	MCIMX7D7DVK10S (0 - 75° C) MCIMX7D3EVK10S (-20 - 85° C)
	CPU Cores	2x Cortex-A7 1x Cortex-M4 with MPU/FPU
	L1 Instruction cache	32 KByte for each Cortex-A7 16 KByte on Cortex-M4
	L1 Data cache	32 KByte for each Cortex-A7 16 KByte on Cortex-M4
	L2 Cache on Cortex-A7 cores	512 KByte
	TCM on Cortex-M4	64 KByte
	NEON SIMD media accelerator on Cortex-A7	✓

	Maximum CPU frequency	996 MHz on Cortex-A7 200 MHz on Cortex-M4
Security Functions	ARM TrustZone	✓
	Advanced High Assurance Boot	✓
	Cryptographic Acceleration and Assurance Module	✓
	Secure Non-Volatile Storage,	✓
	System JTAG controller	✓
Memory	LPDDR3 RAM Size	1 GByte
	LPDDR3 RAM Speed	1066 MT/s
	LPDDR3 RAM Memory Width	32 bit
	eMMC NAND Flash (8 bit)	8 GByte
Graphical Processing	PiXel Processing Pipeline (PXP)	✓
Graphical Output	RGB, 24-bit parallel interface	✓
	MIPI-DSI, 2 lanes	✓
	EPD	✓ (Note: not on industrial ver.)
Graphical Input	Parallel camera, up to 24-bit parallel interface	✓
	MIPI-CSI, 2 lanes	✓
Interfaces (all functions are not available at the same time)	Dual 10/100/1000 Mbps Gigabit Ethernet controllers (IEEE1588 compliant) with support for Audio Video Bridging (AVB)	✓ **Note**: off-board PHYs required
	Quad SPI	✓
	PCIe v2.1 (1 lane)	✓
	4 ch 12-bit ADC	✓
	2x USB 2.0 OTG ports, 1x HSIC	✓
	3x SD3.0/MMC 5.0	✓ SD3 interface used on-board to eMMC
	4x SPI, 7x UART, 4x I²C, 3x I²S/AC97	✓
	Dual FlexCAN, CAN bus 2.0B	✓ (Note: not on industrial ver.)
	4x PWM, KPP, GPIOs, WDOG	✓
Other	PMIC (BD71815GW) supporting DVFS techniques for low power modes	✓
	PMIC (BD71815GW) with Coulomb counter for battery fuel gauging. Up to 28V input voltage	✓
	E2PROM storing board information including Ethernet MAC address and memory bus setup parameters	✓

	BD71815AGW low power RTC	✓
	White LED driver, 25mA, up to 26V	✓
	On-board watchdog functionality	✓

2.4 Reference Documents

The following documents are important reference documents and should be consulted when integrating the *iMX7 Dual uCOM board*:

- EACOM Board Integration Manual - note that this document is written for creating EACOM carrier boards, which the *iMX7 Dual uCOM board* is not, but all interface principles are still the same.

The following NXP documents are also important reference documents and should be consulted for functional details:

- IMX7DCEC, i.MX 7Dual Applications Processors for Consumer Products - Data Sheet, latest revision
- IMX6DRM, i.MX 7Dual Applications Processor Reference Manual, latest revision
- IMX7DCE, Chip Errata for the i.MX 7Dual, latest revision
  Note: It is the user's responsibility to make sure all errata published by the manufacturer are taken note of. The manufacturer's advice should be followed.
- i.MX 7Dual Power Consumption Measurement, latest revision
- i.MX 7Dual Product Lifetime Usage Estimates, latest revision

The following documents are external industry standard reference documents and should also be consulted when applicable:

- eMMC (Embedded Multi-Media Card) the eMMC electrical standard is defined by JEDEC JESD84-B45 and the mechanical standard by JESD84-C44 (www.jedec.org)
- GbE MDI (Gigabit Ethernet Medium Dependent Interface) defined by IEEE 802.3. The 1000Base-T operation over copper twisted pair cabling is defined by IEEE 802.3ab (www.ieee.org)
- The I2C Specification, Version 2.1, January 2000, Philips Semiconductor (now NXP) (www.nxp.com)
- I2S Bus Specification, Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) (www.nxp.com)
- JTAG (Joint Test Action Group) defined by IEEE 1149.1-2001 - IEEE Standard Test Access Port and Boundary Scan Architecture (www.ieee.org)
- MXM3 Graphics Module Mobile PCI Express Module Electromechanical Specification, Version 3.0, Revision 1.1, © 2009 NVIDIA Corporation (www.mxm-sig.org)
- PCI Express Specifications (www.pci-sig.org)
- SD Specifications Part 1 Physical Layer Simplified Specification, Version 3.01, May 18, 2010, © 2010 SD Group and SD Card Association (Secure Digital) (www.sdcard.org)

- SPDIF (aka S/PDIF) (Sony Philips Digital Interface) - IEC 60958-3
- SPI Bus – “Serial Peripheral Interface” – de-facto serial interface standard defined by Motorola. A good description may be found on Wikipedia (http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus)
- USB Specifications (www.usb.org)

3 Board Pinning

Because of the ultra-compact form factor, the *iMX7 Dual uCOM Board* does not have a standard pinning that is compatible between different boards (like the EACOM standard).

There are three Hirose DF40C expansion connectors; one 70 pos and two 100 pos connectors. The 0.4mm pitch connectors have a board-to-board stacking height of only 1.5mm. There are also versions of the receptacle connectors that gives 3.0mm stacking height.

3.1 Pin Numbering

The figures below illustrates the location of the three expansion connectors and their respective pin numbering on the bottom side of the *iMX7 Dual uCOM Board*.

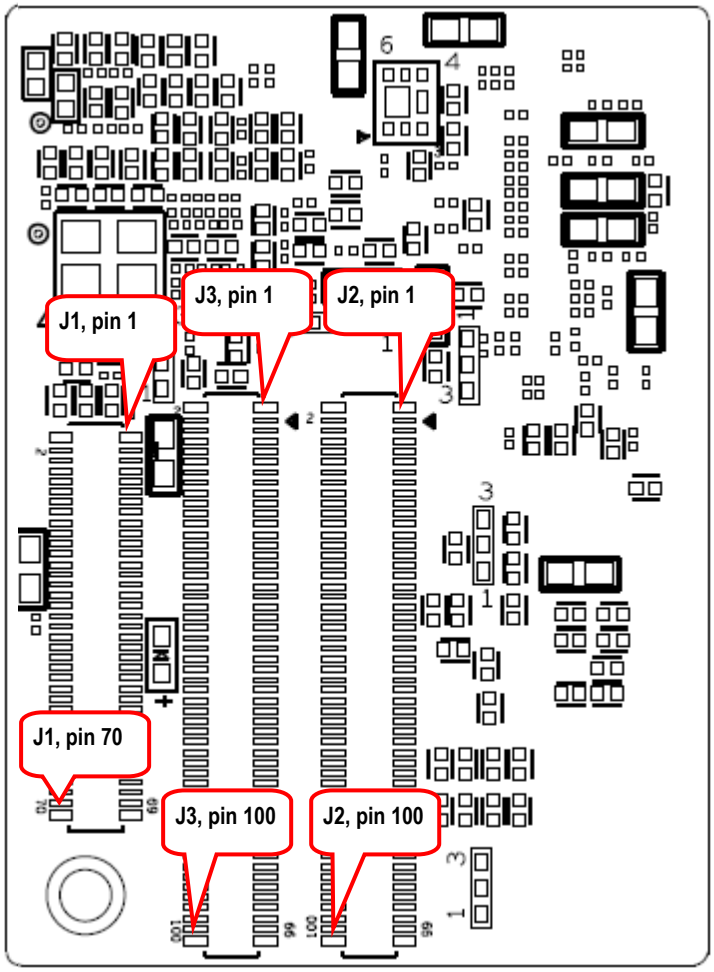


Figure 2 – EACOM Board Pin Numbering, Bottom Side

3.2 Pin Assignment

This section describes the pin assignment of the board, with the following columns:

Connector and Pin number	The pin numbers are listed in consecutive order. Odd pin numbers are on one row and even numbers on the other row.
Non-i.MX 7Dual signals	Lists signals that are not directly connected to the i.MX 7Dual SoC. These signals are typically related to powering and connected to the on-board Power Management IC (PMIC), BD71815GW.
i.MX 7Dual Ball Name	The name of the ball of the i.MX 7Dual SoC that is connected to this pin.
Alternative Pin Function	Information if the signals is a dedicated interface or a general pin that can multiples different signals. See separate Excel sheet for details about available multiplexing alternatives.
Notes	When relevant, the preferred pin function is listed.

The table below lists the pins on expansion connector J1 (70-pos connector).

J1 Pin Number	Non-i.MX 7Dual Signals	i.MX 7Dual Ball Name	Alternative Pin Function?	Notes
1	GND			
2	VSYS			System supply voltage, see chapter 6 for more details.
3		USB_OTG1_ID	No	
4	VSYS			System supply voltage, see chapter 6 for more details.
5	GND			
6	VSYS			System supply voltage, see chapter 6 for more details.
7	Not connected			
8	VDD_3P3			3.3V voltage rail, see chapter 6 for more details.
9	GND			
10	VDD_3P3			3.3V voltage rail, see chapter 6 for more details.
11	GND			
12	VDD_1P8			1.8V voltage rail, see chapter 6 for more details.
13	GND			
14	DCIN			Charge voltage rail, see chapter 6 for more details.
15	GND			
16		USB_OTG1_DP	No	
17		ONOFF	No	
18		USB_OTG1_DN	No	
19		GPIO1_IO04	Yes	LPSR capable pin
20		USB_OTG1_VBUS	No	
21		GPIO1_IO05	Yes	LPSR capable pin
22		UART2_RXD	Yes	
23	EXT_RTC_VBAT			Supply voltage to keep PMIC and RTC functioning during standby, see chapter 6 for more details.
24		SAI2_RXD	Yes	
25		GPIO1_IO15	Yes	LPSR capable pin

26	SAI2_TXD	Yes	
27	UART2_TXD	Yes	
28	GPIO1_IO10	Yes	LPSR capable pin
29	ADC1_IN0	No	Note: Maximum input voltage 1.8V
30	GPIO1_IO12	Yes	LPSR capable pin
31	E2PROM_WP		Should be left open (will write protect the on-board parameter storage E2PROM), or connected to GND (will enable writes to the on-board parameter storage E2PROM AND place the i.MX 7Dual SoC in USB OTG boot mode after a power cycle).
32	GPIO1_IO13	Yes	LPSR capable pin
33	GPIO1_IO01	Yes	LPSR capable pin
34	GPIO1_IO14	Yes	LPSR capable pin
35	GPIO1_IO11	Yes	LPSR capable pin
36	POR_B		Reset (open drain) output, active low. Driven low during reset. 10K pull-up resistor to IO voltage. Signal can be pulled low (open drain) externally to reset the board.
37	GPIO1_IO02	Yes	LPSR capable pin
38	ADC1_IN1	No	Note: Maximum input voltage 1.8V
39	GPIO1_IO03	Yes	LPSR capable pin
40	ADC1_IN2	No	Note: Maximum input voltage 1.8V
41	I2C1_SCL	No	Dedicated I2C channel (connects internally to PMIC and E2PROM)
42	SD2_RESET	Yes	
43	I2C1_SDA	No	Dedicated I2C channel (connects internally to PMIC and E2PROM)
44	GPIO1_IO06	Yes	LPSR capable pin
45	I2C2_SCL	Yes	
46	UART1_TXD	Yes	
47	I2C2_SDA	Yes	
48	GPIO1_IO07	Yes	LPSR capable pin
49	ADC1_IN3	No	Note: Maximum input voltage 1.8V
50	SAI1_RXD	Yes	
51	SD2_WP	Yes	
52	SAI1_TXC	Yes	
53	ECSPI1_SS0	Yes	
54	SAI1_TXFS	Yes	
55	ECSPI1_SCLK	Yes	
56	SAI1_TXD	Yes	
57	ECSPI1_MOIS	Yes	
58	SD2_CLK	Yes	
59	ECSPE1_MISO	Yes	
60	SD2_CD	Yes	
61	UART1_RXD	Yes	
62	SD2_CMD	Yes	

63		SAI2_TXC	Yes	
64		SD2_DATA2	Yes	
65		SAI2_TXFS	Yes	
66		SD2_DATA0	Yes	
67		SAI1_MCLK	Yes	
68		SD2_DATA3	Yes	
69				Not connected
70		SD2_DATA1	Yes	

The table below lists the pins on expansion connector J2 (100-pos connector).

J2 Pin Number	Non-i.MX 7Dual Signals	i.MX 7Dual Ball Name	Alternative Pin Function?	Notes
1		MIPI_CSI_CLK_P	No	
2	NVCC_JTAG			Debug interface voltage level
3		MIPI_CSI_CLK_N	No	
4		JTAG_TMS	No	
5	GND			
6		JTAG_TCK	No	
7		MIPI_CSI_D0_P	No	
8		JTAG_TDO	No	
9		MIPI_CSI_D0_N	No	
10		JTAG_TDI	No	
11	GND			
12		JTAG_TRST	No	
13		MIPI_CSI_D1_P	No	
14		JTAG_MOD	No	
15		MIPI_CSI_D1_N	No	
16	GND			
17	GND			
18	VO1_3P3			LDO1, 3.3V voltage rail, see chapter 6 for more details.
19		MIPI_DSI_CLK_P	No	
20	VO2_3P3			LDO2, 3.3V voltage rail, see chapter 6 for more details.
21		MIPI_DSI_ CLK_N	No	
22	GND			
23	GND			
24	V04_3P3			LDO4, 3.3V voltage rail, see chapter 6 for more details.
25		MIPI_DSI_D0_P	No	
26	GND			
27		MIPI_DSI_ D0_N	No	
28		EPDC_D00	Yes	
29	GND			
30		EPDC_D01	Yes	

31		MIPI_DSI_ D1_P	No
32		EPDC_D02	Yes
33		MIPI_DSI_ D1_N	No
34		EPDC_D03	Yes
35	GND		
36		EPDC_D04	Yes
37		PCIE_REFCLK_P	No
38		EPDC_D05	Yes
39		PCIE_REFCLK_N	No
40		EPDC_D06	Yes
41	GND		
42		EPDC_D07	Yes
43		PCIE_REFCLKOUT_P	No
44		EPDC_D08	Yes
45		PCIE_REFCLKOUT_N	No
46		EPDC_D09	Yes
47	GND		
48		EPDC_D10	Yes
49		PCIE_RX_P	No
50		EPDC_D11	Yes
51		PCIE_RX_N	No
52		EPDC_D12	Yes
53	GND		
54		EPDC_D13	Yes
55		PCIE_TX_P	No
56		EPDC_D14	Yes
57		PCIE_TX_N	No
58		EPDC_D15	Yes
59	GND		
60		EPDC_SDCE0	Yes
61		USB_OTG2_DP	No
62		EPDC_SDCE1	Yes
63		USB_OTG2_DN	No
64		EPDC_SDCE2	Yes
65	GND		
66		EPDC_SDCE3	Yes
67		USB_OTG2_VBUS	No
68		EPDC_SDCLK	Yes
69		USB_OTG2_ID	No
70		EPDC_SDLE	Yes
71		ENET1_TD0	Yes
72		EPDC_SDOE	Yes

73		ENET1_TD1	Yes
74		EPDC_SDSHR	Yes
75		ENET1_TD2	Yes
76		EPDC_GDCLK	Yes
77		ENET1_TD3	Yes
78		EPDC_GDOE	Yes
79		ENET1_TXC	Yes
80		EPDC_GDRL	Yes
81		ENET1_TX_CTL	Yes
82		EPDC_GDSP	Yes
83		ENET1_TX_CLK	Yes
84		EPDC_PWRCOM	Yes
85		ENET1_RD0	Yes
86		EPDC_PWRSTAT	Yes
87		ENET1_RD1	Yes
88		EPDC_BDR0	Yes
89		ENET1_RD2	Yes
90		EPDC_BDR1	Yes
91		ENET1_RD3	Yes
92		ENET1_COL	Yes
93		ENET1_RXC	Yes
94		ENET1_CRS	Yes
95		ENET1_RX_CTL	Yes
96	GND		
97		ENET1_RX_CLK	Yes
98		CCM_CLK1_N	No
99	GND		
100		CCM_CLK1_P	No

The table below lists the pins on expansion connector J3 (100-pos connector).

J3 Pin Number	Non-i.MX 7Dual Signals	i.MX 7Dual Ball Name	Alternative Pin Function?	Notes
1	DCIN			Charge voltage rail, see chapter 6 for more details.
2	VBAT_EXT_TS			Battery pack thermistor voltage sense, see chapter 6 for more details. If not used, connect to ground via 10K resistor.
3	DCIN			Charge voltage rail, see chapter 6 for more details.
4	EXT_BATTM			Current sense input (ground side, see chapter 6 for more details. If not used, connect to ground.
5	DCIN			Charge voltage rail, see chapter 6 for more details.
6	EXT_BATTP			Current sense input (battery pack), see chapter 6 for more details. If not used, connect to ground.
7	DCIN			Charge voltage rail, see chapter 6 for more details.
8	VBAT_EXT			Battery connection, see chapter 6 for more details.

9	VSYS			System supply voltage, see chapter 6 for more details.
10	VBAT_EXT			Battery connection, see chapter 6 for more details.
11	VSYS			System supply voltage, see chapter 6 for more details.
12	VBAT_EXT			Battery connection, see chapter 6 for more details.
13	VDD_IO			IO voltage rail, see chapter 6 for more details.
14	VBAT_EXT			Battery connection, see chapter 6 for more details.
15	VDD_IO			IO voltage rail, see chapter 6 for more details.
16	VBAT_EXT			Battery connection, see chapter 6 for more details.
17	GND			
18	WLED_P			Positive voltage for white LEDs, see chapter 6 for more details.
19		LCD1_DATA0	Yes	
20	WLED_N			Negative voltage for white LEDs, see chapter 6 for more details.
21		LCD1_DATA1	Yes	
22	GND			
23		LCD1_DATA2	Yes	
24		I2C3_SCL	Yes	
25		LCD1_DATA3	Yes	
26		I2C3_SDA	Yes	
27	GND			
28		I2C4_SCL	Yes	
29		LCD1_DATA4	Yes	
30		I2C4_SDA	Yes	
31		LCD1_DATA5	Yes	
32		ECSPI2_SCLK	Yes	
33		LCD1_DATA6	Yes	
34		ECSPI2_MISO	Yes	
35		LCD1_DATA7	Yes	
36		ECSPI2_MOSI	Yes	
37	GND			
38		ECSPI2_SS0	Yes	
39		LCD1_DATA8	Yes	
40		UART3_RXD	Yes	
41		LCD1_DATA9	Yes	
42		UART3_TXD	Yes	
43		LCD1_DATA10	Yes	
44		UART3_RTS	Yes	
45		LCD1_DATA11	Yes	
46		UART3_CTS	Yes	
47	GND			
48		SAI1_RXC	Yes	
49		LCD1_DATA12	Yes	

50		SAI1_RXFS	Yes	
51		LCD1_DATA13	Yes	
52	GND			
53		LCD1_DATA14	Yes	
54		GPIO1_IO09	Yes	LPSR capable pin. Connected to PMIC interrupt signal
55		LCD1_DATA15	Yes	
56	VO4_PWR_EN			LDO4 enable signal, see chapter 6 for more details.
57	GND			
58		GPIO1_IO08	Yes	LPSR capable pin
59		LCD1_DATA16	Yes	
60	SD1_VSELECT			SD1 voltage select. High level = 1.8V, Low level = 3.3V.
61		LCD1_DATA17	Yes	
62	EXT_RST_IN			Reset input, active low. Pull signal low to reset PMIC. No need to pull signal high externally.
63		LCD1_DATA18	Yes	
64	PMIC_GPIO			General purpose output from PMIC, see chapter 6 for more details.
65		LCD1_DATA19	Yes	
66	LED_EXT_CHG			Charging status indication output (open drain), see chapter 6 for more details.
67	GND			
68	LED_EXT_RDY			PMIC ready output, see chapter 6 for more details.
69		LCD1_DATA20	Yes	
70		BOOT_MODE1	No	
71		LCD1_DATA21	Yes	
72		SNVS_TAMPER0	No	
73		LCD1_DATA22	Yes	
74		SNVS_TAMPER1	No	
75		LCD1_DATA23	Yes	
76		SNVS_TAMPER2	No	
77	GND			
78		SD1_CLK	Yes	Signal voltage level defined by NVCC_SD1, see pin 92 in this connector.
79		LCD1_ENABLE	Yes	
80		SD1_CMD	Yes	Signal voltage level defined by NVCC_SD1, see pin 92 in this connector.
81		LCD1_HSYNC	Yes	
82	GND			
83		LCD1_VSYNC	Yes	
84		SD1_DATA0	Yes	Signal voltage level defined by NVCC_SD1, see pin 92 in this connector.
85		LCD1_RESET	Yes	
86		SD1_DATA1	Yes	Signal voltage level defined by NVCC_SD1, see pin 92 in this connector.
87	GND			

88		SD1_DATA2	Yes	Signal voltage level defined by NVCC_SD1, see pin 92 in this connector.
89		LCD1_CLK	Yes	
90		SD1_DATA3	Yes	Signal voltage level defined by NVCC_SD1, see pin 92 in this connector.
91	GND			
92	NVCC_SD1			Output supply voltage rail for SD interface (1.8V or 3.3V). Should only supply the SD1 interface.
93		HSIC_DATA	No	
94		SD1_CD	Yes	Signal voltage level defined by NVCC_SD1, see pin 92 in this connector.
95		HSIC_STROBE	No	
96		SD1_WP	Yes	Signal voltage level defined by NVCC_SD1, see pin 92 in this connector.
97	GND			
98		SD1_RESET	Yes	Signal voltage level defined by NVCC_SD1, see pin 92 in this connector.
99		CCM_CLK2	No	
100	GND			

4 Pin Mapping

4.1 Functional Multiplexing on I/O Pins

There are a lot of different peripherals inside the i.MX 7Dual SoC. Many of these peripherals are connected to the IOMUX block, that allows the I/O pins to be configured to carry one of many (up to nine different) alternative functions. This leave great flexibility to select a function multiplexing scheme for the pins that satisfy the interface need for a particular application.

Some interfaces with specific voltage levels/drivers/transceivers have dedicated pins, like ADC, PCIe, MIPI-DSI, MIPI-CSI and USB. i.MX 7Dual pins carrying these signals do not have any functional multiplexing possibilities. These interfaces are fixed.

When the *iMX7 Dual uCOM Board* is used in combination with the *uCOM Adapter Board* (see chapter 7 for details about this board), a specific pin allocation has been done. The Linux BSP initialize the pins according to this pin allocation. There is no need to keep this pin allocation for custom boards. In general there are no restrictions to select alternative pin multiplexing schemes.

Functional multiplexing is normally controlled via the Linux BSP. It can also be done directly via register `IOMUXC_LPSR_SW_MUX_CTL_PAD_xxx / IOMUXC_SW_MUX_CTL_PAD_xxx` where `xxx` is the name of the i.MX 7Dual pin. For more information about the register settings, see the *i.MX 7Dual Application Processor Reference Manual* from NXP.

Note that input functions that are available on multiple pins will require control of an input multiplexer. This is controlled via register `IOMUXC_xxx_SELECT_INPUT` where `xxx` is the name of the input function. Again, for more information about the register settings, see the *i.MX 7Dual Application Processor Reference Manual* from NXP.

4.1.1 Alternative I/O Function List

There is an accompanying Excel document that lists all alternative functions for each available I/O pin. The reset state is shown as well as the *uCOM Adapter board*/EACOM function allocation. The reset state is typically GPIO, ALT5 function, except for the GPIO1_IO01-15 signals that are ALT0 functions, but that is the GPIO function.

4.2 I/O Pin Control

Each pin also has an additional control register for configuring input hysteresis, pull up/down resistors, push-pull/open-drain driving, drive strength and more. Also in this case, configuration is normally done via the Linux BSP but it is possible to directly access the control registers, which are called `IOMUXC_SW_PAD_CTL_PAD_xxx` where `xxx` is the name of the i.MX 7Dual pin. For more information about the register settings, see the *i.MX 7Dual Application Processor Reference Manual* from NXP.

As a general recommendation, select slow slew rate and lowest drive strength (that still result in acceptable signal edges for the system) in order to reduce problems with EMC.

Note that many pins (but not all) are configured as GPIO inputs, with a 100Kohm pull-down resistor, after reset. When the bootloader (typically u-boot) executes it is possible to reconfigure the pins.

5 Interface Description

This chapter lists details about all different interfaces. The **i.MX 7Dual datasheet and user manual should always be consulted** for details about different functions and interfaces. Many interfaces are multiplexed on different pins and not available simultaneously.

Note that this chapter do not list all peripheral functions available on the i.MX7 Dual SoC. Only the ones related to the EACOM specification - note that the uCOM board is not an EACOM compatible board, but in combination with the *uCOM Adapter Board* it is. Therefore there are references to the EACOM specification in this chapter's text.

For all available interfaces, consult *Chapter 8 - Chip IO and pinmux, Section 8.1 External Signals and Pin Multiplexing* in NXP's *i.MX 7Dual Applications Processor Reference Manual* (document id: IMX7DRM).

Example of peripheral blocks **not** listed in this chapter are listed below (see document IMX7DRM for details). Some of the blocks have multiple instances.

- CCM - Clock Controller Module
  Besides internal clocks, this peripheral can generate external clocks.
- EIM - External Interface Module
  This peripheral provides asynchronous access to devices with SRAM-like interface and synchronous access to devices with NOR-Flash-like or PSRAM-like interface.
- EPDC - Electrophoretic Display Controller
  This peripheral is a controller for E-INK™ displays.
- FTM - Flex Timer
  This peripheral is a flexible timer that supports input capture and can generate PWM signals.
- GPT - General Purpose Timer
  This peripheral is a 32-bit general purpose timer with capture and trigger functions.
- KPP - Keypad Port
  This peripheral provides a keypad matrix interface.
- SDMA - Smart Direct Memory Access Controller
  This peripheral provides fast data transfers between peripheral I/O devices and internal/external memories
- SIM - Subscriber Identification Module
  This peripheral provides an interface to SIM cards and is compatible with ISO/IEC 7816-3.
- WDOG - Watchdog Timer
  This peripheral implements a watchdog timer.

There is an accompanying Excel document that lists all alternative functions for each available I/O pin.

5.1 Camera Interfaces

This section lists signals related to CMOS Sensor Interface (CSI) functions.

There are two camera interfaces, one parallel and one serial (MIPI-CSI2) input interface. One at a time is multiplexed to the CSI unit. The picture below illustrates the multiplexing.

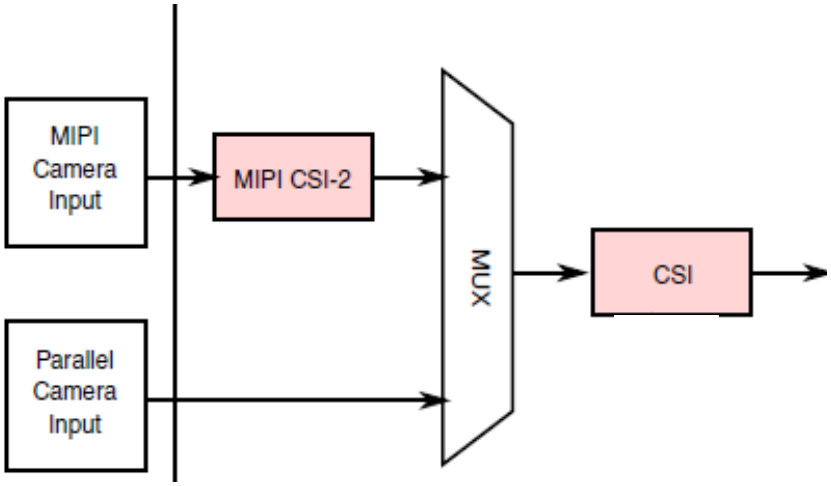


Figure 3 – Camera Port Multiplexing Scheme

5.1.1 Parallel Camera Interface

There is no pre-allocation interface for the parallel camera interface (CSI). All SCI signals are available via pin-multiplexing.

The table below lists the alternative pin locations for the parallel camera interface.

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	i.MX 7 Ball Name	I/O	Description	Remarks
J3, PIN 61	LCD_R1	LCD1_DATA17	I	Data Sensor Signal	Alternative location for CSI_DATA00
J3, PIN 59	LCD_R0	LCD1_DATA16	I	Data Sensor Signal	Alternative location for CSI_DATA01
J1, PIN 55	SPI-A_CLK	ECSPI1_SCLK	I	Data Sensor Signal	Alternative location for CSI_DATA02
J3, PIN 55	LCD_G7	LCD1_DATA15	I	Data Sensor Signal	Alternative location for CSI_DATA02
J1, PIN 57	SPI-A_MOSI	ECSPI1_MOSI	I	Data Sensor Signal	Alternative location for CSI_DATA03
J3, PIN 53	LCD_G6	LCD1_DATA14	I	Data Sensor Signal	Alternative location for CSI_DATA03
J1, PIN 59	SPI-A_MISO	ECSPI1_MISO	I	Data Sensor Signal	Alternative location for CSI_DATA04
J3, PIN 51	LCD_G5	LCD1_DATA13	I	Data Sensor Signal	Alternative location for CSI_DATA04
J1, PIN 53	SPI-A_SSEL	ECSPI1_SS0	I	Data Sensor Signal	Alternative location for CSI_DATA05
J3, PIN 49	LCD_G4	LCD1_DATA12	I	Data Sensor Signal	Alternative location for CSI_DATA05
J3, PIN 32	SPI-B_CLK	ECSPI2_SCLK	I	Data Sensor Signal	Alternative location for CSI_DATA06
J3, PIN 45	LCD_G3	LCD1_DATA11	I	Data Sensor Signal	Alternative location for CSI_DATA06
J3, PIN 36	SPI-B_MOSI	ECSPI2_MOSI	I	Data Sensor Signal	Alternative location for CSI_DATA07
J3, PIN 43	LCD_G2	LCD1_DATA10	I	Data Sensor Signal	Alternative location for CSI_DATA07
J3, PIN 34	SPI-B_MISO	ECSPI2_MISO	I	Data Sensor Signal	Alternative location for CSI_DATA08
J3, PIN 41	LCD_G1	LCD1_DATA09	I	Data Sensor Signal	Alternative location for CSI_DATA08
J3, PIN 38	SPI-B_SSEL	ECSPI2_SS0	I	Data Sensor Signal	Alternative location for CSI_DATA09
J3, PIN 39	LCD_G0	LCD1_DATA08	I	Data Sensor Signal	Alternative location for CSI_DATA09

J3, PIN 75	LCD_R7	LCD1_DATA23	I	Data Sensor Signal	Alternative location for CSI_DATA10
J3, PIN 73	LCD_R6	LCD1_DATA22	I	Data Sensor Signal	Alternative location for CSI_DATA11
J3, PIN 71	LCD_R5	LCD1_DATA21	I	Data Sensor Signal	Alternative location for CSI_DATA12
J3, PIN 69	LCD_R4	LCD1_DATA20	I	Data Sensor Signal	Alternative location for CSI_DATA13
J3, PIN 65	LCD_R3	LCD1_DATA19	I	Data Sensor Signal	Alternative location for CSI_DATA14
J3, PIN 63	LCD_R2	LCD1_DATA18	I	Data Sensor Signal	Alternative location for CSI_DATA15
J3, PIN 89	LCD_CLK	LCD1_CLK	I	Data Sensor Signal	Alternative location for CSI_DATA16
J3, PIN 79	LCD_ENABLE	LCD1_ENABLE	I	Data Sensor Signal	Alternative location for CSI_DATA17
J3, PIN 81	LCD_HSYNC	LCD1_HSYNC	I	Data Sensor Signal	Alternative location for CSI_DATA18
J3, PIN 83	LCD_VSYNC	LCD1_VSYNC	I	Data Sensor Signal	Alternative location for CSI_DATA19
J3, PIN 19	LCD_B0	LCD1_DATA00	I	Data Sensor Signal	Alternative location for CSI_DATA20
J3, PIN 21	LCD_B1	LCD1_DATA01	I	Data Sensor Signal	Alternative location for CSI_DATA21
J3, PIN 23	LCD_B2	LCD1_DATA02	I	Data Sensor Signal	Alternative location for CSI_DATA22
J3, PIN 25	LCD_B3	LCD1_DATA03	I	Data Sensor Signal	Alternative location for CSI_DATA23
J3, PIN 85	GPIO7	LCD1_RESET	I	CSI Field Signal	Alternative location for CSI_FIELD
J3, PIN 26	HDMI/I2C-C_SDA	I2C3_SDA	I	Horizontal Sync	Alternative location for CSI_HSYNC **Note** that there is a 2.2Kohm pull-up resistor on this signal.
J3, PIN 31	LCD_B5	LCD1_DATA05	I	Horizontal Sync	Alternative location for CSI_HSYNC
J3, PIN 30	COM specific	I2C4_SDA	O	Master Clock	Alternative location for CSI_MCLK
J3, PIN 35	LCD_B7	LCD1_DATA07	O	Master Clock	Alternative location for CSI_MCLK
J3, PIN 28	COM specific	I2C4_SCL	I	Pixel Clock	Alternative location for CSI_PIXCLK
J3, PIN 33	LCD_B6	LCD1_DATA06	I	Pixel Clock	Alternative location for CSI_PIXCLK
J3, PIN 24	HDMI/I2C-C_SCL	I2C3_SCL	I	Vertical Sync	Alternative location for CSI_VSYNC **Note** that there is a 2.2Kohm pull-up resistor on this signal.
J3, PIN 29	LCD_B4	LCD1_DATA04	I	Vertical Sync	Alternative location for CSI_VSYNC

The CSI can support connection with the sensor as follows.

- To connect with a 8-bit sensor, the sensor data interface should connect to CSI_DATA[9:2].
- To connect with a 10-bit sensor, the sensor data interface should connect to CSI_DATA[9:0].
- To connect with a 16-bit sensor, the sensor data interface should connect to CSI_DATA[15:0].
- To connect with two 8-bit sensors, the sensor data interfaces should connect to CSI_DATA[7:0] and CSI_DATA[15:8], respectively.

The CSI input data format mapping is shown in the table below.

Internal CSI Signal Name	TVdecoder YCbCr 1 cycle	RGB888 1 cycle	RGB888/ YUV4444 3 cycles	RGB666 1 cycle	RGB565 1 cycle	YCbCr422 1 cycle	YCbCr422 2 cycles	Generic 10 bit	CCIR656
CSI_DATA23	Y7	R7		R5					
CSI_DATA22	Y6	R6		R4					
CSI_DATA21	Y5	R5		R3					
CSI_DATA20	Y4	R4		R2					
CSI_DATA19	Y3	R3		R1					

CSI_DATA18	Y2	R2		R0					
CSI_DATA17	Y1	R1		Y5					
CSI_DATA16	Y0	R0		Y4					
CSI_DATA15	Cb7	G7		G5	R4	Y7			
CSI_DATA14	Cb6	G6		G4	R3	Y6			
CSI_DATA13	Cb5	G5		G3	R2	Y5			
CSI_DATA12	Cb4	G4		G2	R1	Y4			
CSI_DATA11	Cb3	G3		G1	R0	Y3			
CSI_DATA10	Cb2	G2		G0	G5	Y2			
CSI_DATA09	Cb1	G1	R7/G7/B7	G5	G4	Y1	Y7/C7	Ge9	C7/Y7
CSI_DATA08	Cb0	G0	R6/G6/B6	G4	G3	Y0	Y6/C6	Ge8	C6/Y6
CSI_DATA07	Cr7	B7	R5/G5/B5	B5	G2	C7	Y5/C5	Ge7	C5/Y5
CSI_DATA06	Cr6	B6	R4/G4/B4	B4	G1	C6	Y4/C4	Ge6	C4/Y4
CSI_DATA05	Cr5	B5	R3/G3/B3	B3	G0	C5	Y3/C3	Ge5	C3/Y3
CSI_DATA04	Cr4	B4	R2/G2/B2	B2	B4	C4	Y2/C2	Ge4	C2/Y2
CSI_DATA03	Cr3	B3	R1/G1/B1	B1	B3	C3	Y1/C1	Ge3	C1/Y1
CSI_DATA02	Cr2	B2	R0/G0/B0	B0	B2	C2	Y0/C0	Ge2	C0/Y0
CSI_DATA01	Cr1	B1		B5	B1	C1		Ge1	
CSI_DATA00	Cr0	B0		B4	B0	C0		Ge0	

5.1.2 Serial Camera Interface

This section lists signals for the serial camera interface, also called MIPI-CSI2.

The *EACOM Board specification* defines an serial camera interface, MIPI-CSI2 with up to 2 lanes. The table below lists the pin assignment according to *EACOM Board specification*.

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	i.MX 7 Ball Name	I/O	Description	Remarks
J2, PIN 1	CSI_CLK_P	MIPI_CSI_CLK0P	I	Positive D-Phy differential clock line Receiver input	
J2, PIN3	CSI_CLK_N	MIPI_CSI_CLK0N	I	Negative D-Phy differential clock line Receiver input	
J2, PIN7	CSI_D0_P	MIPI_CSI_D0P	I	Positive D-Phy differential data line Receiver input , Lane 0	
J2, PIN9	CSI_D0_N	MIPI_CSI_D0N	I	Negative D-Phy differential data line Receiver input , Lane 0	
J2, PIN13	CSI_D1_P	MIPI_CSI_D1P	I	Positive D-Phy differential data line Receiver input , Lane 1	
J2, PIN15	CSI_D1_N	MIPI_CSI_D1N	I	Negative D-Phy differential data line Receiver input , Lane 1	

5.2 Display Interfaces

This section lists signals related to display output interfaces; parallel RGB (Enhanced LCD Interface - eLCDIF) and MIPI-DSI transmitter.

The i.MX 7Dual SoC has a display and graphics subsystem with dedicated components:

- PXP pixel pipeline: pixel/image processing engine for LCD display
- LCD interface (LCDIF), which is 24-bit parallel RGB LCD interface
- CSI interface with up to 24-bit parallel interface for image sensor
- EPDC interface for E-INK™ displays. This interface will not be presented further in this document. For more details, see NXP document IMX7DRM.

The picture below shows the high-level structure of the display and graphics subsystem. It picture comes from chapter 13 - Multimedia in the IMX7DRM.

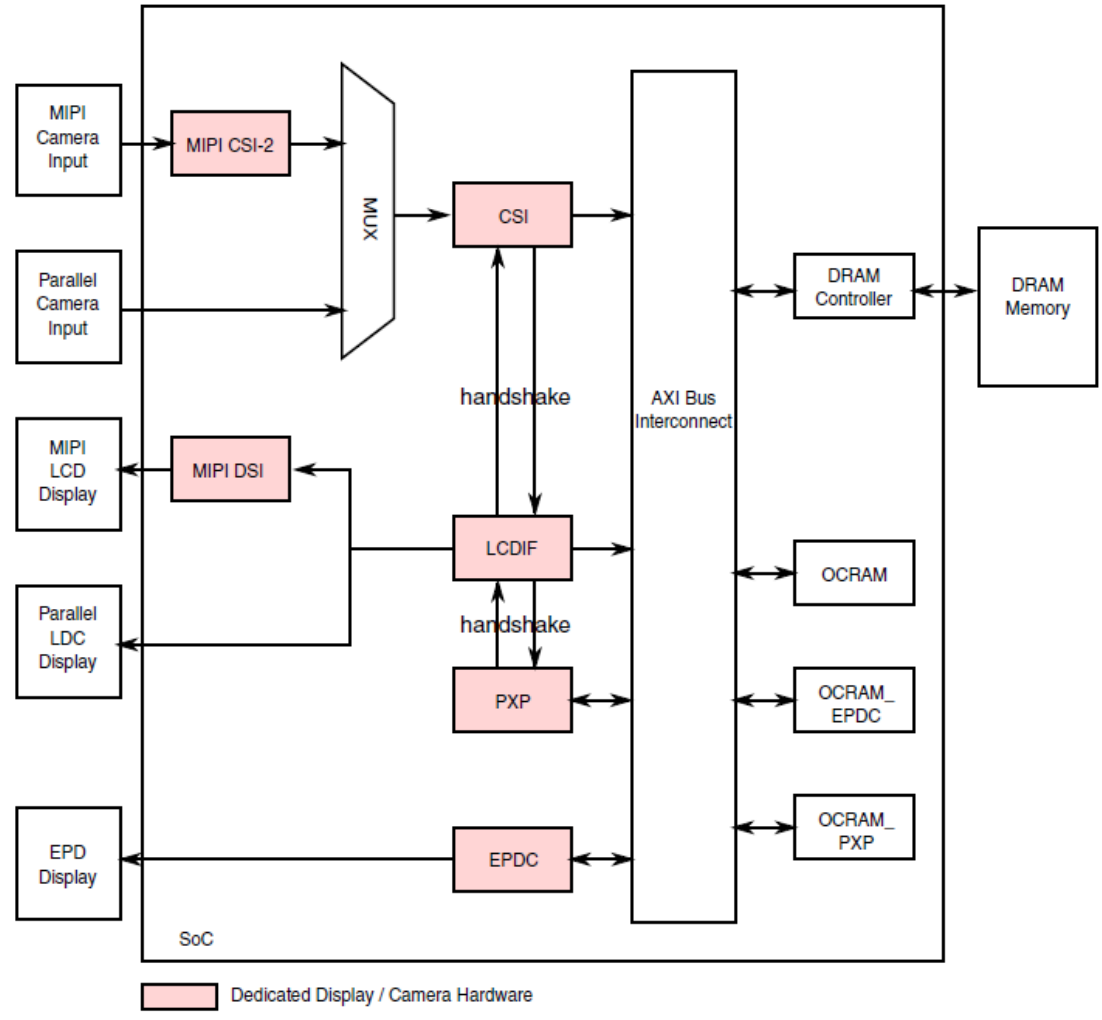


Figure 4 – Structure of Display and Graphics Subsystem

The *i.MX 7Dual COM board* has allocated pins (according to the *EACOM Board specification*) for one serial camera input, a parallel RGB LCD output and a serial display output. The EACOM pins for LVDS and HDMI output interfaces are not allocated since the i.MX 7Dual SoC does not support these interfaces. The serial camera interface is presented in section 5.1 .

The *EACOM Board specification* has allocated some additional support signals that are typically needed to implement a display interface. The table below list these signals. These are common for all display interfaces.

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	i.MX 7 Ball Name	I/O	Description	Remarks
J1, PIN 33	BL_PWM	GPIO1_IO01	O	PWM signal to control backlight contrast.	Signal is connected to PWM1_OUT
J2, PIN 76	BL_PWR_EN	EPDC_GDCLK	O	Power control for backlight. Active high	Signal is connected to GPIO2_IO24
J2, PIN 78	DISP_PWR_EN	EPDC_GDOE	O	Power control for LCD power supply. Active high	Signal is connected to GPIO2_IO25
J2, PIN 80	TP_IRQ	EPDC_GDRL	I	Interrupt from touch controller	Signal is connected to GPIO2_IO26
J2, PIN 82	TP_RST	EPDC_GDSP	O	Reset signal to touch controller. Active low	Signal is connected to GPIO2_IO27
J1, PIN 41	I2C-A_SCL	I2C1_SCL	I/O	Clock signal of I2C channel A	It is recommended to connect the RGB LCD touch controller (if I2C interface) to this channel.
J1, PIN 43	I2C-A_SDA	I2C1_SDA	I/O	Data signal of I2C channel A	It is recommended to connect the RGB LCD touch controller (if I2C interface) to this channel.
J1, PIN 45	I2C-B_SCL	I2C2_SCL	I/O	Clock signal of I2C channel B	A touch controller can be connected to this I2C channels also, but will require adjustment in Linux BSP.
J1, PIN 47	I2C-B_SDA	I2C2_SDA	I/O	Data signal of I2C channel B	A touch controller can be connected to this I2C channels also, but will require adjustment in Linux BSP.
J3, PIN 24	I2C-C_SCL	I2C3_SCL	I/O	Clock signal of I2C channel C	A touch controller can be connected to this I2C channels also, but will require adjustment in Linux BSP.
J3, PIN 26	I2C-C_SDA	I2C3_SDA	I/O	Data signal of I2C channel C	A touch controller can be connected to this I2C channels also, but will require adjustment in Linux BSP.

5.2.1 Parallel RGB LCD Interface

This section lists signals for the parallel RGB LCD interface.

The parallel RGB LCD interface with 24-bit color depth. It can for example drive 1080p (1920x1080 pixel) at 60 fps.

The parallel RGB LCD interface is ideal for smaller, lower resolution displays. Note that due to EMI MIPI-DSI might be better choices of interface for high resolution displays.

Note that both the parallel RGB and MIPI-DSI interfaces will carry the same display output data. Only one display output data stream is possible at a time.

The *EACOM Board specification* defines a 24-bit parallel LCD interface. The table below lists the pin assignment according to *EACOM Board specification*. For best portability it is recommended to always have the LCD interface running in 24-bit mode. If less bits are needed in a specific LCD implementation the LSB bits of each color is just ignored, see the three rightmost columns.

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	i.MX 7 Ball Name	I/O	Color Config. for 16-bit 565RGB	Color Config. for 18-bit 666RGB	Color Config. for 16-bit 565RGB if interface set to 24-bit	Color Config. for 18-bit 666RGB if interface set to 24-bit	Color Config. for 24-bit 888RGB
J3, PIN 19	LCD_DATA00	LCD1_DATA00	O	B0	B0			B0
J3, PIN 21	LCD_DATA01	LCD1_DATA01	O	B1	B1			B1
J3, PIN 23	LCD_DATA02	LCD1_DATA02	O	B2	B2		B2	B2
J3, PIN 25	LCD_DATA03	LCD1_DATA03	O	B3	B3	B3	B3	B3
J3, PIN 29	LCD_DATA04	LCD1_DATA04	O	B4	B4	B4	B4	B4
J3, PIN 31	LCD_DATA05	LCD1_DATA05	O	G0	B5	B5	B5	B5
J3, PIN 33	LCD_DATA06	LCD1_DATA06	O	G1	G0	B6	B6	B6
J3, PIN 35	LCD_DATA07	LCD1_DATA07	O	G2	G1	B7	B7	B7
J3, PIN 39	LCD_DATA08	LCD1_DATA08	O	G3	G2			G0
J3, PIN 41	LCD_DATA09	LCD1_DATA09	O	G4	G3			G1
J3, PIN 43	LCD_DATA10	LCD1_DATA10	O	G7	G4	G2	G2	G2
J3, PIN 45	LCD_DATA11	LCD1_DATA11	O	R0	G5	G3	G3	G3
J3, PIN 49	LCD_DATA12	LCD1_DATA12	O	R1	R0	G4	G4	G4
J3, PIN 51	LCD_DATA13	LCD1_DATA13	O	R2	R1	G5	G5	G5
J3, PIN 53	LCD_DATA14	LCD1_DATA14	O	R3	R2	G6	G6	G6
J3, PIN 55	LCD_DATA15	LCD1_DATA15	O	R4	R3	G7	G7	G7
J3, PIN 59	LCD_DATA16	LCD1_DATA16	O		R4			R0
J3, PIN 61	LCD_DATA17	LCD1_DATA17	O		R5			R1
J3, PIN 63	LCD_DATA18	LCD1_DATA18	O				R2	R2
J3, PIN 65	LCD_DATA19	LCD1_DATA19	O			R3	R3	R3
J3, PIN 69	LCD_DATA20	LCD1_DATA20	O			R4	R4	R4
J3, PIN 71	LCD_DATA21	LCD1_DATA21	O			R5	R5	R5
J3, PIN 73	LCD_DATA22	LCD1_DATA22	O			R6	R6	R6
J3, PIN 75	LCD_DATA23	LCD1_DATA23	O			R7	R7	R7
J3, PIN 81	LCD_HSYNC	LCD1_HSYNC	O	Horizontal (line) synchronization				
J3, PIN 83	LCD_VSYNC	LCD1_VSYNC	O	Vertical (frame) synchronization				
J3, PIN 79	LCD_ENABLE	LCD1_ENABLE	O	Data enable				
J3, PIN 89	LCD_CLK	LCD1_CLK	O	Pixel (dot) clock				

Note that the eLCDIF peripheral in the i.MX 7Dual SoC also supports MPU-like display interfaces. See chapter 13, section 13.2 in IMX7DRM for more details.

5.2.2 MIPI-DSI Interface

This section lists signals for the MIPI-DSI interface. The interface supports display resolutions up to 1400x1050 pixels (SXGA+) with 24-bit resolution at 60 fps.

Note that both the parallel RGB and MIPI-DSI interfaces will carry the same display output data. Only one display output data stream is possible at a time.

The *EACOM Board specification* has not allocated pins for this interface, since it is mostly used in very high volume applications (where COM boards are not so commonly used). The MIPI-DSI interface supports two data lanes and together with the clock signal, six pins as been used.

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	i.MX 7 Ball Name	I/O	Description	Remarks
J2, PIN21	COM specific	MIPI_DSI_CLK0M	O	Differential clock pair, negative signal	
J2, PIN19	COM specific	MIPI_DSI_CLK0P	O	Differential clock pair, positive signal	
J2, PIN 27	COM specific	MIPI_DSI_D0M	I/O	Differential data pair #0, negative signal	
J2, PIN 25	COM specific	MIPI_DSI_D0P	I/O	Differential data pair #0, positive signal	
J2, PIN 33	AIN1	MIPI_DSI_D1M	O	Differential data pair #1, negative signal	
J2, PIN 31	AIN0	MIPI_DSI_D1P	O	Differential data pair #1, positive signal	

5.3 Digital Audio Interfaces: Synchronous Audio Interfaces (SAI)

This section lists signals related to the Digital Audio Interfaces.

The i.MX 7 SoC contains an audio subsystem. It consists of three Synchronous Audio Interfaces (SAI1-SAI3) and a Medium Quality Speaker Interface (MQS). In addition, the IOMUX block allows the signals to get in and out of the SoC via configured pins.

Each SAI block is a full-duplex serial port with frame synchronization that allows communication with external devices using a variety of serial protocols (like I2S, AC-97, TDM and codec/DSP interfaces), up to 32-bits per word and different clock/frame options.

The three SAI interfaces and MQS block are directly connected to the IOMUX.

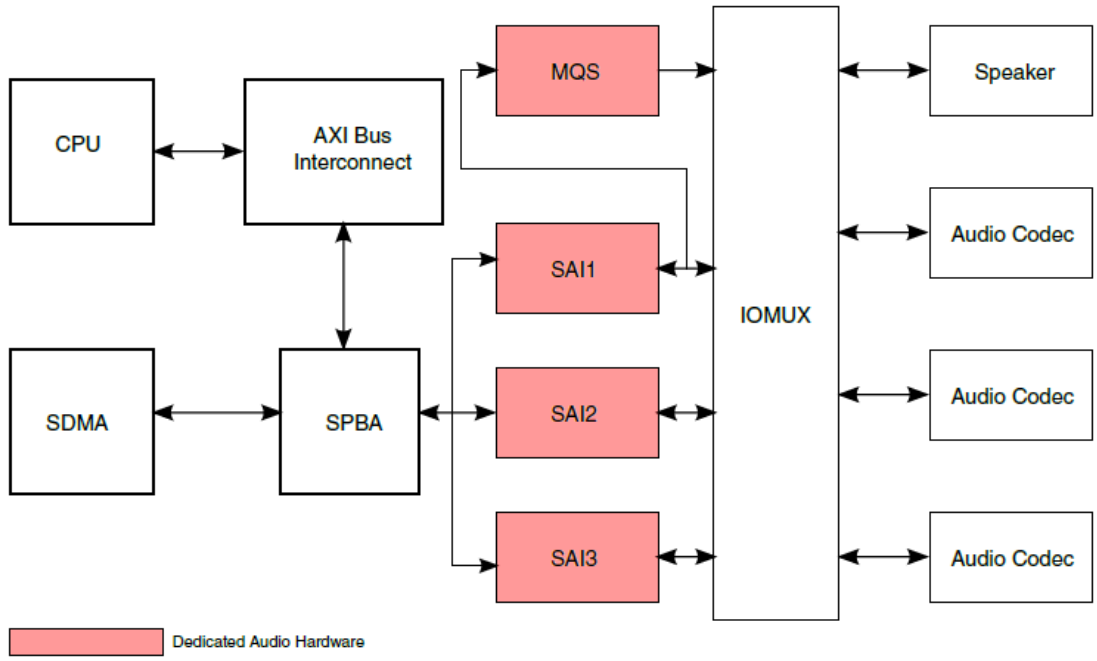


Figure 5 – Audio Subsystem Block Diagram

The table below lists pins that have been allocated according to the *EACOM Board specification*. The SAI1 port is used with **synchronous** transmit and receive sections (meaning that transmit and receive share the clock and frame synch signals).

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	i.MX 7 Ball Name	I/O	Description	Remarks
J1, PIN 50	AUDIO_RXD	SAI1_RXD	I	Data receive signal	Alternative function SAI1_RXD
J1, PIN 52	AUDIO_TXC	SAI1_TXC	O	Transmit clock signal. Also work as Receive clock signal	Alternative function SAI1_TXC
J1, PIN 56	AUDIO_TXD	SAI1_TXD	O	Data transmit signal	Alternative function SAI1_TXD
J1, PIN 54	AUDIO_TXFS	SAI1_TXFS	O	Transmit Frame sync signal. Also work as Receive Frame sync signal	Alternative function SAI1_TXFS
J1, PIN 67	AUDIO_MCLK	SAI1_MCLK	O	Clock output signal	Alternative function SAI1_MCLK

Besides the SAI port #1 signals allocated in the *EACOM Board specification* there are more (alternative) pins for the SAI1 interface. The table below lists these pins.

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	i.MX 7 Ball Name	I/O	Description	Remarks
J1, PIN 33	BL_PWM	GPIO1_IO01	I/O	Audio Master Clock	Alternative function SAI1_MCLK
J2, PIN 48	MQS_LEFT	SAI1_RXC	I/O	Receive Bit Clock	Alternative function SAI1_ RX_BCLK
J2, PIN 50	MQS_RIGHT	SAI1_RXFS	I/O	Receive Frame Sync	Alternative function SAI1_RX_SYNC

The table below lists pins available for the SAI2 interface.

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	i.MX 7 Ball Name	I/O	Description	Remarks
J1, PIN 37	GPIO9	GPIO1_IO02	I/O	Audio Master Clock	Alternative function SAI2_MCLK
J1, PIN 67	AUDIO_MCLK	SAI1_MCLK	I/O	Audio Master Clock	Alternative function SAI2_MCLK
J1, PIN 42	CSI_D4	SD2_RESET_B	I/O	Audio Master Clock	Alternative function SAI2_MCLK
J3, PIN 48	MQS_LEFT	SAI1_RXC	I/O	Receive Bit Clock	Alternative function SAI2_RX_BCLK
J1, PIN 62	MMC_CMD	SD2_CMD	I/O	Receive Bit Clock	Alternative function SAI2_RX_BCLK
J1, PIN 24	UART-B_CTS	SAI2_RXD	I	Receive Data	Alternative function SAI2_RX_DATA
J1, PIN 66	MMC_D0	SD2_DATA0	I	Receive Data	Alternative function SAI2_RX_DATA
J3, PIN 50	MQS_RIGHT	SAI1_RXFS	I/O	Receive Frame Sync	Alternative function SAI2_RX_SYNC
J1, PIN 58	MMC_CLK	SD2_CLK	I/O	Receive Frame Sync	Alternative function SAI2_RX_SYNC
J1, PIN 63	UART-A_RTS	SAI2_TXC	I/O	Transmit Bit Clock	Alternative function SAI2_TX_BCLK
J1, PIN 70	MMC_D1	SD2_DATA1	I/O	Transmit Bit Clock	Alternative function SAI2_TX_BCLK
J1, PIN 26	UART-B_RTS	SAI2_TXD	O	Transmit Data	Alternative function SAI2_TX_DATA
J1, PIN 68	MMC_D3	SD2_DATA3	O	Transmit Data	Alternative function SAI2_TX_DATA
J1, PIN 65	UART-A_CTS	SAI2_TXFS	I/O	Transmit Frame Sync	Alternative function SAI2_TX_SYNC
J1, PIN 64	MMC_D2	SD2_DATA2	I/O	Transmit Frame Sync	Alternative function SAI2_TX_SYNC

The table below lists pins available for the SAI3 interface.

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	i.MX 7 Ball Name	I/O	Description	Remarks
J1, PIN 39	PWM	GPIO1_IO03	I/O	Audio Master Clock	Alternative function SAI3_MCLK
J3, PIN 98	GPIO3	SD1_RESET_B	I/O	Audio Master Clock	Alternative function SAI3_MCLK
J1, PIN 46	UART-A_TXD	UART1_TXD	I/O	Audio Master Clock	Alternative function SAI3_MCLK
J3, PIN 80	SD_CMD	SD1_CMD	I/O	Receive Bit Clock	Alternative function SAI3_RX_BCLK
J1, PIN 22	UART-B_RXD	UART2_RXD	I/O	Receive Bit Clock	Alternative function SAI3_RX_BCLK
J3, PIN 84	SD_D0	SD1_DATA0	I	Receive Data	Alternative function SAI3_RX_DATA
J1, PIN 27	UART-B_TXD	UART2_TXD	I	Receive Data	Alternative function SAI3_RX_DATA
J3, PIN 78	SD_CLK	SD1_CLK	I/O	Receive Frame Sync	Alternative function SAI3_RX_SYNC
J3, PIN 40	UART-C_RXD	UART3_RXD	I/O	Receive Frame Sync	Alternative function SAI3_RX_SYNC
J3, PIN 86	SD_D1	SD1_DATA1	I/O	Transmit Bit Clock	Alternative function SAI3_TX_BCLK
J3, PIN 42	UART-C_TXD	UART3_TXD	I/O	Transmit Bit Clock	Alternative function SAI3_TX_BCLK
J3, PIN 90	SD_D3	SD1_DATA3	O	Transmit Data	Alternative function SAI3_TX_DATA
J3, PIN 44	COM specific	UART3_RTS	O	Transmit Data	Alternative function SAI3_TX_DATA
J3, PIN 88	SD_D2	SD1_DATA2	I/O	Transmit Frame Sync	Alternative function SAI3_TX_SYNC
J3, PIN 46	COM specific	UART3_CTS	I/O	Transmit Frame Sync	Alternative function SAI3_TX_SYNC

5.4 Digital Audio Interface: Medium Quality Speaker (MQS)

This section lists signals related to the Medium Quality Speaker (MQS) function.

The i.MX 7 SoC has one MQS block that can generate audio via PWM modulation on digital output pins. It convert the I2S audio data from SAI1 to PWM signals that can drive external speaker directly. MQS provides only simple audio reproduction. No internal pop, click or distortion artifact reduction methods are provided.

See *Figure 5* on page 29 for a block diagram how the MQS block is connected.

The EACOM Board specification defines a stereo output for MQS sound signals. The table below lists the pin assignment according to EACOM Board specification.

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	**i.MX 7 Ball Name**	**I/O**	**Description**	**Remarks**
J3, PIN 48	MQS_LEFT	SAI1_RXC	O	Left signal output	Alternative function MQS_LEFT
J3, PIN 50	MQS_RIGHT	SAI1_RXFS	O	Right signal output	Alternative function MQS_ RIGHT

The table below lists these the alternative pin locations are.

Exp. Conn. Pin	**EACOM Board Name (on uCOM Adap. Board)**	**i.MX 7 Ball Name**	**I/O**	**Description**	**Remarks**
J1, PIN 62	MMC_CMD	SD2_CMD	O	Left signal output	Alternative function MQS_LEFT
J1, PIN 58	MMC_CLK	SD2_CLK	O	Right signal output	Alternative function MQS_ RIGHT

5.5 Ethernet

This section lists signals related to the Ethernet interface.

The i.MX 7 has two Gigabit Ethernet controllers (10/100/1000Mbps) that are IEEE1588 compliant. There are no on-board Ethernet PHYs on the uCOM board. The Ethernet interfaces must be implemented with (external) Ethernet-PHY on the carrier board.

For implementation with external Ethernet-PHYs, see section 11.1 - Ethernet MAC (ENET) in the iMX7 Dual Reference Manual, document IMX7DRM. The i.MX 7 supports the MII, RMII and RGMII interfaces and can be connected to any industry standard Ethernet-PHY. The table below lists the signals used when connecting to Ethernet interface #1.

Exp. Conn. Pin	i.MX 7 Ball Name	I/O	Description	MII interface	RMII interface	RGMII interface
J2, PIN 92	ENET1_COL	I	Pin carry alternative signal ENET1_COL	MII_COL	-	-
J2, PIN 94	ENET1_CRS	I	Pin carry alternative signal ENET1_CRS	MII_CRS	-	-
J2, PIN 97	ENET1_RX_CLK	I	Pin carry alternative signal ENET1_RX_CLK	MII_RX_CLK	-	-
J2, PIN 83	ENET1_TX_CLK	O	Pin carry alternative signal ENET1_TX_CLK	MII_TX_CLK	50MHz ref clock	-
J2, PIN 79	ENET1_TXC	O	Pin carry alternative signal ENET1_TX_ER	MII_TX_ER	-	RGMII_TXC
J2, PIN 85	ENET1_RDATA0	I	Pin carry alternative signal RGMII1_RD0	MII_RD0	RMII_RXD0	RGMII_RXD0
J2, PIN 87	ENET1_RDATA1	I	Pin carry alternative signal RGMII1_RD1	MII_RD1	RMII_RXD1	RGMII_RXD1
J2, PIN 89	ENET1_RDATA2	I	Pin carry alternative signal RGMII1_RD2	MII_RD2	-	RGMII_RXD2
J2, PIN 91	ENET1_RDATA3	I	Pin carry alternative signal RGMII1_RD3	MII_RD3	-	RGMII_RXD3
J2, PIN 95	ENET1_RX_CTL	I	Pin carry alternative signal RGMII1_RX_CTL	MII_RX_DV	RMII_CRS_DV	RGMII_RX_CTL
J2, PIN 93	ENET1_RXC	I	Pin carry alternative signal RGMII1_RXC	MII_RX_ER	RMII_RXER	RGMII_RXC
J2, PIN 71	ENET1_TDATA0	O	Pin carry alternative signal RGMII1_TD0	MII_TD0	RMII_TXD0	RGMII_TXD0
J2, PIN 73	ENET1_TDATA1	O	Pin carry alternative signal RGMII1_TD1	MII_TD1	RMII_TXD1	RGMII_TXD1
J2, PIN 75	ENET1_TDATA2	O	Pin carry alternative signal RGMII1_TD2	MII_TD2	-	RGMII_TXD2
J2, PIN 77	ENET1_TDATA3	O	Pin carry alternative signal RGMII1_TD3	MII_TD3	-	RGMII_TXD3
J2, PIN 81	ENET1_TX_CTL	O	Pin carry alternative signal RGMII1_TX_CTL	MII_TX_EN	RMII_TXEN	RGMII_TX_CTL

The table below lists the signals used when connecting to Ethernet interface #2.

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	i.MX 7 Ball Name	I/O	Description	MII interface	RMII interface	RGMII interface
J2, PIN 86	COM specific	EPDC1_PWRSTAT	I	Pin carry alternative signal ENET2_COL	MII_COL	-	-

J2, PIN 84	COM specific	EPDC1_PWRCOM	I	Pin carry alternative signal ENET2_CRS	MII_CRS	-	-
J2, PIN 90	COM specific	EPDC1_BDR1	I	Pin carry alternative signal ENET2_RX_CLK	MII_RX_CLK	-	-
J2, PIN 88	COM specific	EPDC1_BDR0	O	Pin carry alternative signal ENET2_TX_CLK	MII_TX_CLK	50MHz ref clock	-
J2, PIN 82	TP_RST	EPDC1_GDSP	O	Pin carry alternative signal ENET2_TX_ER	MII_TX_ER	-	RGMII_TXC
J2, PIN 68	COM specific	EPDC1_SDCLK	I	Pin carry alternative signal RGMII2_RD0	MII_RD0	RMII_RXD0	RGMII_RXD0
J2, PIN 70	COM specific	EPDC1_SDLE	I	Pin carry alternative signal RGMII2_RD1	MII_RD1	RMII_RXD1	RGMII_RXD1
J2, PIN 72	COM specific	EPDC1_SDOE	I	Pin carry alternative signal RGMII2_RD2	MII_RD2	-	RGMII_RXD2
J2, PIN 74	CSI_D2	EPDC1_SDSHR	I	Pin carry alternative signal RGMII2_RD3	MII_RD3	-	RGMII_RXD3
J2, PIN 60	GPIO1	EPDC1_SDCE0	I	Pin carry alternative signal RGMII2_RX_CTL	MII_RX_DV	RMII_CRS_DV	RGMII_RX_CTL
J2, PIN 62	GPIO2	EPDC1_SDCE1	I	Pin carry alternative signal RGMII2_RXC	MII_RX_ER	RMII_RXER	RGMII_RXC
J2, PIN 64	GPIO5	EPDC1_SDCE2	O	Pin carry alternative signal RGMII2_TD0	MII_TD0	RMII_TXD0	RGMII_TXD0
J2, PIN 66	GPIO6	EPDC1_SDCE3	O	Pin carry alternative signal RGMII2_TD1	MII_TD1	RMII_TXD1	RGMII_TXD1
J2, PIN 76	BL_PWR_EN	EPDC1_GDCLK	O	Pin carry alternative signal RGMII2_TD2	MII_TD2	-	RGMII_TXD2
J2, PIN 78	DISP_PWR_EN	EPDC1_GDOE	O	Pin carry alternative signal RGMII2_TD3	MII_TD3	-	RGMII_TXD3
J2, PIN 80	TP_IRQ	EPDC1_GDRL	O	Pin carry alternative signal RGMII2_TX_CTL	MII_TX_EN	RMII_TXEN	RGMII_TX_CTL

The MDIO interface is a two-wire management interface. The MDIO management interface implements a standardized method to access the PHY device management registers.

The *uCOM Adapter Board* has one on-board 10/100/1000 Mbps Ethernet interface. Atheros AR8031 Integrated 10/100/1000 Mbps Ethernet Transceiver is used as PHY and is connected via the RGMII interface to the i.MX 7 SoC. The *EACOM Board Specification* defines two Ethernet interfaces. The Ethernet interface on the *uCOM Adapter Board* is assigned to ETH1. ETH2 is left unconnected.

On the *uCOM Adapter Board*, the MDIO interface is used for accessing the on-board Ethernet-PHY, see the first two rows in the table below. These can with advantage be used to control a second Ethernet-PHY. Alternatively, a second MDIO interface is also available, see row 3-8 in the table below.

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	**i.MX 7 Ball Name**	**I/O**	**Description**	**Remarks**
J1, PIN 28	CSI_MCLK	GPIO1_IO10-ETH_PHY_MDIO	I/O		Non-standard pin allocation. Signal allocated for ETH_PHY_MDIO and used by on-board Ethernet-PHY. Signal can be used for external Ethernet-PHY for second Ethernet interface.

J1, PIN 35	CSI_VSYNC	GPIO1_IO11/ ETH_PHY_MDC	O		Non-standard pin allocation. Signal allocated for ETH_PHY_MDC and used by on-board Ethernet-PHY. Signal can be used for external Ethernet-PHY for second Ethernet interface.
J1, PIN 25	CAN2_TX	GPIO1_IO15	O	Pin carry alternative signal ENET2_MDC	
J1, PIN 51	CSI_D5	SD2_WP	O	Pin carry alternative signal ENET2_MDC	
J1, PIN 27	UART-B_TXD	UART2_TXD	O	Pin carry alternative signal ENET2_MDC	
J1, PIN 34	CAN2_RX	GPIO1_IO14	I/O	Pin carry alternative signal ENET2_ MDIO	
J1, PIN 60	CSI_D3	SD2_CD_B	I/O	Pin carry alternative signal ENET2_ MDIO	
J1, PIN 22	UART-B_RXD	UART2_RXD	I/O	Pin carry alternative signal ENET2_ MDIO	

5.6 FlexCAN

This section lists signals related to the Controller Area Network (CAN) interface.

The i.MX 7 SoC has two Flexible Controller Area Network (FlexCAN) interfaces that supports bitrates of up to 1Mbps each. The FlexCAN module is a communication controller implementing the CAN protocol according to the CAN 2.0B protocol specification, which supports both standard and extended message frames.

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	i.MX 7 Ball Name	I/O	Description	Remarks
J1, PIN 30	CAN1_RX	GPIO1_IO12	I	CAN port 1 receive signal	Default location for EACOM Board spec.
J1, PIN 32	CAN1_TX	GPIO1_IO13	O	CAN port 1 transmit signal	Default location for EACOM Board spec.
J1, PIN 34	CAN2_RX	GPIO1_IO14	I	CAN port 2 receive signal	Default location for EACOM Board spec.
J1, PIN 25	CAN2_TX	GPIO1_IO14	O	CAN port 2 transmit signal	Default location for EACOM Board spec.
J1, PIN 50	AUDIO_RXD	SAI1_RXD	I	CAN port 1 receive signal	Alternative location for CAN1_RX signal
J1, PIN 52	AUDIO_TXC	SAI1_TXC	O	CAN port 1 transmit signal	Alternative location for CAN1_TX signal
J1, PIN 54	AUDIO_TXFS	SAI1_TXFS	I	CAN port 2 receive signal	Alternative location for CAN2_RX signal
J1, PIN 56	AUDIO_TXD	SAI1_TXD	O	CAN port 2 transmit signal	Alternative location for CAN2_TX signal

5.7 GPIOs

This section lists signals related to General Purpose Input/Output (GPIO) functionality.

Many pins have GPIO functionality that can be enabled (via pin multiplexing). All GPIO pins can be used to generate interrupts as well as be wakeup sources.

The *EACOM Board specification* defines only a few GPIOs and they are listed in the table below. The pins that cannot be configured as GPIOs are Ethernet, USB, PCIe, MIPI-CSI and MIPI-DSI. I2C pins can be GPIOs but are unsuitable since I2C-A is used on-board and I2C-B and I2C-C have 2.2Kohm on-board pull-up resistors.

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	i.MX 7 Ball Name	I/O	Description	Remarks
J2, PIN 60	GPIO1	EPDC_SDCE0	I/O	GPIO	GPIO1 controlled by alternative pin function GPIO2_IO20
J2, PIN 62	GPIO2	EPDC_SDCE1	I/O	GPIO	GPIO2 controlled by alternative pin function GPIO2_IO21
J3, PIN 98	GPIO3	SD1_RESET_B	I/O	GPIO	GPIO3 controlled by alternative pin function GPIO5_IO02
J3, PIN 94	GPIO4	SD1_CD_B	I/O	GPIO	GPIO4 controlled by alternative pin function GPIO5_IO00
J2, PIN 64	GPIO5	EPDC_SDCE2	I/O	GPIO	GPIO5 controlled by alternative pin function GPIO2_IO22
J2, PIN 66	GPIO6	EPDC_SDCE3	I/O	GPIO	GPIO6 controlled by alternative pin function GPIO2_IO23
J3, PIN 85	GPIO7	LCD_RESET	I/O	GPIO	GPIO7 controlled by alternative pin function GPIO3_IO04
J2, PIN 94	GPIO8	ENET1_CRS	I/O	GPIO	GPIO7 controlled by alternative pin function GPIO7_IO14
J1, PIN 37	GPIO9	GPIO1_IO02	I/O	GPIO	GPIO7 controlled by alternative pin function GPIO1_IO02

5.8 I2C

This section lists signals related to the Inter-Integrated Circuit (I2C) interface.

The i.MX 7 SoC has four I2C interfaces. Three of these are assigned in the *EACOM Board Specification*. i.MX 7 I2C channel #1 is assigned to EACOM I2C channel A. I2C channel #2 is assigned to EACOM I2C channel B. I2C channel #3 is assigned to EACOM I2C channel C.

Pin assignment for I2C channel A cannot be changed since this channel is used on the *iMX7 Dual uCOM board* (for PMIC and E2PROM communication). The *uCOM Adapter Board* has placed 2.2Kohm pull-up resistors on EACOM I2C channel B and C (I2C channel #2 and #3, respectively).

The table below lists the pin assignment as well as alternative pin locations.

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	i.MX 7 Ball Name	I/O	Description	Remarks
J1, PIN 41	I2C-A_SCL	I2C1_SCL	I/O	Clock signal of I2C channel #1	Signal has on-board 2.2Kohm pullup resistor. Signal is connected to on-board I2C channel to PMIC and E2PROM.
J1, PIN 43	I2C-A_SDA	I2C1_SDA	I/O	Data signal of I2C channel #1	Signal has on-board 2.2Kohm pullup resistor. Signal is connected to on-board I2C channel to PMIC and E2PROM.
J1, PIN 45	I2C-B_SCL	I2C2_SCL	I/O	Clock signal of I2C channel #2	Signal has on-board 2.2Kohm pullup resistor.
J1, PIN 47	I2C-B_SDA	I2C2_SDA	I/O	Data signal of I2C channel #2	Signal has on-board 2.2Kohm pullup resistor.
J3, PIN 24	I2C-C_SCL	I2C3_SCL	I/O	Clock signal of I2C channel #3	Signal has on-board 2.2Kohm pullup resistor.
J3, PIN 26	I2C-C_SDA	I2C3_SDA	I/O	Data signal of I2C channel #3	Signal has on-board 2.2Kohm pullup resistor.

Note that the following two positions for I2C interfaces are not allowed:

- I2C1_SCL on i.MX 7 pins GPIO1_IO04 and UART1_RXD should not be used. I2C channel #1 is allocated on another pin.
- I2C1_SDA on i.MX 7 pins GPIO1_IO05 and UART1_TXD should not be used. I2C channel #1 is allocated on another pin.

i.MX 7 I2C interface #2 can are located on the following pins (as alternative functions), but note that these locations are not recommended since the *EACOM Board specification* has allocated this function on another pin, see above.

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	i.MX 7 Ball Name	I/O	Description	Remarks
J1, PIN 44	USB_H1_OC	GPIO1_IO06	I/O	Clock signal of I2C channel #2	I2C2_SCL. Note that this location is not recommended since the EACOM Board specification has allocated this function on another pin, see above.
J1, PIN 22	UART-B_RXD	UART2_RXD	I/O	Clock signal of I2C channel #2	I2C2_SCL. Note that this location is not recommended since the EACOM Board specification has allocated this function on another pin, see above.
J1, PIN 48	USB_H1_PWR_EN	GPIO1_IO07	I/O	Data signal of I2C channel #2	I2C2_SDA. Note that this location is not recommended since the EACOM Board specification has allocated this function on another pin, see above.
J1, PIN 27	UART-B_TXD	UART2_TXD	I/O	Data signal of I2C channel #2	I2C2_SDA. Note that this location is not recommended since the EACOM Board specification has allocated this function on another pin, see above.

i.MX 7 I2C interface #3 can are located on the following pins (as alternative functions).

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	i.MX 7 Ball Name	I/O	Description	Remarks
J3, PIN 58	COM specific	GPIO1_IO08	I/O	Clock signal of I2C channel #3	I2C3_SCL. Note that this location is not recommended since the EACOM Board specification has allocated this function on another pin, see above.
J3, PIN 69	LCD_R4	LCD1_DATA20	I/O	Clock signal of I2C channel #3	I2C3_SCL. Note that this location is not recommended since the EACOM Board specification has allocated this function on another pin, see above.
J3, PIN 54	CSI_PCLK	GPIO1_IO09	I/O	Data signal of I2C channel #3	I2C3_SDA. Note that this location is not recommended since the EACOM Board specification has allocated this function on another pin, see above.
J3, PIN 71	LCD_R5	LCD1_DATA21	I/O	Data signal of I2C channel #3	I2C3_SDA. Note that this location is not recommended since the EACOM Board specification has allocated this function on another pin, see above.

i.MX 7 I2C interface #4 can are located on the following pins (as alternative functions).

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	i.MX 7 Ball Name	I/O	Description	Remarks
J3, PIN 28	COM specific	I2C4_SCL	I/O	Clock signal of I2C channel #4	Note that an external pull-up resistor is needed.
J1, PIN 28	CSI_MCLK	GPIO1_IO10	I/O	Clock signal of I2C channel #4	Note that an external pull-up resistor is needed.
J3, PIN 73	LCD_R6	LCD1_DATA22	I/O	Clock signal of I2C channel #4	Note that an external pull-up resistor is needed.
J3, PIN 50	MQS_RIGHT	SAI1_RXFS	I/O	Clock signal of I2C channel #4	Note that an external pull-up resistor is needed.
J3, PIN 30	COM specific	I2C4_SDA	I/O	Data signal of I2C channel #4	Note that an external pull-up resistor is needed.
J1, PIN 35	CSI_VSYNC	GPIO1_IO11	I/O	Data signal of I2C channel #4	Note that an external pull-up resistor is needed.
J3, PIN 75	LCD_R7	LCD1_DATA23	I/O	Data signal of I2C channel #4	Note that an external pull-up resistor is needed.
J3, PIN 48	MQS_LEFT	SAI1_RXC	I/O	Data signal of I2C channel #4	Note that an external pull-up resistor is needed.

5.9 JTAG

This section lists signals related to the JTAG debug interface.

The i.MX 7 SoC has a module called System JTAG Controller (SJC) that provides a JTAG interface to internal logic, including the two ARM Cortex-A9 cores and Cortex-M4 core. The SJC complies with JTAG TAP standards. The i.MX 7 SoC use the JTAG port for production, testing, and system debugging.

The JTAG signals are available as listed in the table below.

Exp. Conn. Pin	i.MX 7 Ball Name	I/O	Description	Remarks
J2, PIN 2	NVCC_JTAG	O	Logic level supply voltage	Used by external debugger to detect logic level to use for signaling. Typically 3.3V.
J2, PIN 4	JTAG_TMS	I	JTAG signal TMS	
J2, PIN 6	JTAG_TCK	I	JTAG signal TCK	
J2, PIN 8	JTAG_TDO	O	JTAG signal TDO	
J2, PIN 10	JTAG_TDI	I	JTAG signal TDI	
J2, PIN 12	JTAG_TRST	I	JTAG signal TRST	
J2, PIN 14	JTAG_MOD	I		Signal shall always be connected to ground. Signal has a 1Kohm pulldown resistor and can be left floating.
J1, PIN 36	EXT_RST_OUT	I	System reset	Signal is active low and controls internal system reset. Signal has a 10K ohm pullup resistor.

When using the the *uCOM Adapter Board*, there is a 10 pos FPC connector that is used on all EACOM boards for JTAG access, see picture below for location and orientation.

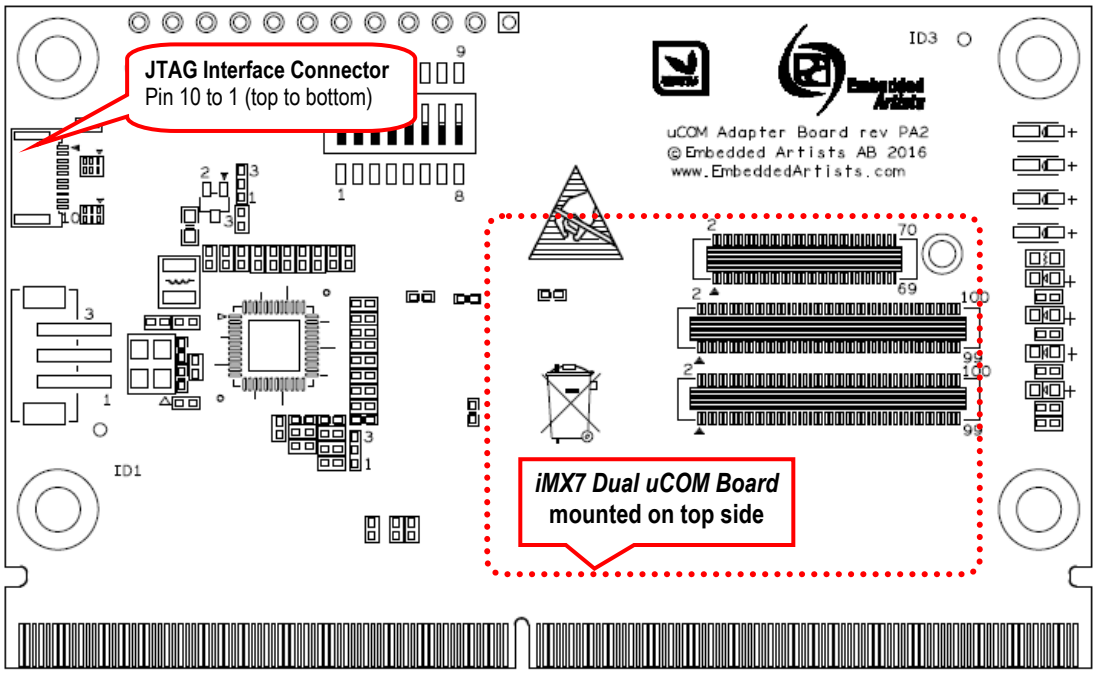


Figure 6 – uCOM Adapter Board, Location of JTAG Interface Connector

The table below lists the 10 signals on the JTAG connector.

FPC connector pin	Connected to i.MX 7 Ball Name	I/O	Description	Remarks
1	NVCC_JTAG	O	Logic level supply voltage	Used by external debugger to detect logic level to use for signaling. Typically 3.3V.
2	JTAG_TMS	I	JTAG signal TMS	
3			Ground	
4	JTAG_TCK	I	JTAG signal TCK	
5			Ground	
6	JTAG_TDO	O	JTAG signal TDO	
7	JTAG_MOD	I		Signal shall always be connected to ground. Signal has a 1Kohm pulldown resistor and can be left floating.
8	JTAG_TDI	I	JTAG signal TDI	
9	JTAG_TRST	I	JTAG signal TRST	
10	JTAG_SRST	I	System reset	Signal is active low and controls internal system reset. Signal has a 10K ohm pullup resistor.

The *iMX7 Dual uCOM Developer's Kit* contains an adapter board for connection to common debug connectors. The 10 pos connector is Molex 512811094 and has 0.5 mm (20 mil) pitch. FPC length should be kept less than 7 cm.

5.10 PCI Express

This section lists signals related to the PCI Express interface.

The i.MX 7Dual SoC has a single lane PCI Express (PCIe) interface. The interface is compliant with the PCIe 2.1 specification that supports up to 6Gbit/s data rate. PCIe 2.1/2.0 is backward compatible with the PCIe 1.1 standard that supports 2.5Gbit/s data rate.

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	i.MX 7 Ball Name	I/O	Description	Remarks
J2, PIN 43	PCIE_CLK_P	PCIE_REFCLKOUT_P	O	100 MHz reference clock, positive signal in differential pair	
J2, PIN 45	PCIE_CLK_N	PCIE_REFCLKOUT_N	O	100 MHz reference clock, negative signal in differential pair	
J2, PIN 55	PCIE_TX_P	PCIE_TX_P	O	Transmit data, positive signal in differential pair	
J2, PIN 57	PCIE_TX_N	PCIE_TX_N	O	Transmit data, negative signal in differential pair	
J2, PIN 49	PCIE_RX_P	PCIE_RX_P	I	Receive data, positive signal in differential pair	
J2, PIN 51	PCIE_RX_N	PCIE_RX_N	I	Receive data, negative signal in differential pair	
J2, PIN 37	SATA_RX_P	PCIE_REFCLKIN_P	I	If the i.MX 7Dual internally generated 100 MHz PCIe clock is not used, an external 100MHz PCIe reference clock shall be connected to this input (HCSL-signal, positive signal). If the internal clock is used, connect pin to ground.	Non-standard EACOM pin allocation.
J2, PIN 39	SATA_RX_N	PCIE_REFCLKIN_N	I	If the i.MX 7Dual internally generated 100 MHz PCIe clock is not used, an external 100MHz PCIe reference clock shall be connected to this input (HCSL-signal, negative signal). If the internal clock is used, connect pin to ground	Non-standard EACOM pin allocation.

A typical PCIe interface also has a USB Host, a I2C interface and (typically) three control signals; wakeup (input to iMX7), disable and reset (outputs from iMX7). These interfaces and control signals are not specifically defined in the *EACOM Board specification* and is up to each carrier board design to assign/allocate.

5.11 Power Management

This section lists signals related to power management, i.e., reset and external power supplies.

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	I/O	Description	Remarks
J1, PIN 36	RESET_OUT	O	Reset output, active low	Open drain output. Driven low during reset. 1.5K pull-up resistor to VIN.
J3, PIN 62	RESET_IN	I	Reset input, active low	Pull signal low to activate reset. No need to pull signal high externally. Connected to cathode of series diode, so logic level of driving signal can be anywhere between 1.5-5 V.
On EACOM board: **P141/290**	PERI_PWR_EN	O	Enable signal (active high) for carrier board peripheral power supplies.	Uses RESET signal from the i.MX 7. More information about carrier board design can be found in *EACOM Board specification*.

5.12 Power Supply Signals

This section lists signals related to power supply.

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	Description	Remarks
J1, PIN 2 J1, PIN 4 J1, PIN 6 J2, PIN 9 J2, PIN 11	VSYS	3.3 - 5.5V supply voltage	See technical specification for details about valid range.
J1, PIN 1 J1, PIN 5 J1, PIN 9 J1, PIN 11 J1, PIN 13 J1, PIN 15 J2, PIN 5 J2, PIN 11 J2, PIN 16 J2, PIN 17 J2, PIN 22 J2, PIN 23 J2, PIN 26 J2, PIN 29 J2, PIN 35 J2, PIN 41 J2, PIN 47 J2, PIN 53 J2, PIN 59 J2, PIN 65 J2, PIN 96 J2, PIN 99 J3, PIN 17 J3, PIN 22 J3, PIN 27 J3, PIN 37 J3, PIN 47 J3, PIN 52 J3, PIN 57	GND	Ground	

J3, PIN 67 J3, PIN 77 J3, PIN 82 J3, PIN 87 J3, PIN 91 J3, PIN 97 J3, PIN 100			
J1, PIN 23	VBAT	Power supply for PMIC on-chip RTC. Connect to external primary (= non rechargeable) or secondary (= rechargeable) coin cell battery.	Connected to BD71815AGW PMIC, pin J6, SNVSC.
J1, PIN 14 J3, PIN 1 J3, PIN 3 J3, PIN 5 J3, PIN 7	DCIN	See	
J3, PIN 13 J3, PIN 15	VDD_IO	Supply rail with the same voltage as the IO pins (3.3 or 1.8V) on the iMX7 Dual uCOM Board.	If 3.3V IO voltage: 600mA on VDD_3P3 and VDD_IO summed. If 1.8V IO voltage: 200mA on VDD_1P8 and VDD_IO summed.
J1, PIN 8 J1, PIN 10	VDD_3P3	3.3V generated by PMIC for external use.	600 mA max
J1, PIN 12	VDD_1P8	1.8V generated by PMIC for external use.	200 mA max
J2, PIN 18	VO1_3P3	Supply rail generated by PMIC for external use.	0.8-3.3V range, 100 mA max Startup at 3.3V but can change by SW.
J2, PIN 20	VO2_3P3	Supply rail generated by PMIC for external use.	0.8-3.3V range, 100 mA max Startup at 3.3V but can change by SW.
J2, PIN 24	VO4_3P3	Supply rail generated by PMIC for external use.	0.8-3.3V range, 400 mA max Startup at 3.3V but can change by SW.
J3, PIN 18	WLED_P	Programmable current source for white LEDs, typically used on display backlight. Positive terminal.	Up to 18V, 25mA max
J3, PIN 20	WLED_N	Programmable current source for white LEDs, typically used on display backlight. Negative terminal.	Up to 18V, 25mA max

For additional information about powering, see chapter 6 .

5.13 PWM

This section lists signals related to Pulse Wide Modulators (PWM).

The i.MX 7 SoC has four PWM channels that are available via pin multiplexing. The generated signals has 16-bit resolution. PWM signals can be used to generate analogue signals (emulate a DAC) and also control intensity / brightness in display applications.

There are two PWM signals defined in the *EACOM Board specification*. One general PWM signal and one that is intended for backlight intensity control for displays. The latter can however be used as a general PWM signals also if backlight intensity control is not needed or control is arranged differently. The remaining PWM signals are available as alternative functions on certain pins.

The table below lists the pin assignment as well as alternative pin locations.

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	i.MX 7 Ball Name	I/O	Description	Remarks
J1, PIN 39	PWM	GPIO1_IO03	O	PWM3_OUT signal	
J1, PIN 33	BL_PWM	GPIO1_IO01	O	PWM1_OUT signal	

The table below lists the pin assignment for the alternative pin locations.

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	i.MX 7 Ball Name	I/O	Description	Remarks
J3, PIN 58	COM specific	GPIO1_IO08	O	PWM1_OUT signal	
J1, PIN 37	GPIO9	GPIO1_IO02	O	PWM2_OUT signal	
J3, PIN 54	CSI_PCLK	GPIO1_IO09	O	PWM2_OUT signal	
J1, PIN 28	CSI_MCLK	GPIO1_IO10	O	PWM3_OUT signal	
J1, PIN 35	CSI_VSYNC	GPIO1_IO11	O	PWM4_OUT signal	

5.14 SD/MMC

This section lists signals related to Ultra Secured Digital Host Controller (uSDHC) functions.

The i.MX 7 SoC has 3 uSDHC interfaces. One, uSDHC3, is allocated (on-board) for interface to eMMC Flash. The interfaces are capable of interfacing with SD Memory Cards, SDIO, MMC, CE-ATA cards and eMMC devices. The features of the uSDHC module include the following:

- Conforms to the SD Host Controller Standard Specification version 3.0
- Compatible with the MMC System Specification version 4.2/4.3/4.4/4.41/4.5/5.0
- Compatible with the SD Memory Card Specification version 3.0 and supports the Extended Capacity SD Memory Card
- Compatible with the SDIO Card Specification version 3.0
- Designed to work with SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC, MMC plus, and MMC RS cards
- Supports 1-bit / 4-bit SD and SDIO modes, 1-bit / 4-bit / 8-bit MMC modes

The *EACOM Board specification* defines one 4-databit SD interface (uSDHC1) and one 8-databit MMC interface (uSDHC2). The 8-bit MMC interface pin allocation is however only 4-bit.

The table below lists the pin assignment according to *EACOM Board specification*.

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	i.MX 7 Ball Name	I/O	Description	Remarks
J3, PIN 78	SD_CLK	SD1_CLK	O	Clock for MMC/SD/SDIO card	
J3, PIN 80	SD_CMD	SD1_CMD	I/O	CMD line connect to card	
J3, PIN 84	SD_D0	SD1_DATA0	I/O	DATA0 line in all modes. Also used to detect busy status	
J3, PIN 86	SD_D1	SD1_DATA1	I/O	DATA1 line in 4/8-bit mode. Also used to detect interrupt in 1/4-bit mode	
J3, PIN 88	SD_D2	SD1_DATA2	I/O	DATA2 line or Read Wait in 4-bit mode, Read Wait in 1-bit mode	
J3, PIN 90	SD_D3	SD1_DATA3	I/O	DATA3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode	
J1, PIN 58	MMC_CLK	SD2_CLK	O	Clock for MMC/SD/SDIO card	
J1, PIN 62	MMC_CMD	SD2_CMD	I/O	CMD line connect to card	
J1, PIN 66	MMC_D0	SD2_DATA0	I/O	DATA0 line in all modes. Also used to detect busy status	
J1, PIN 70	MMC_D1	SD2_DATA1	I/O	DATA1 line in 4/8-bit mode Also used to detect interrupt in 1/4-bit mode	
J1, PIN 64	MMC_D2	SD2_DATA2	I/O	DATA2 line or Read Wait in 4-bit mode, Read Wait in 1-bit mode	
J1, PIN 68	MMC_D3	SD2_DATA3	I/O	DATA3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode	

The table below lists of alternative pin locations for uSDHC1 signals.

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	i.MX 7 Ball Name	I/O	Description	Remarks
J3, PIN 32	SPI-B_CLK	ECSPI2_SCLK	I/O	DATA4 line in 8-bit mode, not used in other modes	Alternative function SD2_DATA4
J3, PIN 36	SPI-B_MOSI	ECSPI2_MOSI	I/O	DATA5 line in 8-bit mode, not used in other modes	Alternative function SD2_DATA5
J3, PIN 34	SPI-B_MISO	ECSPI2_MISO	I/O	DATA6 line in 8-bit mode, not used in other modes	Alternative function SD2_DATA6
J3, PIN 38	SPI-B_SSEL	ECSPI2_SS0	I/O	DATA7 line in 8-bit mode, not used in other modes	Alternative function SD2_DATA7
J3, PIN 94	GPIO4	SD1_CD_B	I	Card detection pin	Alternative function SD1_CD_B.
J3, PIN 58	COM specific	GPIO1_IO08	O	IO power voltage selection signal	Alternative function SD1_VSELECT
J3, PIN 46	COM specific	UART3_CTS	O	IO power voltage selection signal	Alternative function SD1_VSELECT
J3, PIN 54	CSI_PCLK	GPIO1_IO09	O	LED control used to drive an external LED Active high	Alternative function SD1_LCTL
J3, PIN 40	UART-C_RXD	UART3_RXD	O	LED control used to drive an external LED Active high	Alternative function SD1_LCTL
J3, PIN 96	COM specific	SD1_WP	I	Card write protect detect	Alternative function SD1_WP

The table below lists of alternative pin locations for uSDHC2 signals as well as data signals 4-7 (for full 8-bit MMC interface).

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	i.MX 7 Ball Name	I/O	Description	Remarks
J1, PIN 60	CSI_D3	SD2_CD_B	I	Card detection pin	Alternative function SD2_CD_B
J1, PIN 55	SPI-A_CLK	ECSPI1_SCLK	I/O	DATA4 line in 8-bit mode, not used in other modes	Alternative function SD2_DATA4
J1, PIN 57	SPI-A_MOSI	ECSPI1_MOSI	I/O	DATA5 line in 8-bit mode, not used in other modes	Alternative function SD2_DATA5
J1, PIN 59	SPI-A_MISO	ECSPI1_MISO	I/O	DATA6 line in 8-bit mode, not used in other modes	Alternative function SD2_DATA6
J1, PIN 53	SPI-A_SSEL	ECSPI1_SS0	I/O	DATA7 line in 8-bit mode, not used in other modes	Alternative function SD2_DATA7
J1, PIN 28	CSI_MCLK	GPIO1_IO10	O	LED control used to drive an external LED Active high	Alternative function SD2_LCTL
J3, PIN 42	UART-C_TXD	UART3_TXD	O	LED control used to drive an external LED Active high	Alternative function SD2_LCTL
J1, PIN 42	CSI_D4	SD2_RESET_B	O		Alternative function SD2_RESET_B
J1, PIN 30	CAN1_RX	GPIO1_IO12	O	IO power voltage selection signal	Alternative function SD2_VSELECT
J1, PIN 51	CSI_D5	SD2_WP	I	Card write protect detect	Alternative function SD2_WP

There are no accessible pins for uSDHC3 signals since these are connected to the on-board eMMC Flash.

5.15 ECSPI / SPI

This section lists signals related to Enhanced Configurable Serial Peripheral Interface (ECSPI) functions.

The i.MX 7 SoC has 4 ECSPI block that are capable of full-duplex, synchronous, four-wire serial communication. The *EACOM Board specification* defines two 4-signal ECSPI interfaces. ECSPI1 and ECSPI2 have been allocated for these. The remaining ECSPI signals are available as alternative functions on certain pins.

The table below lists the pin assignment according to *EACOM Board specification*.

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	i.MX 7 Ball Name	I/O	Description	Remarks
J1, PIN 59	SPI-A_MISO	ECSPI1_MISO	I/O	Master data in, slave data out	ECSPI1_MISO
J1, PIN 57	SPI-A_MOSI	ECSPI1_MOSI	I/O	Master data out, slave data in	ECSPI1_MOSI
J1, PIN 55	SPI-A_SCLK	ECSPI1_SCLK	I/O	SPI clock signal	ECSPI1_SCLK
J1, PIN 53	SPI-A_SS0	ECSPI1_SS0	I/O	Chip select signal	ECSPI1_SS0
J3, PIN 34	SPI-B_MISO	ECSPI2_MISO	I/O	Master data in, slave data out	ECSPI2_MISO
J3, PIN 36	SPI-B_MOSI	ECSPI2_MOSI	I/O	Master data out, slave data in	ECSPI2_MOSI
J3, PIN 32	SPI-B_SCLK	ECSPI2_SCLK	I/O	SPI clock signal	ECSPI2_SCLK
J3, PIN 38	SPI-B_SS0	ECSPI2_SS0	I/O	Chip select signal	ECSPI2_SS0

The table below lists of alternative pin locations for ECSPI1 signals.

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	i.MX 7 Ball Name	I/O	Description	Remarks
J3, PIN 40	UART-C_RXD	UART3_RXD	I/O	Master data in, slave data out	ECSPI1_MISO
J3, PIN 42	UART-C_TXD	UART3_TXD	I/O	Master data out, slave data in	ECSPI1_MOSI
J1, PIN 27	UART-B_TXD	UART2_TXD	I/O	SPI data ready signal	ECSPI1_RDY
J3, PIN 44	COM specific	UART3_RTS	I/O	SPI clock signal	ECSPI1_SCLK
J3, PIN 46	COM specific	UART3_CTS	I/O	Chip select signal	ECSPI1_SS0
J1, PIN 61	UART-A_RXD	UART1_RXD	I/O	Chip select signal	ECSPI1_SS1
J1, PIN 46	UART-A_TXD	UART1_TXD	I/O	Chip select signal	ECSPI1_SS2
J1, PIN 22	UART-B_RXD	UART2_RXD	I/O	Chip select signal	ECSPI1_SS3

There are no alternative pin locations for the ECSPI2 signals.

The table below lists of alternative pin locations for ECSPI3 signals.

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	i.MX 7 Ball Name	I/O	Description	Remarks
J1, PIN 65	UART-A_CTS	SAI2_TXFS	I/O	Master data in, slave data out	ECSPI3_MISO
J1, PIN 63	UART-A_RTS	SAI2_TXC	I/O	Master data out, slave data in	ECSPI3_MOSI
J1, PIN 42	CSI_D4	SD2_RESET_B	I/O	SPI data ready signal	ECSPI3_RDY
J1, PIN 45	I2C-B_SCL	I2C2_SCL	I/O	SPI clock signal	ECSPI3_SCLK **Note** that there is a 2.2Kohm pull-up resistor on this signal.
J1, PIN 24	UART-B_CTS	SAI2_RXD	I/O	SPI clock signal	ECSPI3_SCLK
J1, PIN 47	I2C-B_SDA	I2C2_SDA	I/O	Chip select signal	ECSPI3_SS0 **Note** that there is a 2.2Kohm pull-up resistor on this signal.
J1, PIN 26	UART-B_RTS	SAI2_TXD	I/O	Chip select signal	ECSPI3_SS0
J3, PIN 90	SD_D3	SD1_DATA3	I/O	Chip select signal	ECSPI3_SS1
J1, PIN 60	CSI_D3	SD2_CD_B	I/O	Chip select signal	ECSPI3_SS2
J1, PIN 51	CSI_D5	SD2_WP	I/O	Chip select signal	ECSPI3_SS3

The table below lists of alternative pin locations for ECSPI4 signals.

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	i.MX 7 Ball Name	I/O	Description	Remarks
J3, PIN 89	LCD_CLK	LCD1_CLK	I/O	Master data in, slave data out	ECSPI4_MISO
J3, PIN 94	GPIO4	SD1_CD_B	I/O	Master data in, slave data out	ECSPI4_MISO
J3, PIN 79	LCD_ENABLE	LCD1_ENABLE	I/O	Master data out, slave data in	ECSPI4_MOSI
J3, PIN 96	COM specific	SD1_WP	I/O	Master data out, slave data in	ECSPI4_MOSI
J3, PIN 88	SD_D2	SD1_DATA2	I/O	SPI data ready signal	ECSPI4_RDY
J3, PIN 81	LCD_HSYNC	LCD1_HSYNC	I/O	SPI clock signal	ECSPI4_SCLK
J3, PIN 98	GPIO3	SD1_RESET_B	I/O	SPI clock signal	ECSPI4_SCLK
J3, PIN 83	LCD_VSYNC	LCD1_VSYNC	I/O	Chip select signal	ECSPI4_SS0

J3, PIN 78	SD_CLK	SD1_CLK	I/O	Chip select signal	ECSPI4_SS0
J3, PIN 80	SD_CMD	SD1_CMD	I/O	Chip select signal	ECSPI4_SS1
J3, PIN 84	SD_D0	SD1_DATA0	I/O	Chip select signal	ECSPI4_SS2
J3, PIN 86	SD_D1	SD1_DATA1	I/O	Chip select signal	ECSPI4_SS3

5.16 UART

This section lists signals related to Universal Asynchronous Receiver/Transmitter (UART) functions.

The i.MX 7 SoC has 7 UARTs, supporting bitrates up to 4Mbps each. The *EACOM Board specification* defines two 4-signal UARTs and one 2-signal UART. The remaining UART signals are available as alternative functions on certain pins.

Note that the chip-level IOMUX modifies the direction and routing of the UART signals based on whether the UART is operating in DCE mode or DTE mode. See section 15.3.2 in IMX7DRM for details.

The table below lists the pin assignment according to *EACOM Board specification*.

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	i.MX 7 Ball Name	I/O	Description	Remarks
J1, PIN 46	UART-A_TXD	UART1_TXD	I/O	UART1 Transmit Data	Alternative function is UART1_TXD.
J1, PIN 61	UART-A_RXD	UART1_RXD	I/O	UART1 Receive Data	Alternative function is UART1_RXD.
J1, PIN 63	UART-A_RTS	SAI2_TXC	I/O	UART1 Request to Send	Alternative function is UART1_RTS_B.
J1, PIN 65	UART-A_CTS	SAI2_TXFS	I/O	UART1 Clear to Send	Alternative function is UART1_CTS_B.
J1, PIN 27	UART-B_TXD	UART2_TXD	I/O	UART2 Transmit Data	Alternative function is UART2_TXD.
J1, PIN 22	UART-B_RXD	UART2_RXD	I/O	UART2 Receive Data	Alternative function is UART2_RXD.
J1, PIN 26	UART-B_RTS	SAI2_TXD	I/O	UART2 Request to Send	Alternative function is UART2_RTS_B.
J1, PIN 24	UART-B_CTS	SAI2_RXD	I/O	UART2 Clear to Send	Alternative function is UART2_CTS_B.
J3, PIN 42	UART-C_TXD	UART3_TXD	I/O	UART3 Transmit Data	Alternative function is UART3_TXD.
J3, PIN 40	UART-C_RXD	UART3_RXD	I/O	UART3 Receive Data	Alternative function is UART3_RXD.

There are no alternative pin locations for UART1 signals.

The table below lists of alternative pin locations for UART2 signals.

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	i.MX 7 Ball Name	I/O	Description	Remarks
J3, PIN 79	LCD_ENABLE	LCD1_ENABLE	I/O	UART2 Transmit Data	Alternative function is UART2_TXD.
J3, PIN 89	LCD_CLK	LCD1_CLK	I/O	UART2 Receive Data	Alternative function is UART2_RXD.
J3, PIN 81	LCD_HSYNC	LCD1_HSYNC	I/O	UART2 Request to Send	Alternative function is UART2_RTS_B.
J3, PIN 83	LCD_VSYNC	LCD1_VSYNC	I/O	UART2 Clear to Send	Alternative function is UART2_CTS_B.

The table below lists of alternative pin locations for UART3 signals.

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	i.MX 7 Ball Name	I/O	Description	Remarks
J3, PIN 54	CSI_PCLK	GPIO1_IO09	I/O	UART3 Transmit Data	Alternative function is UART3_TXD.
J3, PIN 58	COM specific	GPIO1_IO08	I/O	UART3 Receive Data	Alternative function is UART3_RXD.
J1, PIN 28	CSI_MCLK	GPIO1_IO10	I/O	UART3 Request to Send	Alternative function is UART3_RTS_B.
J3, PIN 44	COM specific	UART3_RTS	I/O	UART3 Request to Send	Alternative function is UART3_RTS_B.
J1, PIN 35	CSI_VSYNC	GPIO1_IO11	I/O	UART3 Clear to Send	Alternative function is UART3_CTS_B.
J3, PIN 46	COM specific	UART3_CTS	I/O	UART3 Clear to Send	Alternative function is UART3_CTS_B.

The table below lists of alternative pin locations for UART4 signals.

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	i.MX 7 Ball Name	I/O	Description	Remarks
J1, PIN 47	I2C-B_SDA	I2C2_SDA	I/O	UART4 Transmit Data	Alternative function is UART4_TXD. **Note** that there is a 2.2Kohm pull-up resistor on this signal.
J1, PIN 63	UART-A_RTS	SAI2_TXC	I/O	UART4 Transmit Data	Alternative function is UART4_TXD.
J1, PIN 70	MMC_D1	SD2_DATA1	I/O	UART4 Transmit Data	Alternative function is UART4_TXD.
J1, PIN 45	I2C-B_SCL	I2C2_SCL	I/O	UART4 Receive Data	Alternative function is UART4_RXD. **Note** that there is a 2.2Kohm pull-up resistor on this signal.
J1, PIN 65	UART-A_CTS	SAI2_TXFS	I/O	UART4 Receive Data	Alternative function is UART4_RXD.
J1, PIN 66	MMC_D0	SD2_DATA0	I/O	UART4 Receive Data	Alternative function is UART4_RXD.
J1, PIN 26	UART-B_RTS	SAI2_TXD	I/O	UART4 Request to Send	Alternative function is UART4_RTS_B.
J1, PIN 68	MMC_D3	SD2_DATA3	I/O	UART4 Request to Send	Alternative function is UART4_RTS_B.
J1, PIN 24	UART-B_CTS	SAI2_RXD	I/O	UART4 Clear to Send	Alternative function is UART4_CTS_B.
J1, PIN 64	MMC_D2	SD2_DATA2	I/O	UART4 Clear to Send	Alternative function is UART4_CTS_B.

The table below lists of alternative pin locations for UART5 signals.

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	i.MX 7 Ball Name	I/O	Description	Remarks
J1, PIN 48	USB_H1_PWR_EN	GPIO1_IO07	I/O	UART5 Transmit Data	Alternative function is UART5_TXD.
J3, PIN 30	COM specific	I2C4_SDA	I/O	UART5 Transmit Data	Alternative function is UART5_TXD.
J1, PIN 52	AUDIO_TXC	SAI1_TXC	I/O	UART5 Transmit Data	Alternative function is UART5_TXD.
J1, PIN 44	USB_H1_OC	GPIO1_IO06	I/O	UART5 Receive Data	Alternative function is UART5_RXD.
J3, PIN 28	COM specific	I2C4_SCL	I/O	UART5 Receive Data	Alternative function is UART5_RXD.
J1, PIN 50	AUDIO_RXD	SAI1_RXD	I/O	UART5 Receive Data	Alternative function is UART5_RXD.
J1, PIN 56	AUDIO_TXD	SAI1_TXD	I/O	UART5 Request to Send	Alternative function is UART5_RTS_B.
J3, PIN 26	HDMI/I2C-C_SDA	I2C3_SDA	I/O	UART5 Request to Send	Alternative function is UART5_RTS_B. **Note** that there is a 2.2Kohm pull-up resistor on this signal.
J1, PIN 21	USB_O1_PWR_EN	GPIO1_IO05	I/O	UART5 Request to Send	Alternative function is UART5_RTS_B.

J1, PIN 54	AUDIO_TXFS	SAI1_TXFS	I/O	UART5 Clear to Send	Alternative function is UART5_CTS_B.
J3, PIN 24	HDMI/I2C-C_SCL	I2C3_SCL	I/O	UART5 Clear to Send	Alternative function is UART5_CTS_B. **Note** that there is a 2.2Kohm pull-up resistor on this signal.
J1, PIN 19	USB_O1_OC	GPIO1_IO04	I/O	UART5 Clear to Send	Alternative function is UART5_CTS_B.

The table below lists of alternative pin locations for UART6 signals.

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	i.MX 7 Ball Name	I/O	Description	Remarks
J1, PIN 57	SPI-A_MOSI	ECSPI1_MOSI	I/O	UART6 Transmit Data	Alternative function is UART6_TXD.
J2, PIN 46	COM specific	EPDC1_DATA09	I/O	UART6 Transmit Data	Alternative function is UART6_TXD.
J3, PIN 96	COM specific	SD1_WP	I/O	UART6 Transmit Data	Alternative function is UART6_TXD.
J1, PIN 55	SPI-A_CLK	ECSPI1_SCLK	I/O	UART6 Receive Data	Alternative function is UART6_RXD.
J2, PIN 44	COM specific	EPDC1_DATA08	I/O	UART6 Receive Data	Alternative function is UART6_RXD.
J3, PIN 94	GPIO4	SD1_CD_B	I/O	UART6 Receive Data	Alternative function is UART6_RXD.
J1, PIN 59	SPI-A_MISO	ECSPI1_MISO	I/O	UART6 Request to Send	Alternative function is UART6_RTS_B.
J2, PIN 48	COM specific	EPDC1_DATA10	I/O	UART6 Request to Send	Alternative function is UART6_RTS_B.
J3, PIN 98	GPIO3	SD1_RESET_B	I/O	UART6 Request to Send	Alternative function is UART6_RTS_B.
J1, PIN 53	SPI-A_SSEL	ECSPI1_SS0	I/O	UART6 Clear to Send	Alternative function is UART6_CTS_B.
J2, PIN 50	COM specific	EPDC1_DATA11	I/O	UART6 Clear to Send	Alternative function is UART6_CTS_B.
J3, PIN 78	SD_CLK	SD1_CLK	I/O	UART6 Clear to Send	Alternative function is UART6_CTS_B.

The table below lists of alternative pin locations for UART7 signals.

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	i.MX 7 Ball Name	I/O	Description	Remarks
J3, PIN 36	SPI-B_MOSI	ECSPI2_MOSI	I/O	UART7 Transmit Data	Alternative function is UART7_TXD.
J2, PIN 54	COM specific	EPDC1_DATA13	I/O	UART7 Transmit Data	Alternative function is UART7_TXD.
J3, PIN 86	SD_D1	SD1_DATA1	I/O	UART7 Transmit Data	Alternative function is UART7_TXD.
J3, PIN 32	SPI-B_CLK	ECSPI2_SCLK	I/O	UART7 Receive Data	Alternative function is UART7_RXD.
J2, PIN 52	COM specific	EPDC1_DATA12	I/O	UART7 Receive Data	Alternative function is UART7_RXD.
J3, PIN 84	SD_D0	SD1_DATA0	I/O	UART7 Receive Data	Alternative function is UART7_RXD.
J3, PIN 34	SPI-B_MISO	ECSPI2_MISO	I/O	UART7 Request to Send	Alternative function is UART7_RTS_B.
J2, PIN 56	COM specific	EPDC1_DATA14	I/O	UART7 Request to Send	Alternative function is UART7_RTS_B.
J3, PIN 90	SD_D3	SD1_DATA3	I/O	UART7 Request to Send	Alternative function is UART7_RTS_B.
J3, PIN 38	SPI-B_SSEL	ECSPI2_SS0	I/O	UART7 Clear to Send	Alternative function is UART7_CTS_B.
J2, PIN 58	COM specific	EPDC1_DATA15	I/O	UART7 Clear to Send	Alternative function is UART7_CTS_B.
J3, PIN 88	SD_D2	SD1_DATA2	I/O	UART7 Clear to Send	Alternative function is UART7_CTS_B.

5.17 USB

This section lists signals related to the USB interfaces.

The *EACOM Board Specification* has one USB 3.0 OTG port, one USB 3.0 Host port and one USB 2.0 Host port. The i.MX 7 has two USB 2.0 OTG ports and one HSIC port. Further, USB 3.0 is backward compatible with USB 2.0. The pins that are specific for USB 3.0 are just left unconnected and are for future upgrade.

The carrier board must provide a +5V supply (with enable and over-current functionality) for USB Host interfaces.

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	i.MX 7 Ball Name	I/O	Description	Remarks
J1, PIN 18	USB_O1_DN	USB_OTG1_DN	I/O	Negative Differential USB Signal, OTG compatible	
J1, PIN 16	USB_O1_DP	USB_OTG1_DP	I/O	Positive Differential USB Signal, OTG compatible	
J1, PIN 3	USB_O1_ID	USB_OTG1_ID	I	USB OTG ID pin	
J1, PIN 20	USB_O1_VBUS	USB_OTG1_VBUS	I	+5V USB VBUS detect input	This pin is +5V tolerant.
J1, PIN 21	USB_O1_PWR_EN	GPIO1_IO05	O	Enable external USB voltage supply. Active high output.	Alternative function is USB_OTG1_PWR
J1, PIN 19	USB_O1_OC	GPIO1_IO04	I	Signals an over-current condition on the USB voltage supply. Active low input.	Alternative function is USB_OTG1_OC
J1, PIN 48	USB_H1_PWR_EN	GPIO1_IO07	O	Enable external USB voltage supply. Active high output.	Alternative function is USB_OTG2_PWR
J1, PIN 44	USB_H1_OC	GPIO1_IO06	I	Signals an over-current condition on the USB voltage supply. Active low input.	Alternative function is USB_OTG2_OC
J2, PIN 63	USB_H1_DN	USB_OTG2_DN	I/O	Negative Differential USB Signal	
J2, PIN 61	USB_H1_DP	USB_OTG2_DP	I/O	Positive Differential USB Signal	
J2, PIN 69	USB_H1_SSTXP	USB_OTG2_ID	I/O	Not standard pin allocation.	Signal can optionally be used to create a OTG port of the *EACOM* USB Host post.
J2, PIN 67	USB_H1_VBUS	USB_OTG2_VBUS	I	+5V USB VBUS detect input	This pin is +5V tolerant.

The table below lists of alternative pin locations for USB signals.

Exp. Conn. Pin	EACOM Board Name (on uCOM Adap. Board)	i.MX 7 Ball Name	I/O	Description	Remarks
J1, PIN 37	GPIO9	GPIO1_IO02	I	USB OTG1 ID	Alternative function is USB OTG1 ID
J1, PIN 30	CAN1_RX	GPIO1_IO12	I	USB OTG1 ID	Alternative function is USB OTG1 ID
J3, PIN 28	COM specific	I2C4_SCL	I	USB OTG1 ID	Alternative function is USB OTG1 ID
J1, PIN 51	CSI_D5	SD2_WP	I	USB OTG1 ID	Alternative function is USB OTG1 ID
J3, PIN 40	UART-C_RXD	UART3_RXD	I	USB OTG1 OC	Signals an over-current condition on the USB voltage supply. Active low input.
J3, PIN 42	UART-C_TXD	UART3_TXD	O	USB OTG1 PWR EN	Enable external USB voltage supply. Active high output.
J1, PIN 39	PWM	GPIO1_IO03	I	USB OTG2 ID	Alternative function is USB OTG2 ID
J1, PIN 32	CAN1_TX	GPIO1_IO13	I	USB OTG2 ID	Alternative function is USB OTG2 ID
J3, PIN 30	COM specific	I2C4_SDA	I	USB OTG2 ID	Alternative function is USB OTG2 ID
J1, PIN 42	CSI_D4	SD2_RESET_B	I	USB OTG2 ID	Alternative function is USB OTG2 ID

J3, PIN 44	COM specific	UART3_RTS	I	USB OTG2 OC	Signals an over-current condition on the USB voltage supply. Active low input.
J3, PIN 46	COM specific	UART3_CTS	O	USB OTG2 PWR EN	Enable external USB voltage supply. Active high output.

6 Powering and PMIC Integration

The i.MX 7Dual SoC is tightly integrated with the PMIC (BD71815GW) in order to achieve high-performance and low-power operation of the *iMX7 Dual uCOM Board*. The BD71815GW PMIC contains an on-chip Li-ion battery charger with embedded Coulomb counter for battery fuel gauging. There are other functions as well that are not directly used on the *iMX7 Dual uCOM Board*, but rather left as an option for the board integration to utilize. The optional function of the PMIC are:

- Li-ion battery charger with programmable charge voltage and current
- White LED programmable current source
- Voltage Measurement for Thermistor
- Embedded Coulomb Counter for Battery Fuel Gauging
- Battery Monitoring and Alarm Output
- One general purpose output
- Voltage regulators that can be used to power the carrier board electronics

See the BD71815GW datasheet for details about each function.

The PMIC has multiple linear and DC/DC voltage regulators. Some are available for the carrier board design, reducing integration cost. Designs with moderate power consumptions may not need any external power supply at all. Everything can be handled by the on-board PMIC. Section 6.1 presents the available power rails.

There are two ways to power the *iMX7 Dual uCOM Board* - with, or without, using a rechargeable Li-ion battery:

- See section 6.2 for a description how to power the *iMX7 Dual uCOM Board* without adding a rechargeable Li-ion battery to the design.
- For battery powered applications, see section 6.3 for a description how to make the integration.

6.1 Available Power Rails

The table below presents the available power rails that can be used on the carrier board that the *iMX7 Dual uCOM Board* is integrated on.

Power Rail Output	Description	Voltage Range	Max Current
VDD_3P3	3.3V for external use.	3.3V	600mA
VDD_1P8	1.8V for external use.	1.8V	200mA
VDD_IO	Supply rail with the same voltage as the IO pins on the *iMX7 Dual uCOM Board*.	3.3V or 1.8V depending on IO voltage version of board	If 3.3V: 600mA on VDD_3P3 and VDD_IO summed. If 1.8V: 200mA on VDD_1P8 and VDD_IO summed.
VO1_3P3	Supply rail for external use.	0.8-3.3V Startup at 3.3V but can change by SW	100mA
VO2_3P3	Supply rail for external use.	0.8-3.3V Startup at 3.3V but can change by SW	100mA
VO4_3P3	Supply rail for external use. Controlled by signal: VO4_PWR_EN	0.8-3.3V Startup at 3.3V but can change by SW	300mA

	(active high, has internal pull-down)		
WLED **(WLED_P / WLED_N)**	Programmable current source for white LEDs, typically used on display backlight.	Up to 18V	25mA

Note that each pin on the Hirose DF40C expansion connectors can carry 300mA maximum. Connect to all pins on the expansion connectors that carry a specific power rail. High current power rails have more than one pin. VDD_3P3 and VDD_IO has each two pins on the expansion connectors.

Note that external load variations can affect the PMIC operation and potentially disturb the i.MX 7Dual SoC operation. Make sure that the carrier board electronics does not have abrupt consumption variations and does not generate noise on the power rails.

6.2 Integration Without Battery

This setup is very simple. An external 3.3-5.5V supply is basically all that is needed.

- Supply the 3.3-5.5V input voltage to **VSYS** (connect to all five pins on the expansion connectors)
    - Note that if the supply is in the range of 3.3-3.5V the LDOs on the PMIC operate in a bypass mode without optimal regulation. The operating point for the LDOs can be decreased for better regulation to, for example 3.1V, as a first thing the bootloader does.
- Note that for rev A boards a special procedure is needed to make it possible to use the *manufacturing tool* in this setup. The *manufacturing tool* is used to update bootloader and Linux images and might be needed during initial program development.
    - Add an option on the carrier board that allows a voltage between 3.5-28V (5V typical) to be supplied to **DCIN**. That will allow the board to startup in USB OTG bootloader mode.
    - This issue will be corrected on rev B boards.
- Supply a 3.3V input voltage to **EXT_RTC_VBAT** (one pin on the expansion connectors) to keep the real-time clock running. This voltage level can vary over a wide range, see section 10.2 for details. If the on-board *iMX7 Dual uCOM Board* real-time clock is not used or is not needed to be active when there is no external VSYS-connected supply, leave EXT_RTC_VBAT unconnected.
- Leave signals DCIN, VBAT_EXTand LED_EXT_CHG unconnected. **Connect EXT_BATTM and EXT_BATTP to ground. Connect VBAT_EXT_TS to ground via a 10K resistor (1%).**

6.3 Integration With Li-ion Rechargeable Battery

This setup is also simple and straight forward.

- Connect the positive terminal of the Li-ion battery to VBAT_EXT (connect to all five pins on the expansion connectors).
- Connect the negative terminal of the Li-ion battery to ground via a 10 milliohm resistor.

- Connect each side of the 10 milliohm resistor to EXT_BATTP/EXT_BATTM. Also connect an NTC termistor between EXT_BATTP and VBAT_EXT_TS. See Figure 7 for details.
- Optionally connect a LED with series with a 10K resistor between VSYS and LED_EXT_CHG. See Figure 7 for details.
- Connect DCIN to the power rail that will charge the battery, for example to VBUS of an USB port or an external supply input (typically a 5V or 12V input). See section 10.2 for details about DCIN voltage range. Connect to all five DCIN pins on the expansion connectors.
- Supply a 3.3V input voltage to **EXT_RTC_VBAT** (one pin on the expansion connectors) to keep the real-time clock running. This voltage level can vary over a wide range, see section 10.2 for details. If the on-board *iMX7 Dual uCOM Board* real-time clock is not used or is not needed to be active when there is no external VSYS-connected supply, leave EXT_RTC_VBAT unconnected.

See the BD71815GW datasheet for details about the battery charger functionality and programmable options.

Note that five pins has been allocated on the expansion connectors for VBAT_EXT. This limits maximum charge current to 1.5A (while the PMIC itself is capable of up to 2A charge current).

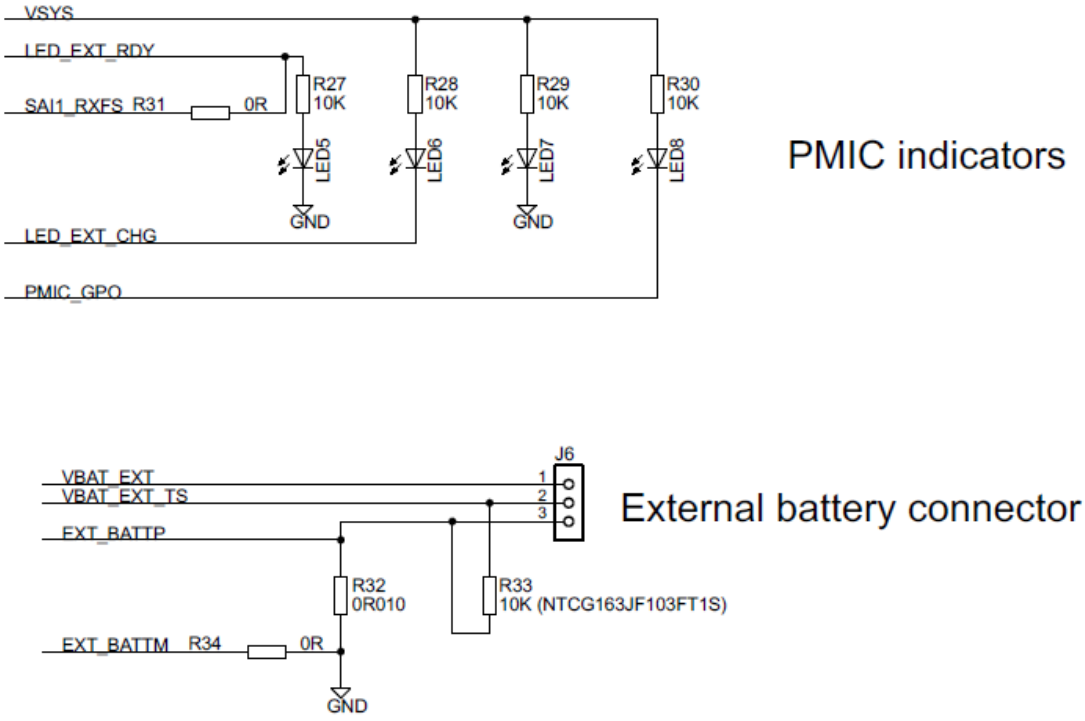


Figure 7 – Battery Integration to iMX7 Dual uCOM Board

7 uCOM Adapter Board

Embedded Artists has defined the EACOM board standard that is based on the SMARC form factor; module size 82 x 50 mm. Note that pinning is different from the SMARC standard. See the *EACOM Board specification* document for details and background information. Hereafter this standard will be referred to as **EACOM**.

Because of the ultra-compact form factor, the *iMX7 Dual uCOM Board* is **not** an EACOM board. There is no standard pinning across different ultra-compact boards like this. In order to utilize the *COM Carrier Board* during initial development, the *uCOM Adapter Board* has been created. It creates an EACOM board out of the *iMX7 Dual uCOM Board*.

The *iMX7 Dual uCOM Developers Kit* consists of:

- One *iMX7 Dual uCOM Board* with 3.3V I/O voltage
- One *uCOM Adapter Board*
- One *COM Carrier Board*

The *uCOM Adapter Board* contains the following functions (see schematic for details):

- Gigabit Ethernet interface
- Optional QSPI flash
- LVDS transmitter (transmitting the contents on the parallel RGB bus)
- Boot control
- Battery connector
- JTAG connector
- USB OTG interface electronics
- PMIC LEDs related to battery charging
- White LEDs for PMIC white LED driver

Note that the *iMX7 Dual uCOM Board* MUST be set for 3.3V I/O operation when mounted on the *uCOM Adapter Board*. See section 7.4 for details how to verify and change I/O voltage.

The carrier board connector has 314 pins with 0.5 mm pitch and the *uCOM Adapter Board* is inserted in a right angle (R/A) style. The connector is originally defined for use with MXM3 graphics cards. There are multiple sources for carrier board (MXM3) connectors due to the popular standard. The signal integrity is excellent and suitable for data rates up to 5 GHz.

7.1 Pin Numbering

The figures below show the pin numbering for *uCOM Adapter Board*, which is compatible with EACOM boards. Top side edge fingers are numbered P1-P156. Bottom side edge fingers are numbered S1-S158. There is an alternative pin numbering that follows the MXM3 standard with even numbers on the bottom and odd numbers on the top. This numbering is from 1-321, with 7 numbers/pins (150-156) removed due to the keying.

The picture below also illustrates where the *iMX7 Dual uCOM board* is mounted on the *uCOM Adapter Board*.

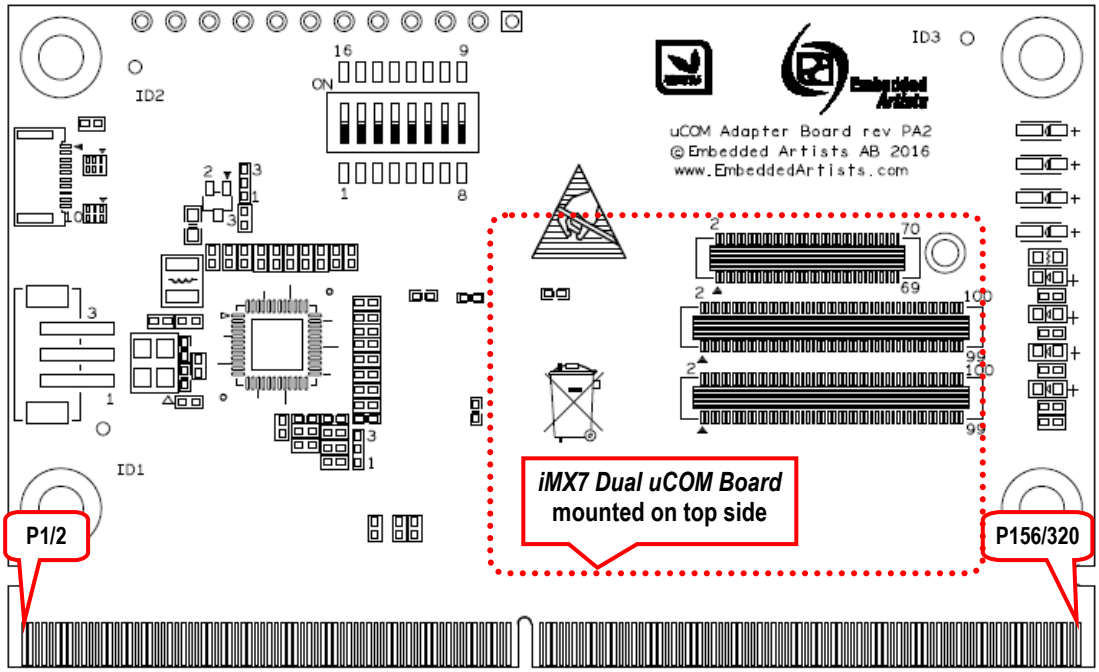


Figure 8 – uCOM Adapter Board Pin Numbering, Top Side

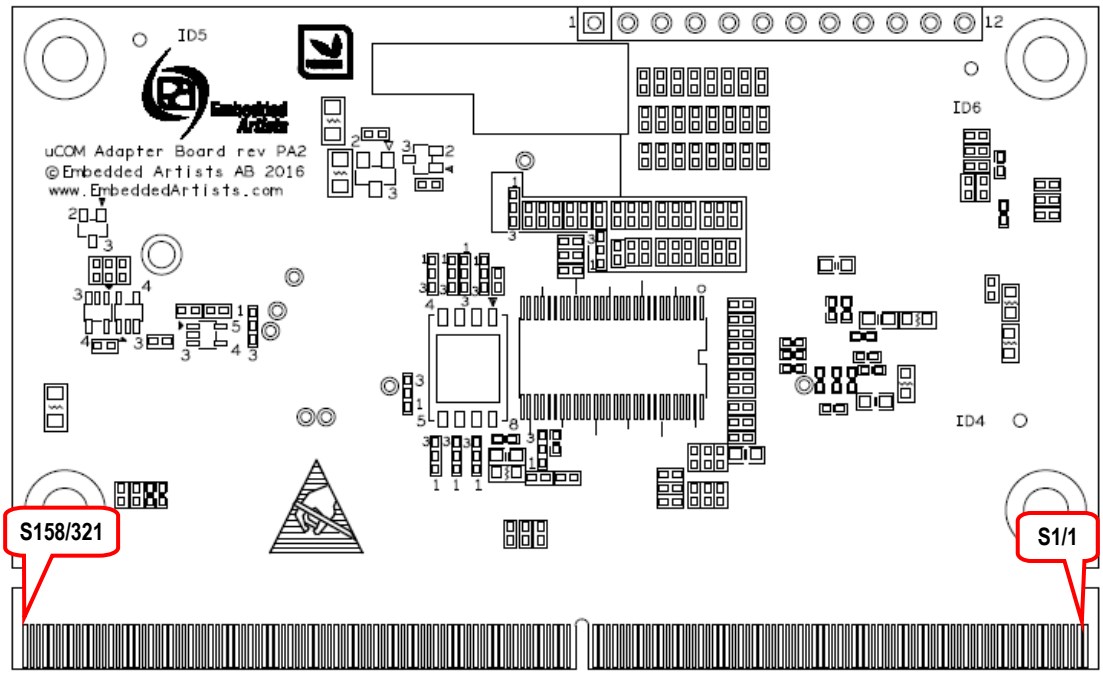


Figure 9 – uCOM Adapter Board Pin Numbering, Bottom Side

7.2 Pin Assignment

This section describes the pin assignment of the board, with the following columns:

Pin number	**Px** are top side edge fingers. **Sx** are bottom side edge fingers. An alternative, consecutive, numbering is also shown with odd numbers on the top and even numbers on the bottom side.
EACOM Board	Describe the typical usage of the pin according to EACOM. This pin usage should be followed to get compatibility between different COM

boards. If this is not needed, then any of the alternative functions on the pin can also be used.

i.MX 7Dual Ball Name — The name of the ball of the i.MX 7Dual SoC (or other component on the uCOM board) that is connected to this pin.

Notes — When relevant, the preferred pin function is listed.

There are 47 ground pins, which equal to about 15%, and 10 input voltage supply pins.

Note that not all EACOM-defined pins are connected on anything, typically because an interface is not supported or there are not enough free pins in the i.MX 7Dual SoC.

Further, some pins are *COM board type specific*, meaning that these pins might not be compatible with other EACOM boards. Using *type specific* pins may result in lost compatibility between EACOM boards, but not always. Check details between EACOM boards of interest.

The table below lists the top side pins, P1-P156, odd numbers.

Top Side Pin Num.	EACOM Board	uCOM Exp. Connector pin	i.MX 7Dual Ball Name	Alternative pin functions?	Notes
P1/2	GPIO6	J2, PIN 66	EPDC_SDCE3	Yes	GPIO6 controlled by alternative pin function GPIO2_IO23
P2/4	GPIO5	J2, PIN 64	EPDC_SDCE2	Yes	GPIO5 controlled by alternative pin function GPIO2_IO22
P3/6	GPIO4	J3, PIN 94	SD1_CD	Yes	GPIO4 controlled by alternative pin function GPIO5_IO01
P4/8	GPIO3	J3, PIN 98	SD1_RESET	Yes	GPIO3 controlled by alternative pin function GPIO5_IO02
P5/10	SD_D1	J3, PIN 86	SD1_DATA1	Yes	
P6/12	SD_D0	J3, PIN 84	SD1_DATA0	Yes	
P7/14	SD_CLK	J3, PIN 78	SD1_CLK	Yes	
P8/16	SD_CMD	J3, PIN 80	SD1_CMD	Yes	
P9/18	SD_D3	J3, PIN 90	SD1_DATA3	Yes	
P10/20	SD_D2	J3, PIN 88	SD1_DATA2	Yes	
P11/22	SD_VCC	J3, PIN 92			Supply voltage for SD interface (1.85V or 3.2V). Should only supply the SD interface.
P12/24	MMC_D1	J1, PIN 70	SD2_DATA1	Yes	
P13/26	MMC_D0	J1, PIN 66	SD2_DATA0	Yes	
P14/28	MMC_D7				Only 4-bit interface is supported.
P15/30	MMC_D6				Only 4-bit interface is supported.
P16/32	MMC_CLK	J1, PIN 58	SD2_CLK	Yes	
P17/34	MMC_D5				Only 4-bit interface is supported.
P18/36	MMC_CMD	J1, PIN 62	SD2_CMD	Yes	
P19/38	MMC_D4				Only 4-bit interface is supported.
P20/40	MMC_D3	J1, PIN 68	SD2_DATA3	Yes	
P21/42	MMC_D2	J1, PIN 64	SD2_DATA2	Yes	
P22/44	GND	GND			
P23/46	HDMI_TXC_N				HDMI interface not assigned on this COM board.
P24/48	HDMI_TXC_P				HDMI interface not assigned on this COM board.
P25/50	GND	GND			
P26/52	HDMI_TXD0_N				HDMI interface not assigned on this COM board.
P27/54	HDMI_TXD0_P				HDMI interface not assigned on this COM board.

P28/56	HDMI_HPD		HDMI interface not assigned on this COM board.
P29/58	HDMI_TXD1_N		HDMI interface not assigned on this COM board.
P30/60	HDMI_TXD1_P		HDMI interface not assigned on this COM board.
P31/62	GND	GND	
P32/64	HDMI_TXD2_N		HDMI interface not assigned on this COM board.
P33/66	HDMI_TXD2_P		HDMI interface not assigned on this COM board.
P34/68	HDMI_CEC		HDMI interface not assigned on this COM board.
P35/70	GND	GND	
P36/72	ETH1_MD1_P	ETH1 interface via external PHY	Connects to uCOM adapter board Ethernet-PHY AR8031, pin 14
P37/74	ETH1_MD1_N	ETH1 interface via external PHY	Connects to uCOM adapter board Ethernet-PHY AR8031, pin 15
P38/76	GND	GND	
P39/78	ETH1_MD0_P	ETH1 interface via external PHY	Connects to uCOM adapter board Ethernet-PHY AR8031, pin 11
P40/80	ETH1_MD0_N	ETH1 interface via external PHY	Connects to uCOM adapter board Ethernet-PHY AR8031, pin 12
P41/82	ETH1_LINK1000	ETH1 interface via external PHY	Connects to uCOM adapter board Ethernet-PHY AR8031, pin 24
P42/84	ETH1_ACT	ETH1 interface via external PHY	Connects to uCOM adapter board Ethernet-PHY AR8031, pin 23
P43/86	ETH1_LINK	ETH1 interface via external PHY	Connects to uCOM adapter board Ethernet-PHY AR8031, pin 26
P44/88	ETH1_MD3_N	ETH1 interface via external PHY	Connects to uCOM adapter board Ethernet-PHY AR8031, pin 21
P45/90	ETH1_MD3_P	ETH1 interface via external PHY	Connects to uCOM adapter board Ethernet-PHY AR8031, pin 20
P46/92	GND	GND	
P47/94	ETH1_MD2_N	ETH1 interface via external PHY	Connects to uCOM adapter board Ethernet-PHY AR8031, pin 18
P48/96	ETH1_MD2_P	ETH1 interface via external PHY	Connects to uCOM adapter board Ethernet-PHY AR8031, pin 17
P49/98	GND	GND	
P50/100	ETH2_MD1_P		
P51/102	ETH2_MD1_N		
P52/104	GND	GND	
P53/106	ETH2_MD0_P		
P54/108	ETH2_MD0_N		
P55/110	ETH2_LINK1000		
P56/112	ETH2_ACT		
P57/114	ETH2_LINK		
P58/116	ETH2_MD3_N		
P59/118	ETH2_MD3_P		
P60/120	GND	GND	
P61/122	ETH2_MD2_N		
P62/124	ETH2_MD2_P		
P63/126	GND	GND	

P64/128	USB_O1_DN	J1, PIN 18	USB_OTG1_DN	No	
P65/130	USB_O1_DP	J1, PIN 16	USB_OTG1_DP	No	
P66/132	USB_O1_OTG_ID	J1, PIN 3	USB_OTG1_ID	No	
P67/134	USB_O1_SSTXN				USB OTG port #1 on i.MX 7Dual does not support USB 3.0 so this pin is unconnected.
P68/136	USB_O1_SSTXP				USB OTG port #1 on i.MX 7Dual does not support USB 3.0 so this pin is unconnected.
P69/138	GND	GND			
P70/140	USB_O1_SSRXN				USB OTG port #1 on i.MX 7Dual does not support USB 3.0 so this pin is unconnected.
P71/142	USB_O1_SSRXP				USB OTG port #1 on i.MX 7Dual does not support USB 3.0 so this pin is unconnected.
P72/144	USB_O1_VBUS	J1, PIN 20	USB_OTG1_VBUS	No	
P73/146	USB_O1_PWR_EN	J1, PIN 21	GPIO1_IO05	Yes	Controlled by alternative pin function USB_OTG1_PWR
P74/148	USB_O1_OC	J1, PIN 19	GPIO1_IO04	Yes	Controlled by alternative pin function USB_OTG1_OC
150	Non existing pin				
152	Non existing pin				
154	Non existing pin				
156	Non existing pin				
P75/158	USB_H1_PWR_EN	J1, PIN 48	GPIO1_IO07	Yes	Controlled by alternative pin function USB_OTG2_OC
P76/160	USB_H1_OC	J1, PIN 44	GPIO1_IO06	Yes	Controlled by alternative pin function USB_OTG2_PWR
P77/162	GND	GND			
P78/164	USB_H1_DN	J2, PIN 63	USB_OTG2_DN	No	
P79/166	USB_H1_DP	J2, PIN 61	USB_OTG2_DP	No	
P80/168	USB_H1_SSTXN				USB OTG port #2 on i.MX 7Dual does not support USB 3.0 so this pin is unconnected.
P81/170	USB_H1_SSTXP	J2, PIN 69	USB_OTG2_ID	No	USB OTG port #2 on i.MX 7Dual does not support USB 3.0. Non-standard pin allocation. Pin carry signal USB_OTG2_ID, i.MX 7Dual ball B10.
P82/172	GND	GND			
P83/174	USB_H1_SSRXN	J3, PIN 76	SNVS_TAMPER2	No	USB OTG port #2 on i.MX 7Dual does not support USB 3.0. Non-standard pin allocation. Pin carry signal SNVS_TAMPER2, i.MX 7Dual ball AC9.
P84/176	USB_H1_SSRXP	J3, PIN 74	SNVS_TAMPER1	No	USB OTG port #2 on i.MX 7Dual does not support USB 3.0. Non-standard pin allocation. Pin carry signal SNVS_TAMPER1, i.MX 7Dual ball AC11.
P85/178	USB_H1_VBUS	J2, PIN 67	USB_OTG2_VBUS	No	
P86/180	USB_H2_PWR_EN	J3, PIN 72	SNVS_TAMPER0	No	USB Host port #2 on i.MX 7Dual does not exist. Non-standard pin allocation. Pin carry signal SNVS_TAMPER0, i.MX 7Dual ball AW11.
P87/182	USB_H2_OC	J1, PIN 17	ONOFF	No	USB Host port #2 on i.MX 7Dual does not exist. Non-standard pin allocation. Pin carry signal ONOFF, i.MX 7Dual ball AD13.
P88/184	GND	GND			
P89/186	USB_H2_DN	J3, PIN 95	HSIC_STROBE	No	USB Host port #2 on i.MX 7Dual does not exist.

					Non-standard pin allocation.
P90/188	USB_H2_DP	J3, PIN 93	HSIC_DATA	No	USB Host port #2 on i.MX 7Dual does not exist. Non-standard pin allocation.
P91/190	GND	GND			
P92/192	COM board specific	J2, PIN 86	EPDC_PWRSTAT	Yes	
P93/194	COM board specific	J2, PIN 84	EPDC_PWRCOM	Yes	
P94/196	COM board specific	J2, PIN 72	EPDC_SDOE	Yes	
P95/198	COM board specific	J2, PIN 70	EPDC_SDLE	Yes	
P96/200	COM board specific	J2, PIN 68	EPDC_SDCLK	Yes	
P97/202	COM board specific	J2, PIN 58	EPDC_D15	Yes	
P98/204	COM board specific	J2, PIN 56	EPDC_D14	Yes	
P99/206	COM board specific	J2, PIN 54	EPDC_D13	Yes	
P100/208	COM board specific	J2, PIN 52	EPDC_D12	Yes	
P101/210	COM board specific	J2, PIN 50	EPDC_D11	Yes	
P102/212	COM board specific	J2, PIN 48	EPDC_D10	Yes	
P103/214	COM board specific	J2, PIN 46	EPDC_D9	Yes	
P104/216	COM board specific	J2, PIN 44	EPDC_D8	Yes	
P105/218	COM board specific	J2, PIN 42	EPDC_D7	Yes	
P106/220	COM board specific	J2, PIN 40	EPDC_D6	Yes	
P107/222	COM board specific	J2, PIN 38	EPDC_D5	Yes	
P108/224	COM board specific	J2, PIN 36	EPDC_D4	Yes	
P109/226	COM board specific	J2, PIN 34	EPDC_D3	Yes	
P110/228	COM board specific	J2, PIN 32	EPDC_D2	Yes	
P111/230	COM board specific	J2, PIN 30	EPDC_D1	Yes	
P112/232	COM board specific	J2, PIN 28	EPDC_D0	Yes	
P113/234	COM board specific	J3, PIN 46	UART3_CTS	Yes	
P114/236	COM board specific	J2, PIN 90	EPDC_BDR1	Yes	
P115/238	COM board specific	J2, PIN 88	EPDC_BDR0	Yes	
P116/240	COM board specific	J3, PIN 44	UART3_RTS	Yes	
P117/242	COM board specific	J3, PIN 58	GPIO1_IO08	Yes	Signal is used on the uCOM Adapter Board to control SD1_VSELECT.
P118/244	GND	GND			
P119/246	SPI-B_SSEL	J3, PIN 38	ECSPI2_SS0	Yes	Controlled by alternative pin function ECSPI2_SS0
P120/248	SPI-B_MOSI	J3, PIN 36	ECSPI2_MOSI	Yes	Controlled by alternative pin function ECSPI2_MOSI
P121/250	SPI-B_MISO	J3, PIN 34	ECSPI2_MISO	Yes	Controlled by alternative pin function ECSPI2_MISO
P122/252	SPI-B_CLK	J3, PIN 32	ECSPI2_SCLK	Yes	Controlled by alternative pin function ECSPI2_SCLK
P123/254	SPI-A_SSEL	J1, PIN 53	ECSPI1_SS0	Yes	Controlled by alternative pin function ECSPI1_SS0
P124/256	SPI-A_MOSI	J1, PIN 57	ECSPI1_MOSI	Yes	Controlled by alternative pin function ECSPI1_MOSI
P125/258	SPI-A_MISO	J1, PIN 59	ECSPI1_MISO	Yes	Controlled by alternative pin function ECSPI1_MISO
P126/260	SPI-A_CLK	J1, PIN 55	ECSPI1_SCLK	Yes	Controlled by alternative pin function ECSPI1_SCLK
P127/262	GND	GND			
P128/264	UART-C_RXD	J3, PIN 40	UART3_RXD	Yes	Controlled by alternative pin function UART3_RXD
P129/266	UART-C_TXD	J3, PIN 42	UART3_TXD	Yes	Controlled by alternative pin function UART3_TXD

P130/268	UART-B_RXD	J1, PIN 22	UART2_RXD	Yes	Controlled by alternative pin function UART2_RXD
P131/270	UART-B_CTS	J1, PIN 24	SAI2_RXD	Yes	Controlled by alternative pin function UART2_CTS_B
P132/272	UART-B_RTS	J1, PIN 26	SAI2_TXD	Yes	Controlled by alternative pin function UART2_RTS_B
P133/274	UART-B_TXD	J1, PIN 27	UART2_TXD	Yes	Controlled by alternative pin function UART2_TXD
P134/276	UART-A_RXD	J1, PIN 61	UART1_TXD	Yes	Controlled by alternative pin function UART1_RXD
P135/278	UART-A_CTS	J1, PIN 65	SAI2_TXFS	Yes	Controlled by alternative pin function UART1_CTS_B
P136/280	UART-A_RTS	J1, PIN 63	SAI2_TXC	Yes	Controlled by alternative pin function UART1_RTS_B
P137/282	UART.A_TXD	J1, PIN 46	UART1_TXD	Yes	Controlled by alternative pin function UART1_TXD
P138/284	PWM	J1, PIN 39	GPIO1_IO03	Yes	Controlled by alternative pin function PWM3_OUT. Pin can only be an output since signal pass through a voltage level translator.
P139/286	GPIO2	J2, PIN 62	EPDC_SDCE1	Yes	GPIO2 controlled by alternative pin function GPIO2_IO21
P140/288	GPIO1	J2, PIN 60	EPDC_SDCE0	Yes	GPIO1 controlled by alternative pin function GPIO2_IO20
P141/290	PERI_PWR_EN		RESET_OUT	Yes	Enable signal (active high) for carrier board peripheral power supplies. More information about carrier board design can be found in *EACOM Board specification*. This signal is a copy of the RESET_OUT signal.
P142/292	RESET_IN	J3, PIN 62			Reset input, active low. Pull signal low to activate reset. No need to pull signal high externally.
P143/294	RESET_OUT	J1, PIN 36			Reset (open drain) output, active low. Driven low during reset. 1.5K pull-up resistor to VIN.
P144/296	GND	GND			
P145/298	VBAT	J1, PIN 23			Supply voltage from coin cell battery for keeping PMIC and RTC functioning during standby.
P146/300	E2PROM_WP	J1, PIN 31			Should be left open (will write protect the on-board parameter storage E2PROM), or connected to GND (will enable writes to the on-board parameter storage E2PROM AND place the i.MX 7Dual SoC in USB OTG boot mode after a power cycle).
P147/302	VIN	VSYS pins on J1 & J3			Main input voltage supply (3.3V)
P148/304	VIN	VSYS pins on J1 & J3			Main input voltage supply (3.3V)
P149/306	VIN	VSYS pins on J1 & J3			Main input voltage supply (3.3V)
P150/308	VIN	VSYS pins on J1 & J3			Main input voltage supply (3.3V)
P151/310	VIN	VSYS pins on J1 & J3			Main input voltage supply (3.3V)
P152/312	VIN	VSYS pins on J1 & J3			Main input voltage supply (3.3V)
P153/314	VIN	VSYS pins on J1 & J3			Main input voltage supply (3.3V)
P154/316	VIN	VSYS pins on J1 & J3			Main input voltage supply (3.3V)
P155/318	VIN	VSYS pins on J1 & J3			Main input voltage supply (3.3V)
P156/320	VIN	VSYS pins on J1 & J3			Main input voltage supply (3.3V)

The table below lists the bottom side pins, S1-S158, even numbers.

Bottom Side Pin Number	EACOM Board	uCOM Exp. Connector pin	i.MX 7Dual Ball Name	Alternative pin functions?	Notes
S1/1	MQS_RIGHT	**J3, PIN 50**	SAI1_RXFS	Yes	Controlled by alternative pin function MQS_RIGHT
S2/3	MQS_LEFT	**J3, PIN 48**	SAI1_RXC	Yes	Controlled by alternative pin function MQS_LEFT
S3/5	GND	**GND**			
S4/7	AUDIO_TXFS	**J1, PIN 54**	SAI1_TXFS	Yes	Controlled by alternative pin function SAI1_TXFS
S5/9	AUDIO_RXD	**J1, PIN 50**	SAI1_RXD	Yes	Controlled by alternative pin function SAI1_RXD
S6/11	AUDIO_TXC	**J1, PIN 52**	SAI1_TXC	Yes	Controlled by alternative pin function SAI1_TXC
S7/13	AUDIO_TXD	**J1, PIN 56**	SAI1_TXD	Yes	Controlled by alternative pin function SAI1_TXD
S8/15	AUDIO_MCLK	**J1, PIN 67**	SAI1_MCLK	Yes	Controlled by alternative pin function SAI1_MCLK
S9/17	GND	**GND**			
S10/19	SPDIF_IN				
S11/21	SPDIF_OUT				
S12/23	CAN2_TX	**J1, PIN 25**	GPIO1_IO15	Yes	Controlled by alternative pin function CAN2_TX
S13/25	CAN2_RX	**J1, PIN 34**	GPIO1_IO14	Yes	Controlled by alternative pin function CAN2_RX
S14/27	CAN1_TX	**J1, PIN 32**	GPIO1_IO13	Yes	Controlled by alternative pin function CAN1_TX
S15/29	CAN1_RX	**J1, PIN 30**	GPIO1_IO12	Yes	Controlled by alternative pin function CAN1_RX
S16/31	GND	**GND**			
S17/33	LVDS1_D3_P				LVDS interface #1 not assigned on this board.
S18/35	LVDS1_D3_N				LVDS interface #1 not assigned on this board.
S19/37	GPIO	**J1, PIN 37**	GPIO1_IO02	Yes	
S20/39	LVDS1_D2_P				LVDS interface #1 not assigned on this board.
S21/41	LVDS1_D2_N				LVDS interface #1 not assigned on this board.
S22/43	GND	**GND**			
S23/45	LVDS1_D1_P				LVDS interface #1 not assigned on this board.
S24/47	LVDS1_D1_N				LVDS interface #1 not assigned on this board.
S25/49	GND	**GND**			
S26/51	LVDS1_D0_P				LVDS interface #1 not assigned on this board.
S27/53	LVDS1_D0_N				LVDS interface #1 not assigned on this board.
S28/55	GND	**GND**			
S29/57	LVDS1_CLK_P				LVDS interface #1 not assigned on this board.
S30/59	LVDS1_CLK_N				LVDS interface #1 not assigned on this board.
S31/61	GND	**GND**			
S32/63	LVDS0_D3_P	**Indirectly RGB display data**	LVDS_DATA3_P	No	Connected to LVDS transmitter on uCOM Adapter Board.
S33/65	LVDS0_D3_N	**Indirectly RGB display data**	LVDS_DATA3_N	No	Connected to LVDS transmitter on uCOM Adapter Board.
S34/67	GPIO	**J2, PIN 94**	ENET1_CRS	Yes	
S35/69	LVDS0_D2_P	**Indirectly RGB display data**	LVDS_DATA2_P	No	Connected to LVDS transmitter on uCOM Adapter Board.
S36/71	LVDS0_D2_N	**Indirectly RGB display data**	LVDS_DATA2_N	No	Connected to LVDS transmitter on uCOM Adapter Board.
S37/73	GND	**GND**			
S38/75	LVDS0_D1_P	**Indirectly RGB**	LVDS_DATA1_P	No	Connected to LVDS transmitter on uCOM Adapter Board.

		display data			
S39/77	LVDS0_D1_N	**Indirectly RGB display data**	LVDS_DATA1_N	No	Connected to LVDS transmitter on uCOM Adapter Board.
S40/79	GND	**GND**			
S41/81	LVDS0_D0_P	**Indirectly RGB display data**	LVDS_DATA0_P	No	Connected to LVDS transmitter on uCOM Adapter Board.
S42/83	LVDS0_D0_N	**Indirectly RGB display data**	LVDS_DATA0_N	No	Connected to LVDS transmitter on uCOM Adapter Board.
S43/85	GND	**GND**			
S44/87	LVDS0_CLK_P	**Indirectly RGB display data**	LVDS_CLK_P	No	Connected to LVDS transmitter on uCOM Adapter Board.
S45/89	LVDS0_CLK_N	**Indirectly RGB display data**	LVDS_CLK_N	No	Connected to LVDS transmitter on uCOM Adapter Board.
S46/91	I2C-A_SDA	**J1, PIN 43**	I2C1_SDA	No	Controlled by alternative pin function I2C1_SDA. Signal must be I2C1_SDA since the signal is connected to on-board PMIC.
S47/93	I2C-A_SCL	**J1, PIN 41**	I2C1_SCL	No	Controlled by alternative pin function I2C1_SCL. Signal must be I2C1_SDA since the signal is connected to on-board PMIC.
S48/95	I2C-B_SDA	**J1, PIN 47**	I2C2_SDA	Yes	Controlled by alternative pin function I2C2_SDA
S49/97	I2C-B_SCL	**J1, PIN 45**	I2C2_SCL	Yes	Controlled by alternative pin function I2C2_SCL
S50/99	HDMI/I2C-C_SDA	**J3, PIN 26**	I2C3_SDA	Yes	Controlled by alternative pin function I2C3_SDA
S51/101	HDMI/I2C-C_SCL	**J3, PIN 24**	I2C3_SCL	Yes	Controlled by alternative pin function I2C3_SCL
S52/103	TP_RST	**J2, PIN 82**	EPDC_GDSP	Yes	Controlled by alternative pin function GPIO2_IO27
S53/105	TP_IRQ	**J2, PIN 80**	EPDC_GDRL	Yes	Controlled by alternative pin function GPIO2_IO26
S54/107	DISP_PWR_EN	**J2, PIN 78**	EPDC_GDOE	Yes	Controlled by alternative pin function GPIO2_IO25
S55/109	BL_PWR_EN	**J2, PIN 76**	EPDC_GDCLK	Yes	Controlled by alternative pin function GPIO4_IO24
S56/111	BL_PWM	**J1, PIN 33**	GPIO1_IO01	Yes	Controlled by alternative pin function PWM1_OUT.
S57/113	GND	**GND**			
S58/115	LCD_R0	**J3, PIN 59**	LCD1_DATA16	Yes	
S59/117	LCD_R1	**J3, PIN 61**	LCD1_DATA17	Yes	
S60/119	LCD_R2	**J3, PIN 63**	LCD1_DATA18	Yes	
S61/121	LCD_R3	**J3, PIN 65**	LCD1_DATA19	Yes	
S62/123	LCD_R4	**J3, PIN 69**	LCD1_DATA20	Yes	
S63/125	LCD_R5	**J3, PIN 71**	LCD1_DATA21	Yes	
S64/127	LCD_R6	**J3, PIN 73**	LCD1_DATA22	Yes	
S65/129	LCD_R7	**J3, PIN 75**	LCD1_DATA23	Yes	
S66/131	LCD_G0	**J3, PIN 39**	LCD1_DATA08	Yes	
S67/133	LCD_G1	**J3, PIN 41**	LCD1_DATA09	Yes	
S68/135	LCD_G2	**J3, PIN 43**	LCD1_DATA10	Yes	
S69/137	LCD_G3	**J3, PIN 45**	LCD1_DATA11	Yes	
S70/139	LCD_G4	**J3, PIN 49**	LCD1_DATA12	Yes	
S71/141	LCD_G5	**J3, PIN 51**	LCD1_DATA13	Yes	
S72/143	LCD_G6	**J3, PIN 53**	LCD1_DATA14	Yes	
S73/145	LCD_G7	**J3, PIN 55**	LCD1_DATA15	Yes	
S74/147	GND	**GND**			

S75/149	LCD_B0	**J3, PIN 19**	LCD1_DATA00	Yes	
151	Non existing pin				
153	Non existing pin				
155	Non existing pin				
S76/157	LCD_B1	**J3, PIN 21**	LCD1_DATA01	Yes	
S77/159	LCD_B2	**J3, PIN 23**	LCD1_DATA02	Yes	
S78/161	LCD_B3	**J3, PIN 25**	LCD1_DATA03	Yes	
S79/163	LCD_B4	**J3, PIN 29**	LCD1_DATA04	Yes	
S80/165	LCD_B5	**J3, PIN 31**	LCD1_DATA05	Yes	
S81/167	LCD_B6	**J3, PIN 33**	LCD1_DATA06	Yes	
S82/169	LCD_B7	**J3, PIN 35**	LCD1_DATA07	Yes	
S83/171	LCD_CLK	**J3, PIN 89**	LCD1_CLK	Yes	
S84/173	GPIO7	**J3, PIN 85**	LCD1_RESET	Yes	Controlled by alternative pin function GPIO3_IO04.
S85/175	LCD_HSYNC	**J3, PIN 81**	LCD1_HSYNC	Yes	
S86/177	LCD_VSYNC	**J3, PIN 83**	LCD1_VSYNC	Yes	
S87/179	LCD_ENABLE	**J3, PIN 79**	LCD1_ENABLE	Yes	
S88/181	GND	**GND**			
S89/183	AIN_VREF				
S90/185	AIN7				
S91/187	AIN6				
S92/189	AIN5	**J1, PIN 49**	ADC1_IN3	No	
S93/191	AIN4	**J1, PIN 40**	ADC1_IN2	No	
S94/193	AIN3	**J1, PIN 38**	ADC1_IN1	No	
S95/195	AIN2	**J1, PIN 29**	ADC1_IN0	No	
S96/197	AIN1	**J2, PIN 31**	MIPI_DSI_D1_P	No	Non-standard pin allocation.
S97/199	AIN0	**J2, PIN 33**	MIPI_DSI_D1_N	No	Non-standard pin allocation.
S98/201	GND	**GND**			
S99/203	COM board specific	**J2, PIN 25**	MIPI_DSI_D0_P	No	
S100/205	COM board specific	**J2, PIN 27**	MIPI_DSI_D0_N	No	
S101/207	GND	**GND**			
S102/209	COM board specific	**J2, PIN 19**	MIPI_DSI_CLK_P	No	
S103/211	COM board specific	**J2, PIN 21**	MIPI_DSI_CLK_N	No	
S104/213	GND	**GND**			
S105/215	COM board specific				
S106/217	COM board specific				
S107/219	COM board specific				
S108/221	COM board specific				
S109/223	COM board specific				
S110/225	COM board specific				
S111/227	COM board specific	**J3, PIN 96**	SD1_WP	Yes	
S112/229	COM board specific	**J3, PIN 30**	I2C4_SDA	Yes	
S113/231	COM board specific	**J3, PIN 28**	I2C4_SCL	Yes	

S114/233	CSI_HSYNC				
S115/235	CSI_VSYNC				
S116/237	CSI_MCLK				
S117/239	CSI_PCLK				
S118/241	GND	**GND**			
S119/243	CSI_D0				
S120/245	CSI_D1				
S121/247	CSI_D2	**J2, PIN 74**	EPDC_SDSHR	Yes	
S122/249	CSI_D3	**J1, PIN 60**	SD2_CD	Yes	
S123/251	CSI_D4	**J1, PIN 42**	SD2_RESET	Yes	
S124/253	CSI_D5	**J1, PIN 51**	SD2_WP	Yes	
S125/255	CSI_D6				
S126/257	CSI_D7				
S127/259	GND	**GND**			
S128/261	CSI_D3_M				MIPI-CSI interface has only 2 lanes.
S129/263	CSI_D3_P				MIPI-CSI interface has only 2 lanes.
S130/265	GND	**GND**			
S131/267	CSI_D2_M				MIPI-CSI interface has only 2 lanes.
S132/269	CSI_D2_P				MIPI-CSI interface has only 2 lanes.
S133/271	GND	**GND**			
S134/273	CSI_D1_M	**J2, PIN 15**	MIPI_CSI_D1_N	No	
S135/275	CSI_D1_P	**J2, PIN 13**	MIPI_CSI_D1_P	No	
S136/277	GND	**GND**			
S137/279	CSI_D0_M	**J2, PIN 9**	MIPI_CSI_D0_N	No	
S138/281	CSI_D0_P	**J2, PIN 7**	MIPI_CSI_D0_P	No	
S139/283	GND	**GND**			
S140/285	CSI_CLK_M	**J2, PIN 3**	MIPI_CSI_CLK_N	No	
S141/287	CSI_CLK_P	**J2, PIN 1**	MIPI_CSI_CLK_P	No	
S142/289	GND	**GND**			
S143/291	SATA_TX_P				
S144/293	SATA_TX_N				
S145/295	GND	**GND**			
S146/297	SATA_RX_N	**J2, PIN 39**	PCIE_REFCLKIN_N		
S147/299	SATA_RX_P	**J2, PIN 37**	PCIE_REFCLKIN_P		
S148/301	GND	**GND**			
S149/303	GND	**GND**			
S150/305	PCIE_CLK_P	**J2, PIN 43**	PCIE_REFCLKOUT_P	No	
S151/307	PCIE_CLK_N	**J2, PIN 45**	PCIE_REFCLKOUT_N	No	
S152/309	GND	**GND**			
S153/311	PCIE_TX_P	**J2, PIN 55**	PCIE_TX_P	No	
S154/313	PCIE_TX_N	**J2, PIN 57**	PCIE_TX_N	No	
S155/315	GND	**GND**			

S156/317	PCIE_RX_P	**J2, PIN 49**	PCIE_RX_P	No
S157/319	PCIE_RX_N	**J2, PIN 51**	PCIE_RX_N	No
S158/321	GND	**GND**		

7.3 Interface Overview

The table below lists the interfaces that are specified in the EACOM specification (see separate document for details about EACOM boards) and what is supported when the *iMX7 Dual uCOM Board* is mounted on the *uCOM Adapter Board*.

Interface	EACOM specification	iMX7 Dual uCOM Board + uCOM Adapter Board	Notes
UART	3 ports (two 4 wire and one 2 wire)	3 ports	More ports available as alternative pin functions
SPI	2 ports	2 ports	More ports available as alternative pin functions
I2C	3 ports	3 ports	A fourth port is available as alternative pin functions
SD/MMC	2 ports (one 4 databits and one 8 databits)	2 ports	Both ports are 4-bit databus
Parallel LCD	24 databits and CLK/HS/VS/DE	Full support	
LCD support	LCD power ctrl, Backlight power/contrast control, touch panel ctrl (RST and IRQ)	Full support	1 PWM and 4 GPIO
LVDS LCD	2 ports (18/24 bit LVDS data)	1 port	Transmitter on *uCOM Adapter Board*, replication 24-bit parallel RGB data
HDMI (TDMS)		-	
Parallel Camera		-	
Serial Camera	CSI, 4 lane	CSI, 2 lane	
Gigabit Ethernet	2 ports	1 port	Ethernet-PHY on *uCOM Adapter Board*
PCIe	1 port, 1 lane	1 port, 1 lane	
SATA		-	
USB	1 USB3.0 OTG 1 USB3.0 Host 1 USB2.0 Host	2 USB2.0 OTG	
SPDIF	1 TX/RX port	-	
CAN	2 ports	2 ports	
I2S/SSI/AC97	1 port (4 wire synchronous plus MCLK)	1 port	More ports available as alternative pin functions.

Analog audio	Stereo output	-	
GPIO	9 pins	7 pins	More GPIO pins are available as alternative pin functions.
PWM	1 pin	1 pin	More pins are available as alternative pin functions.
ADC	8 inputs	4 inputs	**Note: max 1.8V input**
Type specific	39 pins	MIPI-DSI port	6 type specific pins not used since all i.MX 7Dual SoC pins allocated.
Power	10 VIN, VBAT and 47 GND	10 VIN, VBAT and 47 GND	About 15% of the pins are ground pins.

7.4 I/O voltage

The *iMX7 Dual uCOM Board* is designed to support two different I/O voltages; 1.8V or 3.3V. This section describes how to change between the two.

All *iMX7 Dual uCOM Board* delivered as part of the *iMX7 Dual uCOM Developer's Kit* have 3.3V I/O voltage. Only *iMX7 Dual uCOM Boards* with 3.3V I/O voltage shall be used in combination with the *uCOM Adapter Board*.

The *iMX7 Dual uCOM Board* can be ordered with 1.8V I/O voltage on request. Contact Embedded Artists for information.

Note that changing settings voids product warranty since it involves soldering on the board. Also note that soldering on this board requires a skilled professional. It is very easy to damage the board.

Figure 10 and Figure 11 below illustrates the locations that must be modified.

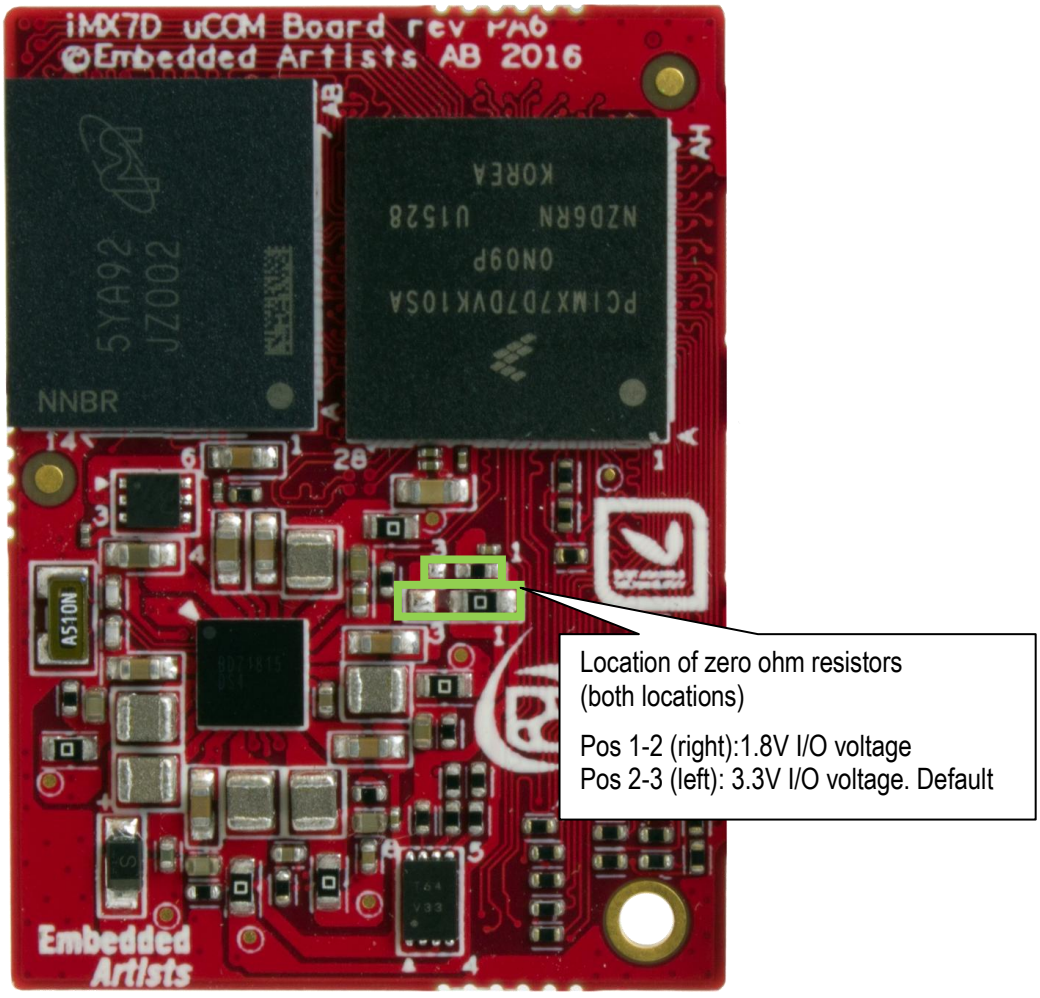


Figure 10 – iMX 7Dual uCOM Board, Top Side Photo

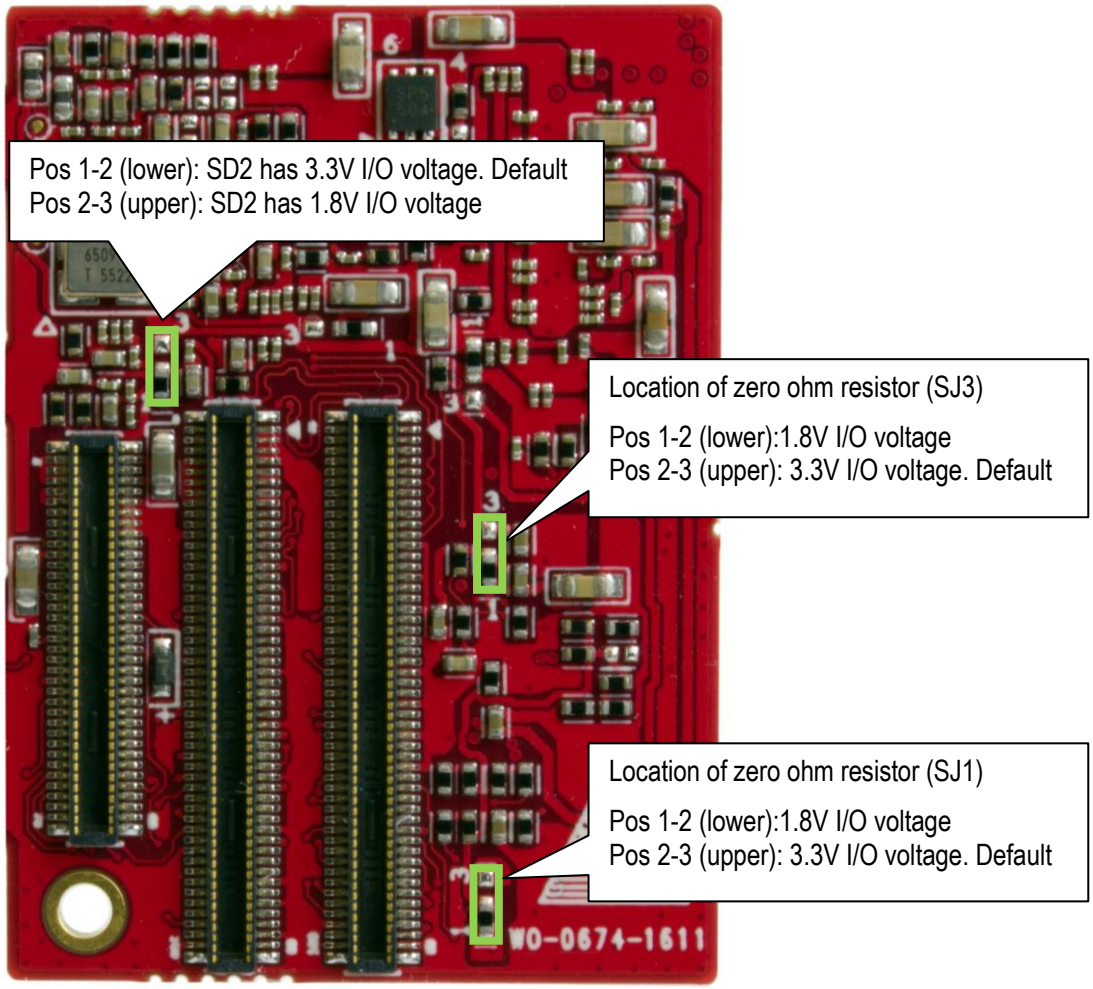


Figure 11 – iMX 7Dual uCOM Board, Bottom Side Photo

8 Boot Options

This chapter presents the different boot settings that the *iMX7 Dual uCOM Board* supports. This chapter will only present how the different options are controlled. Other documents discuss the pros and cons with different options and what general system architectures (with different booting phases) that are suitable in different situations.

The *iMX7 Dual uCOM Board* supports booting from four different sources:

- On-board eMMC Flash
- External SD/MMC memory card, two different interfaces
- External QSPI Flash (on *uCOM Adapter Board*)
- USB OTG download (also called 'serial download')

There are three main boot modes that controls which boot source to use.

- Boot according to how internal (i.MX 7Dual on-chip) OTP fuses have been programmed
  - Normally eMMC is selected but if a QSPI flash or memory card interface is present on the carrier board it is possible to select these sources as well.
  - This mode is selected by leaving the two signals BOOT_MODE0 and BOOT_MODE1 floating. Signal E2PROM_WP should be left floating.
  - Note that ***iMX7 Dual uCOM Boards*** **have not programmed the on-chip OTP fuses**. Users have full control over these. This mode can only be used after having programmed the OTP fuses. This document does not describe how to program the OTP fuses.
- Boot according to external configuration pull-up/pull-down resistors
  - Since the OTP fuses on the *iMX7 Dual uCOM Board* are not programmed, this is the booting method used on the *iMX7 Dual uCOM Developer's Kit*. The *uCOM Adapter Board* has an 8-pos slider switch to select boot source.
  - Normally eMMC is selected but if a QSPI flash or memory card interface is present on the carrier board it is possible to select these sources as well.
  - This mode is selected by pulling signal BOOT_MODE1 high (10K pullup to VIN_3V3). Signals BOOT_MODE0 and E2PROM_WP should be left floating. See the *uCOM Adpater Board* schematic for a reference implementation.
- Boot from USB OTG interface
  - This mode is used in production to download the first stage bootloader and is typically not used by *iMX7 Dual uCOM Board* integrators. Sometimes this mode is called "Recovery mode".
    - Note that a special procedure is needed on rev A boards to enter this mode. See section 12.3 for details.
  - This mode is activated by pulling signal E2PROM_WP low. Signals BOOT_MODE0 and BOOT_MODE1 should be left floating.

There is an 8-pos slider switch on the *uCOM Adapter Board* to select boot source, i.e., from where the i.MX 7Dual SoC starts downloading code to start executing from. The picture below illustrates the location of the slider switch.

Note that if the OTP fuses have been programmed, their settings will override the slider switches.

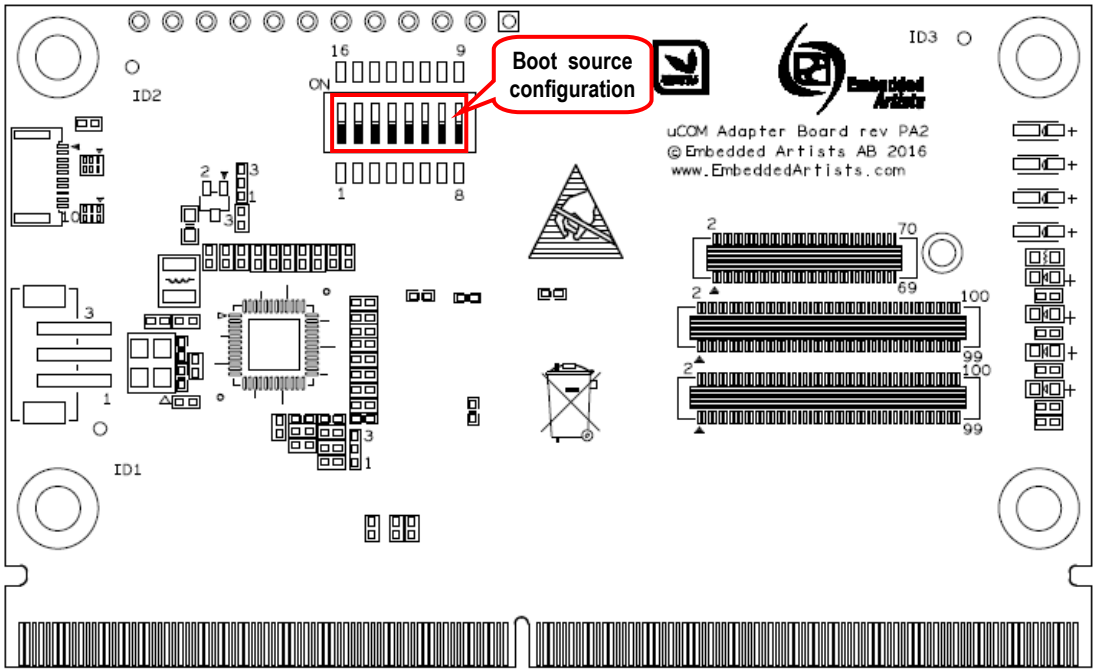
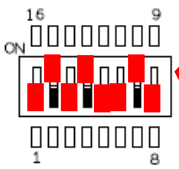
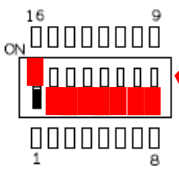
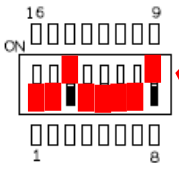
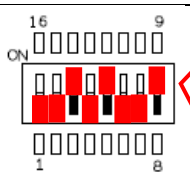


Figure 12 –uCOM Adapter Board Boot Control Slider Switches Location

The table below presents ho to set the slider switches for different boot modes and boot sources.

Boot Modes	Slider Settings
Boot according to slider switches - **on-board eMMC Flash** Note that if OTP fuse BT_FUSE_SEL = 1 then the system will boot according to OTP fuses, i.e., it overrides this setting.	 **Slider#1 in off-position (down)** **Slider#2 in on-position (up)** **Slider#3 in off-position (down)** **Slider#4 in on-position (up)** **Slider#5 in off-position (down)** **Slider#6 in off-position (down)** **Slider#7 in on-position (up)** **Slider#8 in off-position (down)**
Boot according to slider switches - **external QSPI Flash** Note that if OTP fuse BT_FUSE_SEL = 1 then the system will boot according to OTP fuses, i.e., it overrides this setting.	 **Slider#1 in on-position (up)** **Slider#2 in off-position (down)** **Slider#3 in off-position (down)** **Slider#4 in off-position (down)** **Slider#5 in off-position (down)** **Slider#6 in off-position (down)** **Slider#7 in off-position (down)** **Slider#8 in off-position (down)**
Boot according to slider switches - **external SD memory card on eSDHC1** Note that if OTP fuse BT_FUSE_SEL = 1 then the system will boot according to OTP fuses, i.e., it overrides this setting.	 **Slider#1 in off-position (down)** **Slider#2 in off-position (down)** **Slider#3 in on-position (up)** **Slider#4 in off-position (down)** **Slider#5 in off-position (down)** **Slider#6 in off-position (down)** **Slider#7 in off-position (down)** **Slider#8 in on-position (up)**

Boot according to slider switches - **external SD memory card on eSDHC2** Note that if OTP fuse BT_FUSE_SEL = 1 then the system will boot according to OTP fuses, i.e., it overrides this setting.	 **Slider#1 in off-position (down)** **Slider#2 in off-position (down)** **Slider#3 in on-position (up)** **Slider#4 in off-position (down)** **Slider#5 in on-position (up)** **Slider#6 in off-position (down)** **Slider#7 in off-position (down)** **Slider#8 in on-position (up)**

9 Power Modes

One of the primary features of the i.MX7 SoC is low power consumption. The *iMX7 COM Board* supports these features in the design. There are several different power modes that gives varying trade-offs between active functionality and power consumption. The table below lists, from lowest to highest power consumption, the available mode. There are three different versions of what is called the *Low Power mode*. These are variations on the basic mode.

Note that software support for these power modes vary between BSPs.

Mode	Description	DRAM state
Off	All power rails are off	Off
SNVS (RTC only)	Only RTC and tamper detection logic is active	Off
LPSR	Low Power State Retention mode: This is an extension of the SNVS mode. All digital/analog modules are powered down but 16 GPIOs are also active for wakeup.	Off or DRAM stay in self-refresh, controlled by SW, pin SNVS_TAMPER9.
Low Power: Deep Sleep or Suspend	CPU power gated, most of the peripherals are power gated. All system clock shut off.	DRAM stay in self-refresh.
Low Power: Low Power Idle	CPU power gated, most of the peripherals are clock gated. Timer or other low speed peripheral can be running at 1MHz clock.	DRAM stay in self-refresh.
Low Power: System Idle	CPU automatically clock gated when in WFI state. Most of the peripherals remain active and running at 24MHz clock.	DRAM stay in self-refresh.
RUN	All external power rails are on, CPU is active and running, other internal module can be on/off based on application	DRAM stay in self-refresh.

Valid power modes transitions are presented in the state machine diagram below.

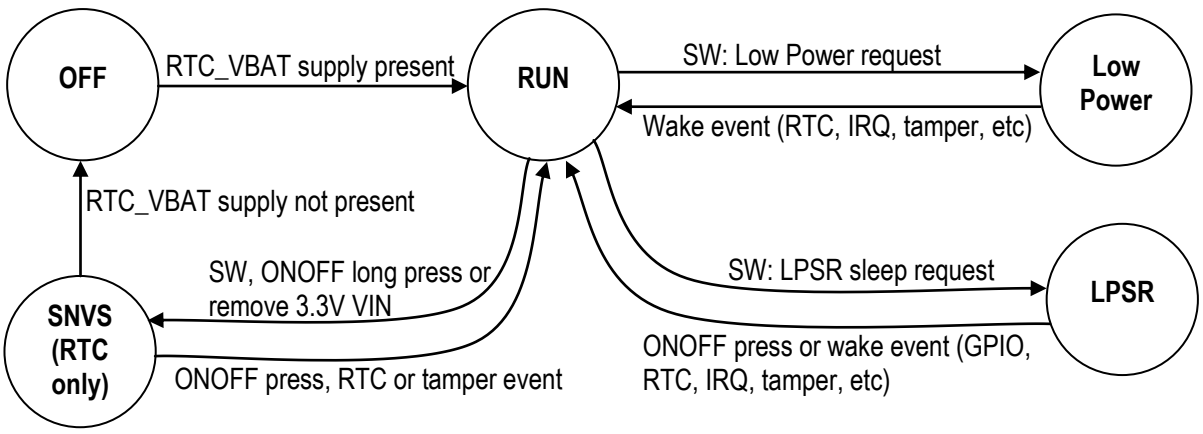


Figure 13 – i.MX7 Power Modes Transitions

The table below presents the different power supply voltage rails and their state in different power modes.

Power Rail	Off	SVNS (RTC only)	LPSR	Low Power	Run
VDD_ARM (CPU cores)	OFF	OFF	OFF	ON/OFF	ON
VDD_SOC	OFF	OFF	OFF	ON	ON
VDD_DRAM	OFF	OFF	ON/OFF	ON	ON
On-board Ethernet PHY	OFF	OFF	OFF	ON/OFF	ON/OFF
Off-board peripherals controlled by PERI_PWR_EN	OFF	OFF	OFF	ON	ON
LPSR I/O	OFF	OFF	ON	ON	ON
3.3V VIN	OFF	OFF	ON	ON	ON
RTC_VBAT	OFF	ON	ON	ON	ON

The different power modes are presented in more detail below.

9.1 Power Mode: OFF

This mode is self explanatory; all power rails are off.

9.2 Power Mode: SNVS (RTC only)

In this mode, only the RTC_VBAT power rail is on. All other power rails are off. The on-board Real-Time Clock (RTC) is running, i.e., keeping track of time.

Note that the power consumption of the RTC can quickly drain a standard (lithium) coin cell. A rechargeable battery solution is recommended. If this is not an option, an ultra-low power RTC (few uA) can be placed on the carrier board instead. In case, the RTC_VBAT power rail shall be connected to the 3.3V VIN power rail.

9.3 Power Mode: LPSR

This mode is an extension of the SNVS (RTC only) mode. In this state, the 3.3V VIN power rail is on but the CPUs and all digital/analog modules are powered down. IO rails are also off. The 16 LPSR IO pins are however active in this mode. One of the LPSR pins is used internally on the board (for watchdog functionality) but 15 LPSR IO pins are available for external expansion. These pins (GPIO1_IO01 - GPIO1_IO15) will keep their state in the LPSR mode and can be used to wake up the system again.

The LPDDR3 DRAM can optionally be kept in self-refresh mode, else it is switched off. Pin SNVS_TAMPER9 controls the self-refresh mode. A low pin level keeps the DRAM in self-refresh. A high pin level shuts down the DRAM.

9.4 Power Modes: Low Power

In this mode, the CPU is not running but the DRAM stays in self-refresh mode. There are three variations with different levels of power save and resulting response times.

- Suspend/Deep Sleep
  This is the lowest power consumption mode of the three. All clocks and peripherals that are not used are turned off. Exiting this mode take the longest of these three modes.

- Low Power Idle
  In this mode, some peripherals blocks are active and some are not. The time to exiting this mode is between the other two modes.
- System Idle
  This is the highest power consumption mode of the three. This mode can be entered automatically if there is no system activity (i.e., no thread running). When entering this mode, the peripheral blocks that shall still be active are defined. Exiting this mode is the fastest of the three modes, resulting in short interrupt response.

9.5 Power Mode: RUN

In this mode, the system is up and running. All power rails are on. Functionality, like the external Ethernet PHY, can be controlled via software to save power. The VDD_ARM (core voltage) can be adjusted via Dynamic Voltage Frequency Scaling (DVFS) techniques to reduce power consumption slightly. Basically, if the system load is low, the core operating frequency can be reduced and this allows the core voltage to also be reduced.

10 Technical Specification

10.1 Absolute Maximum Ratings

All voltages are with respect to ground, unless otherwise noted. Stress above these limits may cause malfunction or permanent damage to the board.

Symbol	Description	Min	Max	Unit
VSYS	System voltage	0	6	V
DCIN	Battery charger voltage	0	30	V
VBAT	(Li-ion) Battery voltage	0	6	V
RTC_VBAT	RTC supply voltage	-0.3	3.6	V
VIO	Vin/Vout (I/O VDD + 0.3): 3.3V IO Vin/Vout (I/O VDD + 0.3): 1.8V IO	-0.4 -0.4	3.6 2.1	V V
VADCIN	Analog input voltage on ADC inputs	-0.3	1.9	V
USB_xx_VBUS	USB VBUS signals	-0.3	5.25	V
USB_xx_DP/DN	USB data signal pairs	-0.3	3.63	V

10.2 Recommended Operating Conditions

All voltages are with respect to ground, unless otherwise noted.

Symbol	Description	Min	Typical	Max	Unit
VSYS	System voltage	2.9	3.3	5.5	V
DCIN	Battery charger voltage	3.5	5	28	V
VBAT	(Li-ion) Battery voltage		3.6		V
RTC_VBAT	RTC supply voltage **Note:** This voltage must remain valid at all times for correct operation of the board (including, but not limited to the RTC).	2.6	3.0	3.6	V
USB_xx_VBUS	USB VBUS signals	4.4	5	5.25	V

10.3 Power Ramp-Up Time Requirements

Input supply voltages (VIN and RTC_VBAT) shall have smooth and continuous ramp from 10% to 90% of final set-point. Input supply voltages shall reach recommended operating range in 1-20 ms.

10.4 Electrical Characteristics

For DC electrical characteristics, see i.MX 7Dual Datasheet. Depending on I/O operating voltage point, OVDD is either 3.3V or 1.8V.

10.4.1 Reset Output Voltage Range

The reset output is an open drain output with a 10 Kohm pull-up resistor to VDD IO (typically 3.3V). Maximum output voltage when active is 0.4V.

10.4.2 PMIC Reset Input

The reset input is triggered by pulling the reset input low (0.9 V max) for 20 uS minimum.

10.5 Power Consumption

There are several factors that determine power consumption of the *iMX7 Dual uCOM Board*, like input voltage, operating temperature, LPDDR3 activity, operating frequencies for the different cores, DVFS levels and software executed (i.e., Linux distribution).

The values presented are typical values and should be regarded as an estimate. Always measure current consumption in the real system to get a more accurate estimate.

Symbol	Description (VIN = 3.3V, Toperating = 25°C)	Typical	Max observed over 1 sec period	Unit
I_{VIN}_MAX	Maximum CPU load, 996MHz ARM frequency, without Ethernet		320	mA
I_{VIN}_IDLE	System idle state, uBoot prompt Linux prompt, without Ethernet Linux prompt, with Ethernet		174 180 350	mA
I_{VIN}_DSM	Deep-Sleep mode (DSM), aka "Dormant mode" or "Suspend-to-RAM" in Linux BSP	46		mA
I_{VIN}_STB	Linux standby	53		mA
I_{VBAT}_BACKUP	Current consumption to keep internal RTC running	116		uA
I_{VIN}_A7ACT	Android 7 Desktop active	182	319	mA
I_{VIN}_A7OFF	Android 7 Display off	57	66	mA
I_{VIN}_A7HALT	Android 7 Halted	15		mA

Linux version 4.1.15-2.0.3 used. Image: core-image-base

10.6 Mechanical Dimensions

The table below presents the mechanical dimensions of the module.

Dimension	Value (±0.1 mm)	Unit
Module width	27	mm
Module height	37	mm
Module top side height	1.4	mm
Module bottom side height	1.4	mm
PCB thickness	1.6	mm
Mounting hole diameter	2.2	mm
Module weight	5 ±1 gram	gram

The picture below show the mechanical details of the *iMX7 Dual uCOM Board*. The outer measurement is only 27 x 37 mm. Note that the picture below is seen from the bottom side.

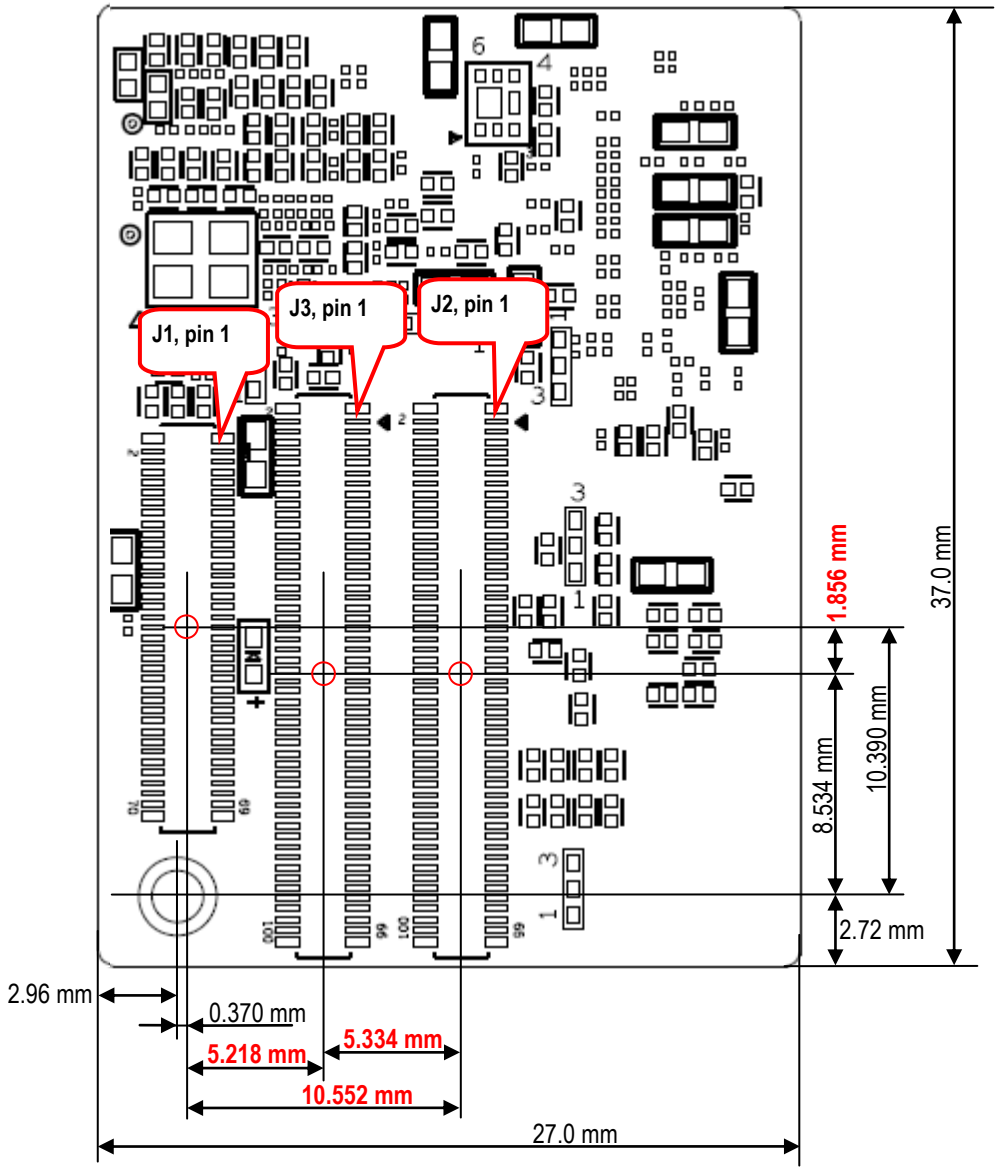


Figure 14 – iMX7 Dual uCOM Board Mechanical Outline, Seen From Bottom Side

Note that placement of the connectors on the carrier board is very important. They must be parallel and have a placement tolerance of +-0.1mm (non-accumulative). Make sure the relative measures between the connectors (marked with red in the picture above) are correct.

Note that the mounting hole location shall be measured relative to the three connectors, not relative to the pcb edge.

Note that the connector numbering above is J1, J3, J2.

Below is a picture illustrating how the carrier board connectors will look like, seen from carrier board top side.

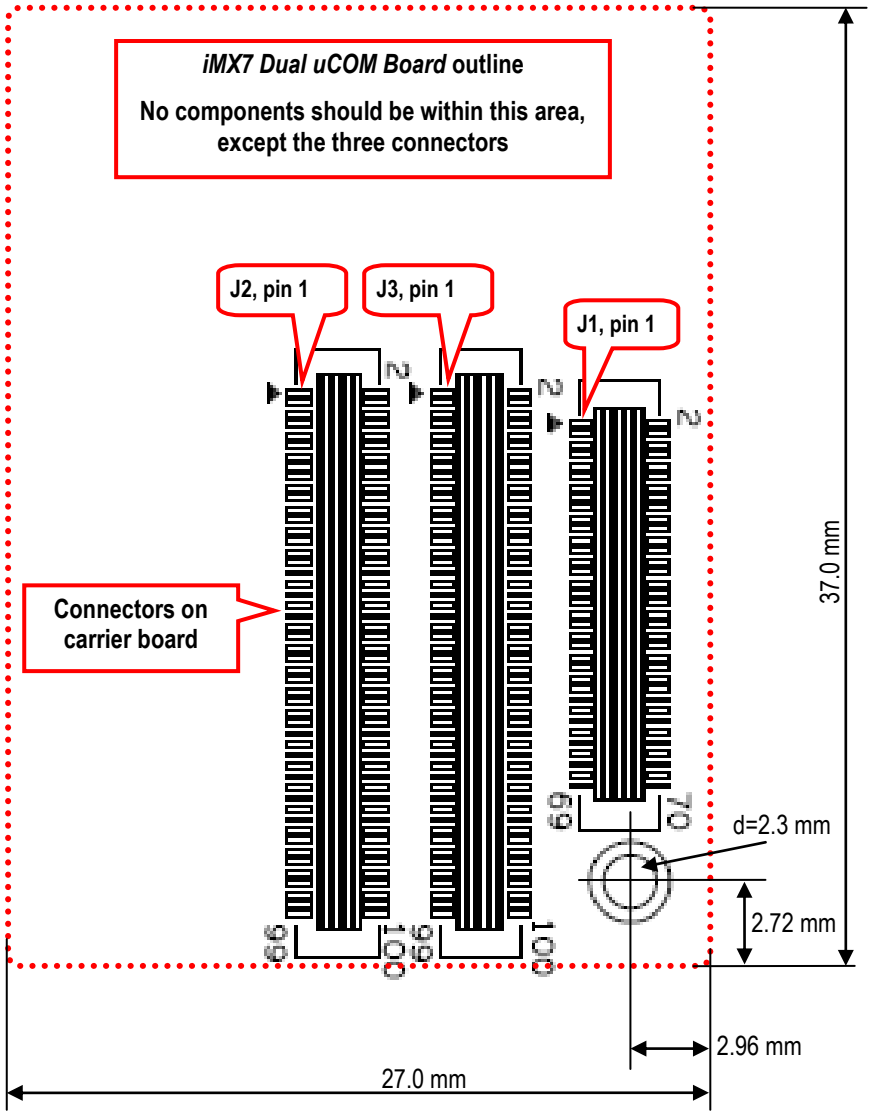


Figure 15 – iMX7 Dual uCOM Board Expansion Connectors on Carrier Board, Seen From Top Side

Since the stacking height is only 1.5mm in normal case, make sure no components other than the three connectors are within the dotted red line. When using 3mm stacking height it is possible to have low-profile components under the *iMX7D uCOM Board*. The picture below illustrates the principal dimensions.

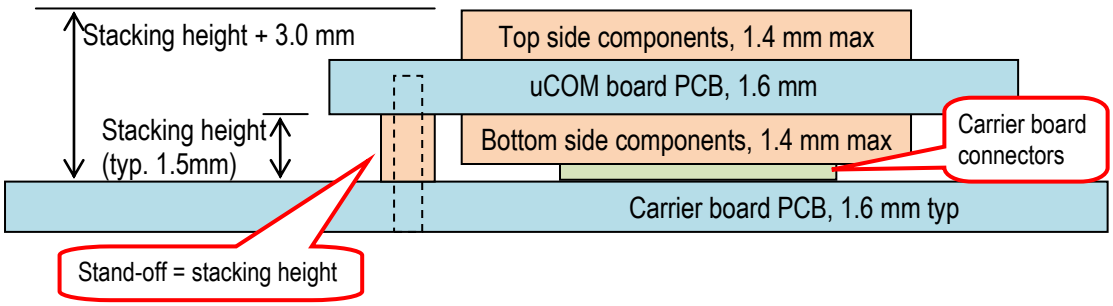


Figure 16 – uCOM Board Mounting on Carrier Board, Stacking Height

10.6.1 DF40C Socket

The headers mounted on the *iMX7 Dual uCOM Board* are DF40C-70DP-0.4V(51) and DF40C-100DP-0.4V(51).

The receptacles that are needed on the carrier board are, depending on stacking height:

Connector	1.5 mm stacking height (standard)	3.0 mm stacking height
70-pos (J1)	DF40C-70DS-0.4V(51) HRS number: 684-4016-5 51	DF40HC(3.0)-70DS-0.4V HRS number: 684-4138-2 51
100-pos (J2, J3)	DF40C-100DS-0.4V(51) HRS number: 684-4033-4 51	DF40HC(3.0)-100DS-0.4V HRS number: 684-4151-0 51

If any of the connectors are not needed on the carrier board design, these do not have to be mounted. This typically apply to J2 and J3.

Note that placement is of the connectors on the carrier board is very important. They must be parallel and have a placement tolerance of +-0.1mm (non-accumulative).

10.6.2 Module Assembly Hardware

The *iMX7 Dual uCOM Board* has a 2.3mm mounting hole for securing a good mechanical mounting. Use an M2 screw and an associated standoff that has the same height as the stacking height (1.5mm or 3 mm, depending on carrier board connectors). The pictures below illustrates how an M2 nut can be used to create the 1.5-1.6mm distance between the uCOM and carrier boards. The pictures also illustrates that a small piece of isolation tape/film (Kapton® polyimide) must be used if there is a risk that the screw head touches the nearby resistors on the uCOM pcb.

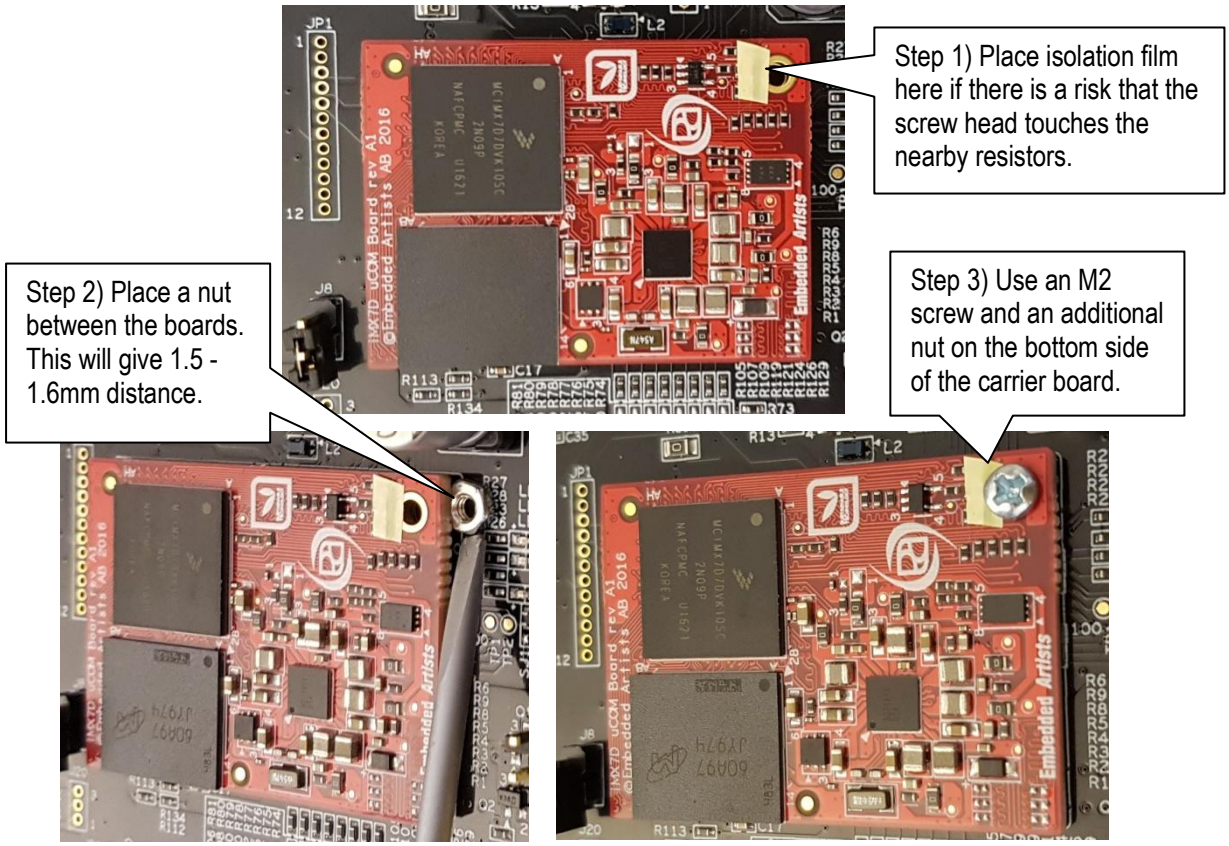


Figure 17 – iMX7 Dual uCOM Board Assembly

10.7 Environmental Specification

10.7.1 Operating Temperature

Ambient temperature (T_A)

Parameter		Min	Max	Unit
Operating temperature range:	commercial temperature range industrial temperature range	0 -20	75[1] 85[1]	°C °C
Storage temperature range		-40	85	°C
Junction temperature i.MX 7Dual SoC, operating:	comm. temp. range ind. temp. range.	0 -20	95 105	°C

[1] Depends on cooling solution.

10.7.2 Relative Humidity (RH)

Parameter	Min	Max	Unit
Operating: 0°C ≤ T_A ≤ 60°C, non-condensing	10	90	%
Non-operating/Storage: -40°C ≤ T_A ≤ 85°C, non-condensing	5	90	%

10.8 Thermal Design Considerations

Heat dissipation from the i.MX 7Dual SoC depending on many operating conditions, like operating frequency, operating voltage, activity type, activity cycle duration and duty cycle. Dissipated heat is less than 1 Watt.

If external cooling is needed, or not, depends on dissipated heat and ambient temperature range. In most cases it is possible to operate the *iMX7 Dual uCOM Board* without external cooling, at least with ambient temperature up to +60° Celsius. Above this, care must be taken not to exceed max junction temperature of the i.MX 7Dual.

The i.MX 7Dual SoC and PMIC (BD71815GW) together implement DVFS (Dynamic Voltage and Frequency Scaling) and Thermal Throttling. This enables the system to continuously adjust operating frequency and voltage in response to changes in workload and temperature. In general this result in higher performance at lower average power consumption.

The .iMX 7Dual SoC has an integrated temperature sensor for monitoring the junction (i.e., die) temperature, which affect several factors:

- A lower junction temperature, Tj, will result in longer SoC lifetime.
- A lower die temperature will result in lower power consumption due to lower leakage current.

10.8.1 Thermal Parameters

The i.MX 7Dual SoC thermal parameters are listed in the table below.

Parameter	Typical	Unit
Thermal Resistance, CPU Junction to ambient ($R_{\theta JA}$), natural convection	32.6	°C/W
Thermal Resistance, CPU Junction to package top (ψ_{JT})	0.2	°C/W

10.9 Product Compliance

Visit Embedded Artists' website at http://www.embeddedartists.com/product_compliance for up to date information about product compliances such as CE, RoHS2, Conflict Minerals, REACH, etc.

11 Functional Verification and RMA

There is a separate document that presents a number of functional tests that can be performed on the *iMX7 Dual uCOM Board* to verify correct operation on the different interfaces. Note that these tests must be performed on the carrier board that is supplied with the *iMX7 Dual uCOM Developer's Kit* and with a precompiled kernel from Embedded Artists.

The tests can also be done to troubleshoot a board that does not seem to operate properly. It is strongly advised to read through the list of tests and actions that can be done before contacting Embedded Artists. The different tests can help determine if there is a problem with the board, or not. For return policy, please read Embedded Artists' General Terms and Conditions document (http://www.embeddedartists.com/sites/default/files/docs/General_Terms_and_Conditions.pdf).

12 Things to Note

This chapter presents a number of issues and considerations that users must note.

12.1 Shared Pins and Multiplexing

The i.MX 7Dual SoC has multiple on-chip interfaces that are multiplexed on the external pins. It is not possible to use all interfaces simultaneously and some interface usage is prohibited by the *iMX7 Dual uCOM* on-board design. Check if the needed interfaces are available to allocation before starting a design. See chapter 4 for details.

12.2 I2C Pull-up Resistors Missing on uCOM Adapter Board, rev PA2

I2C channel 2 and 3 are missing I2C pull-up resistors on the uCOM Adapter Board, rev PA2. If using any of these I2C channels when the *uCOM Adapter board* is mounted on the *COM Carrier board* 2.2Kohm pull-up resistors must be added. The signals can be accessed at the expansion connectors.

12.3 Entering USB OTG Boot-mode (Manufacturing Tool), rev A

Note that this only affects boards up to, and including, rev A.

If the *iMX7 Dual uCOM board* is powered from an external 3.3-5.5V supply (as opposed to a battery powered design), a special procedure is needed to make it possible to use the *Manufacturing Tool* (which is a program that is used to update the bootloader and Linux images - it might be needed during initial program development).

Temporary connect a voltage between 3.5-28V (5V typical) to **DCIN**, for example the VBUS signals from the USB OTG interface that is used to connect to the *Manufacturing Tool* application. This will allow the iMX7 USB interface to startup correctly in USB OTG bootloader mode.

The *uCOM Adapter Board* has a cable jumper to accomplish this temporary connection of +5V to DCIN. See picture below .

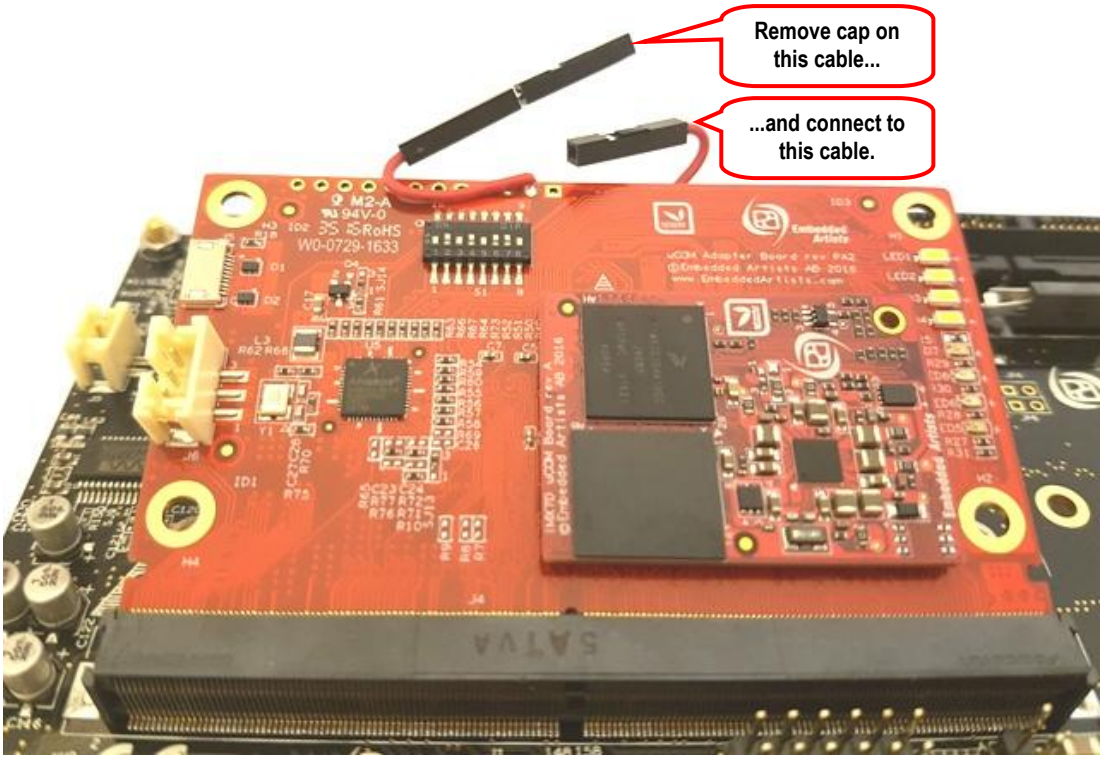


Figure 18 – uCOM Adapter Board with Special Cable

12.4 Cannot Access Some Memory Cards

Some memory cards have a very high current consumption peak when turned on. This can cause problems accessing the memory cards because there voltage dip becomes too big.

As a solution, move the zero-ohm resistor in SJ8 to position 2-3 (instead of the default position: 1-2). This will power the memory card from the *COM Carrier Board* 3.3V supply instead of a supply from the *iMX7 Dual uCOM board*.

The picture below illustrates where SJ8 can be found on the bottom side of the *COM Carrier Board*.

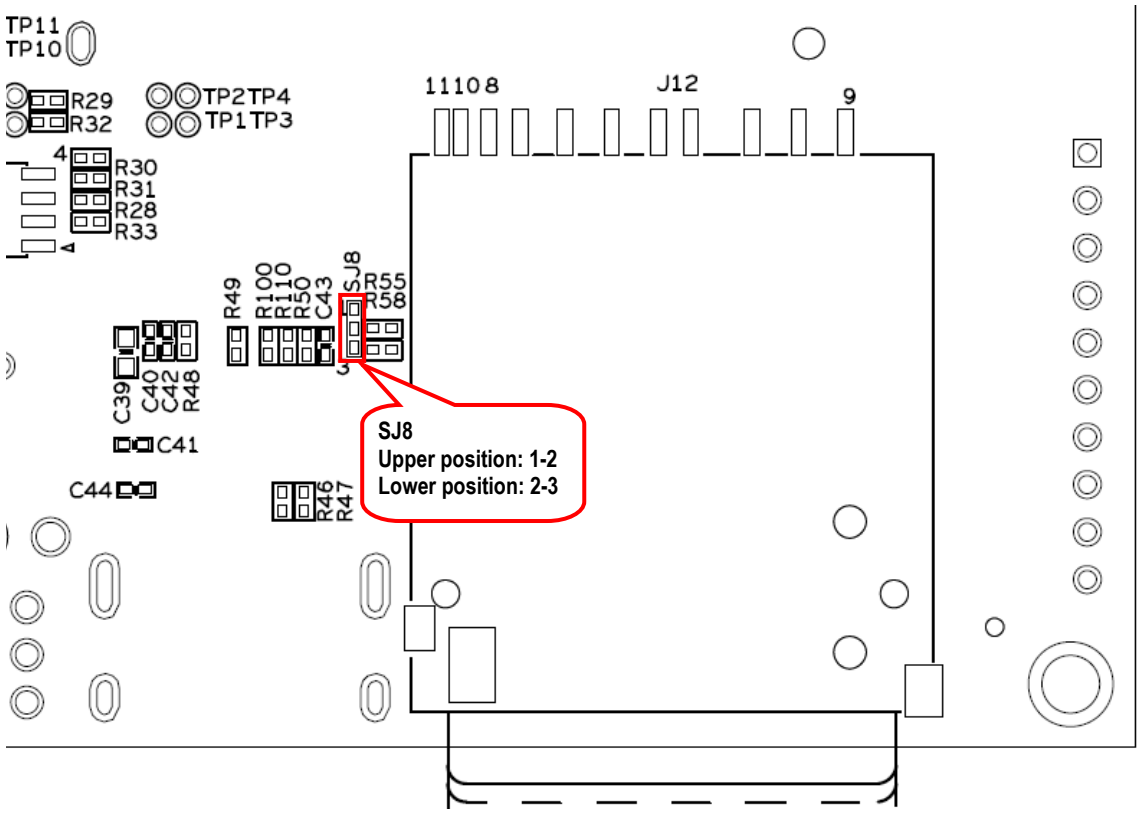


Figure 19 – Location of SJ8 on COM Carrier Board

12.5 Be Careful when Mounting/Detaching the uCOM Board

The DF40C connectors on both the *iMX7 Dual uCOM Board* and *uCOM Adapter Board* **are fragile**.

When mounting the *iMX7 Dual uCOM Board* on the *uCOM Adapter Board*;

- First carefully place the *iMX7 Dual uCOM Board* on top of the connectors on the *uCOM Adapter Board*. Do not press the board in place.
- Secondly, lightly pressing the iMX7 Dual uCOM board, find the correct location where the connectors on the *iMX7 Dual uCOM Board* and *uCOM Adapter Board* match above each other.
- Third, press with even force above all three connectors. Do not press first in one end and then the other end. It is important to press with even force all over the connector area. If not, the connectors can easily be damaged.

When detaching the *iMX7 Dual uCOM Board* from the *uCOM Adapter Board* be very careful. Only make very small movements in each short end of the board. Wiggle the board back and forth (with very small movements, typically in the 0.5 mm range) until the board detach.

12.6 Only Use EA Board Support Package (BSP)

The *iMX7 Dual uCOM board* use multiple on-board interfaces for the internal design, for example PMIC, eMMC and watchdog. Only use the BSP that is delivered from Embedded Artists. Do not change interface initialization and/or pin assignment for the on-board interfaces. Changing BSP settings can result in permanent board failure.

Note that Embedded Artists does not replace iMX7 Dual uCOM Boards that have been damaged because of improper interface initialization and/or improper pin assignment.

12.7 OTP Fuse Programming

The i.MX 7Dual SoC has on-chip OTP fuses that can be programmed, see NXP documents *iMX 7Dual Datasheet* and *iMX 7Dual Reference Manual* for details. Once programmed, there is no possibility to reprogram them.

iMX7 Dual uCOM Boards are delivered without any OTP fuse programming. It is completely up to the COM board user to decide if OTP fuses shall be programmed and in that case, which ones.

Note that Embedded Artists does not replace iMX7 Dual uCOM Boards because of wrong OTP programming. It's the user's responsibility to be absolutely certain before OTP programming and not to program the fuses by accident.

12.8 Write Protect on Parameter Storage E2PROM

The parameter storage E2PROM contains important system data like DDR memory initialization settings and Ethernet MAC addresses. The content should not be erased or overwritten. The E2PROM is write protected if signal E2PROM_WR (pin P146/300) is left unconnected, i.e. floating. This should always be the case.

Note that all carrier board design should include the possibility to ground this pin.

12.9 Integration - Contact Embedded Artists

It is strongly recommended to contact Embedded Artists at an early stage in your project. A wide range of support during evaluation and the design-in phase are offered, including but not limited to:

- Developer's Kit to simplify evaluation
- Custom Carrier board design, including 'ready-to-go' standard carrier boards
- Display solutions
- Mechanical solutions
- Schematic review of customer carrier board designs
- Driver and application development

The *iMX7 Dual uCOM Board* targets a wide range of applications, such as:

- Portable systems
- HMI/GUI solutions
- Portable medical and health care
- Connected vending machines
- Point-of-Sale (POS) applications
- Access control panels
- Audio
- IP phones
- Smart appliances
- eReaders
- Wearables
- Home energy management systems
- Industrial automation
- HVAC Building and Control Systems

- Smart Grid and Smart Metering
- Smart Toll Systems
- Data acquisition
- Communication gateway solutions
- Connected real-time systems
- ...and much more

For more harsh use and environments, and where fail-safe operation, redundancy or other strict reliability or safety requirements exists, always contact Embedded Artists for a discussion about suitability.

There are application areas that the *iMX7 Dual uCOM Board* is not designed for (and such usage is strictly prohibited), for example:

- Military equipment
- Aerospace equipment
- Control equipment for nuclear power industry
- Medical equipment related to life support, etc.
- Gasoline stations and oil refineries

If not before, **it is essential to contact Embedded Artists before production begins**. In order to ensure a reliable supply for you, as a customer, we need to know your production volume estimates and forecasts. Embedded Artists can typically provide smaller volumes of the *iMX7 Dual uCOM Board* directly from stock (for evaluation and prototyping), but **larger volumes need to be planned**.

The more information you can share with Embedded Artists about your plans, estimates and forecasts the higher the likelihood is that we can provide a reliable supply to you of the *iMX7 Dual uCOM Board*.

12.10 ESD Precaution when Handling iMX7 Dual uCOM Board

Please note that the *iMX7 Dual uCOM Board* come without any case/box and all components are exposed for finger touches – and therefore extra attention must be paid to ESD (electrostatic discharge) precaution, for example use of static-free workstation and grounding strap. Only qualified personnel shall handle the product.

Make it a habit always to first touch the mounting hole (which is grounded) for a few seconds with both hands before touching any other parts of the boards. That way, you will have the same potential as the board and therefore minimize the risk for ESD.

In general touch as little as possible on the boards in order to minimize the risk of ESD damage. The only reasons to touch the board are when mounting/unmounting it on a carrier board.

Note that Embedded Artists does not replace boards that have been damaged by ESD.

12.11 EMC / ESD

The *iMX7 Dual uCOM Board* has been developed according to the requirements of electromagnetic compatibility (EMC). Nevertheless depending on the target system, additional anti-interference measurement may still be necessary to adherence to the limits for the overall system.

The *iMX7 Dual uCOM Board* must be mounted on carrier board (typically an application specific board) and therefore EMC and ESD tests only makes sense on the complete solution.

No specific ESD protection has been implemented on the *iMX7 Dual uCOM Board*. ESD protection on board level is the same as what is specified in the i.MX 7Dual SoC datasheet. **It is strongly advised to implement protection against electrostatic discharges (ESD) on the carrier board** on all

signals to and from the system. Such protection shall be arranged directly at the inputs/outputs of the system.

13 Custom Design

This document specify the standard *iMX7 Dual uCOM Board* design. Embedded Artists offers many custom design services. Contact Embedded Artists for a discussion about different options.

Examples of custom design services are:

- Different memory sizes on LPDDR3 SDRAM and eMMC Flash.
- Different pinning on DF40C connectors.
- Different I/O voltage levels on all or parts of the pins.
- Different board form factor.
- Different input supply voltage range, for example 5V input.
- Single Board Computer solutions, where the core design of the *iMX7 Dual uCOM Board* is integrated together with selected interfaces.
- Replace eMMC Flash with (unmanaged) MLC/SLC NAND Flash.
- Changed internal pinning to make certain pins available.

Embedded Artists also offers a range of services to shorten development time and risk, such as:

- Standard Carrier boards ready for integration
- Custom Carrier board design
- Display solutions
- Mechanical solutions

14 Disclaimers

Embedded Artists reserves the right to make changes to information published in this document, including, without limitation, specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Customer is responsible for the design and operation of their applications and products using Embedded Artists' products, and Embedded Artists accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Embedded Artists' product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. Customer is required to have expertise in electrical engineering and computer engineering for the installation and use of Embedded Artists' products.

Embedded Artists does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Embedded Artists' products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Embedded Artists does not accept any liability in this respect.

Embedded Artists does not accept any liability for errata on individual components. Customer is responsible to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.

Embedded Artists does not accept any liability and no warranty is given for any unexpected software behavior due to deficient components.

Customer is required to take note of manufacturer's specification of used components, for example PMIC and eMMC. Such specifications, if applicable, contains additional information that must be taken note of for the safe and reliable operation. These documents are stored on Embedded Artists' product support page.

All Embedded Artists' products are sold pursuant to Embedded Artists' terms and conditions of sale: http://www.embeddedartists.com/sites/default/files/docs/General_Terms_and_Conditions.pdf

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by Embedded Artists for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN EMBEDDED ARTISTS' TERMS AND CONDITIONS OF SALE EMBEDDED ARTISTS DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF EMBEDDED ARTISTS PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY THE CEO OF EMBEDDED ARTISTS, PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, NUCLEAR, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE.

Resale of Embedded Artists' products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by Embedded Artists

for the Embedded Artists' product or service described herein and shall not create or extend in any manner whatsoever, any liability of Embedded Artists.

This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

14.1 Definition of Document Status

Preliminary – The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Embedded Artists does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information. The document is in this state until the product has passed Embedded Artists product qualification tests.

Approved – The information and data provided define the specification of the product as agreed between Embedded Artists and its customer, unless Embedded Artists and customer have explicitly agreed otherwise in writing.