8-bit AVR Microcontrollers

ATmega324PA

DATASHEET SUMMARY

Introduction

The Atmel® ATmega324PA is a low-power CMOS 8-bit microcontroller based on the AVR® enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega324PA achieves throughputs close to 1MIPS per MHz. This empowers system designer to optimize the device for power consumption versus processing speed.

Feature

High Performance, Low Power Atmel®AVR® 8-Bit Microcontroller Family

- Advanced RISC Architecture
  - 131 Powerful Instructions
  - Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 20 MIPS Throughput at 20MHz
  - On-chip 2-cycle Multiplier
- High Endurance Non-volatile Memory Segments
  - 32KBytes of In-System Self-Programmable Flash Program Memory
  - 1KBytes EEPROM
  - 2KBytes Internal SRAM
  - Write/Erase Cycles: 10,000 Flash/100,000 EEPROM
  - Data Retention: 20 Years at 85°C/100 Years at 25°C(1)
  - Optional Boot Code Section with Independent Lock Bits
    - In-System Programming by On-chip Boot Program
    - True Read-While-Write Operation
  - Programming Lock for Software Security
- Atmel QTouch® Library Support
  - Capacitive Touch Buttons, Sliders and Wheels
  - QTouch and QMatrix acquisition
  - Up to 64 Sense Channels

- JTAG (IEEE std. 1149.1 Compliant) Interface
  - Boundary-scan Capabilities According to the JTAG Standard
  - Extensive On-chip Debug Support
  - Programming of Flash, EEPROM, Fuses, and Lock Bits through the JTAG Interface
- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescaler and Compare Mode
  - One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Six PWM Channels
  - 8-channel 10-bit ADC
    - Differential Mode with Selectable Gain at 1×, 10× or 200×
  - One Byte-oriented 2-wire Serial Interface (Philips I^2C compatible)
  - Two Programmable Serial USART
  - One Master/Slave SPI Serial Interface
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
  - Interrupt and Wake-up on Pin Change
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated RC Oscillator
  - External and Internal Interrupt Sources
  - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby, and Extended Standby
- I/O and Packages
  - 32 Programmable I/O Lines
  - 40-pin PDIP
  - 44-lead TQFP
  - 44-pad VQFN/QFN
  - 44-pad DRQFN
  - 49-ball VFBGA
- Operating Voltage:
  - 1.8 - 5.5V
- Speed Grades
  - 0 - 4MHz @ 1.8V - 5.5V
  - 0 - 10MHz @ 2.7V - 5.5V
  - 0 - 20MHz @ 4.5 - 5.5V
- Power Consumption at 1MHz, 1.8V, 25°C
  - Active Mode: 0.4mA
  - Power-down Mode: 0.1µA
  - Power-save Mode: 0.6µA (Including 32kHz RTC)

Note:

1. Refer to *Data Retention*

Related Links

Data Retention on page 15

1. Description

The Atmel® ATmega324PA is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega324PA achieves throughputs close to 1MIPS per MHz. This empowers system designer to optimize the device for power consumption versus processing speed.

The Atmel AVR® core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in a single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega324PA provides the following features: 32Kbytes of In-System Programmable Flash with Read-While-Write capabilities, 1Kbytes EEPROM, 2Kbytes SRAM, 32 general purpose I/O lines, 32 general purpose working registers, Real Time Counter (RTC), three flexible Timer/Counters with compare modes and PWM, two serial programmable USARTs , one byte-oriented 2-wire Serial Interface (I2C), a 8-channel 10-bit ADC with optional differential input stage with programmable gain, a programmable Watchdog Timer with internal Oscillator, an SPI serial port, IEEE std. 1149.1 compliant JTAG test interface, also used for accessing the On-chip Debug system and programming and six software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or hardware reset. In Power-save mode, the asynchronous timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except asynchronous timer and ADC to minimize switching noise during ADC conversions. In Standby mode, the crystal/resonator oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low power consumption. In Extended Standby mode, both the main oscillator and the asynchronous timer continue to run.

Atmel offers the QTouch® library for embedding capacitive touch buttons, sliders and wheels functionality into AVR microcontrollers. The patented charge-transfer signal acquisition offers robust sensing and includes fully debounced reporting of touch keys and includes Adjacent Key Suppression® (AKS™) technology for unambiguous detection of key events. The easy-to-use QTouch Suite toolchain allows you to explore, develop and debug your own touch applications.

The device is manufactured using Atmel's high density non-volatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed In-System through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an On-chip Boot program running on the AVR core. The Boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega324PA is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATmega324PA is supported with a full suite of program and system development tools including: C Compilers, Macro Assemblers, Program Debugger/Simulators, In-Circuit Emulators, and Evaluation kits.

2. Configuration Summary

The table below compares the device series of feature and pin compatible devices, providing a seamless migration path.

Table 2-1. Configuration Summary and Device Comparison

Features	ATmega164PA	ATmega324PA	ATmega644PA	ATmega1284P
Pin Count	40/44/49	40/44/49	40/44	40/44
Flash (Bytes)	16K	32K	64K	128K
SRAM (Bytes)	1K	2K	4K	16K
EEPROM (Bytes)	512	1K	2K	4K
General Purpose I/O Lines	32	32	32	32
SPI	1	1	1	1
TWI (I^2C)	1	1	1	1
USART	2	2	2	2
ADC	10-bit 15ksps	10-bit 15ksps	10-bit 15ksps	10-bit 15ksps
ADC Channels	8	8	8	8
Analog Comparator	1	1	1	1
8-bit Timer/ Counters	2	2	2	2
16-bit Timer/ Counters	1	1	1	2
PWM channels	6	6	6	8
Packages	PDIP TQFP VQFN/QFN DRQFN VFBGA	PDIP TQFP VQFN/QFN DRQFN VFBGA	PDIP TQFP VQFN/QFN	PDIP TQFP VQFNQFN

3. Ordering Information

Speed [MHz][3]	Power Supply [V]	Ordering Code[2]	Package[1]	Operational Range
20	1.8 - 5.5	ATmega324PA-AU	44A	Industrial (-40°C to 85°C)
		ATmega324PA-AUR[5]	44A	
		ATmega324PA-PU	40P6	
		ATmega324PA-MU	44M1	
		ATmega324PA-MUR[5]	44M1	
		ATmega324PA-MCH[4]	44MC	
		ATmega324PA-MCHR[4][5]	44MC	
		ATmega324PA-CU	49C2	
		ATmega324PA-CUR[5]	49C2	
20	1.8 - 5.5	ATmega324PA-AN	44A	Industrial (-40°C to 105°C)
		ATmega324PA-ANR[5]	44A	
		ATmega324PA-PN	40P6	
		ATmega324PA-MN	44M1	
		ATmega324PA-MNR[5]	44M1	

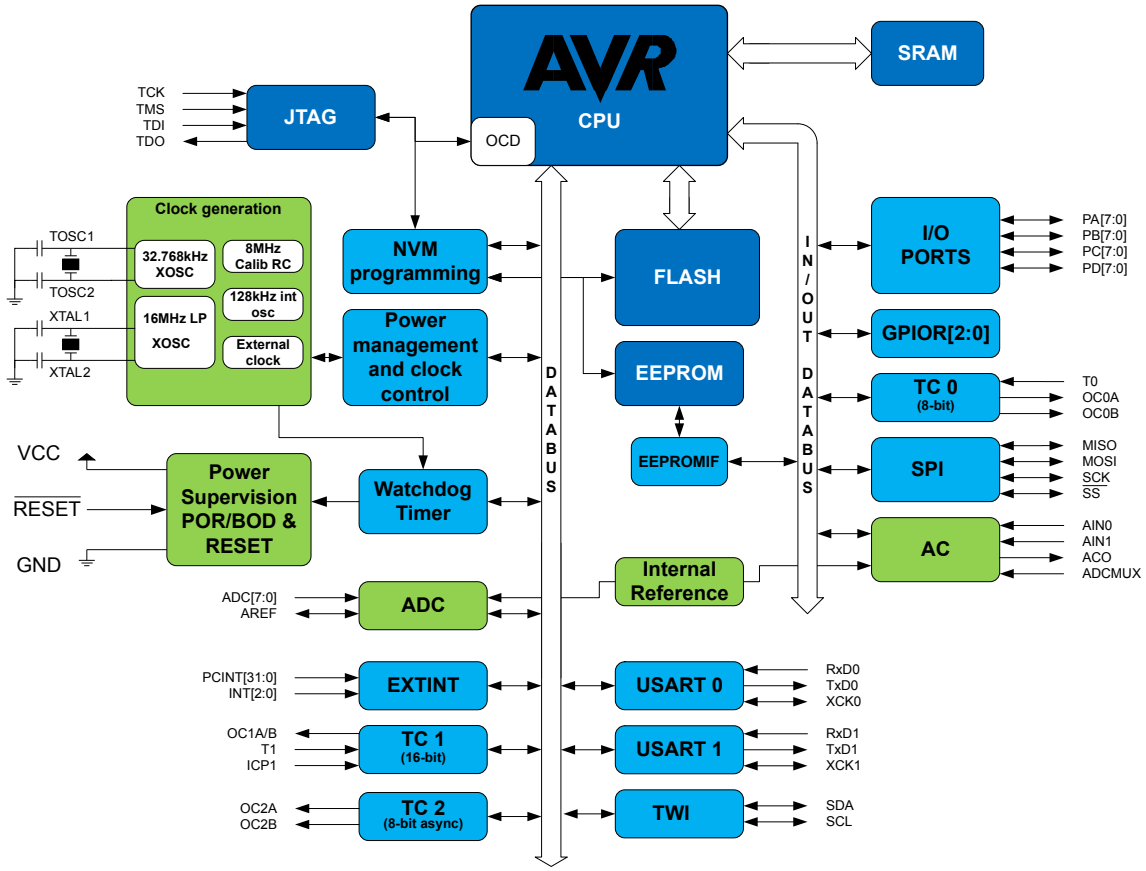
Note:

1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. Refer to *Speed Grades* for Speed vs. V_{CC}
4. NiPdAu Lead Finish.
5. Tape & Reel.

Package Type	
40P6	40-pin, 0.600” Wide, Plastic Dual Inline Package (PDIP)
44A	44-lead, Thin (1.0mm) Plastic Quad Flat Package (TQFP)
44M1	44-pad, 7 × 7 × 1.0mm body, lead pitch 0.50mm, Thermally Enhanced Plastic Very Thin Quad Flat No-Lead (VQFN)
44MC	44-lead (2-row Staggered), 5 × 5 × 1.0mm body, 2.60 × 2.60mm Exposed Pad, Quad Flat No-Lead Package (QFN)
49C2	49-ball, (7 × 7 Array) 0.65mm Pitch, 5 × 5 × 1mm, Very Thin, Fine-Pitch Ball Grid Array Package (VFBGA)

4. Block Diagram

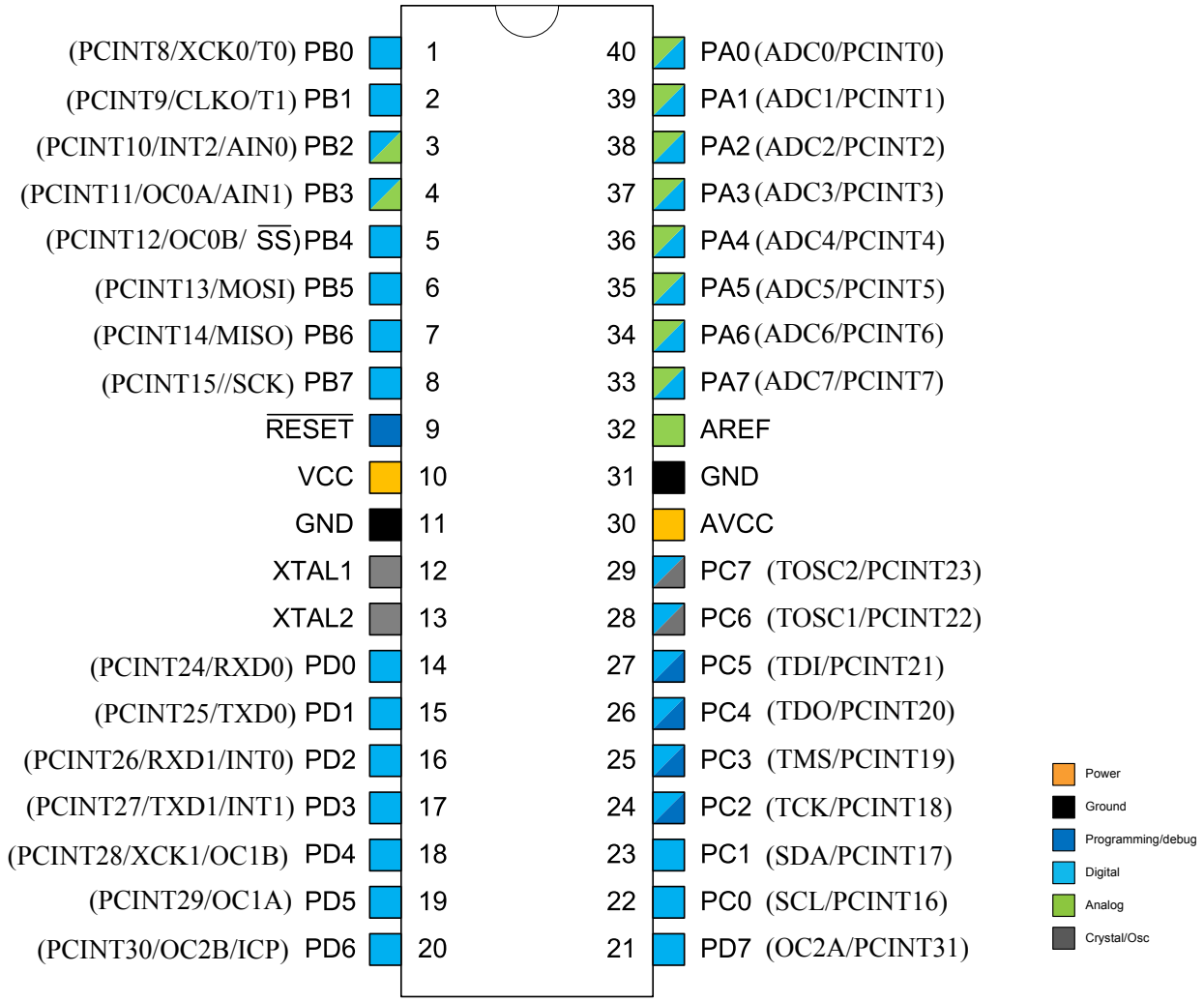
Figure 4-1. Block Diagram



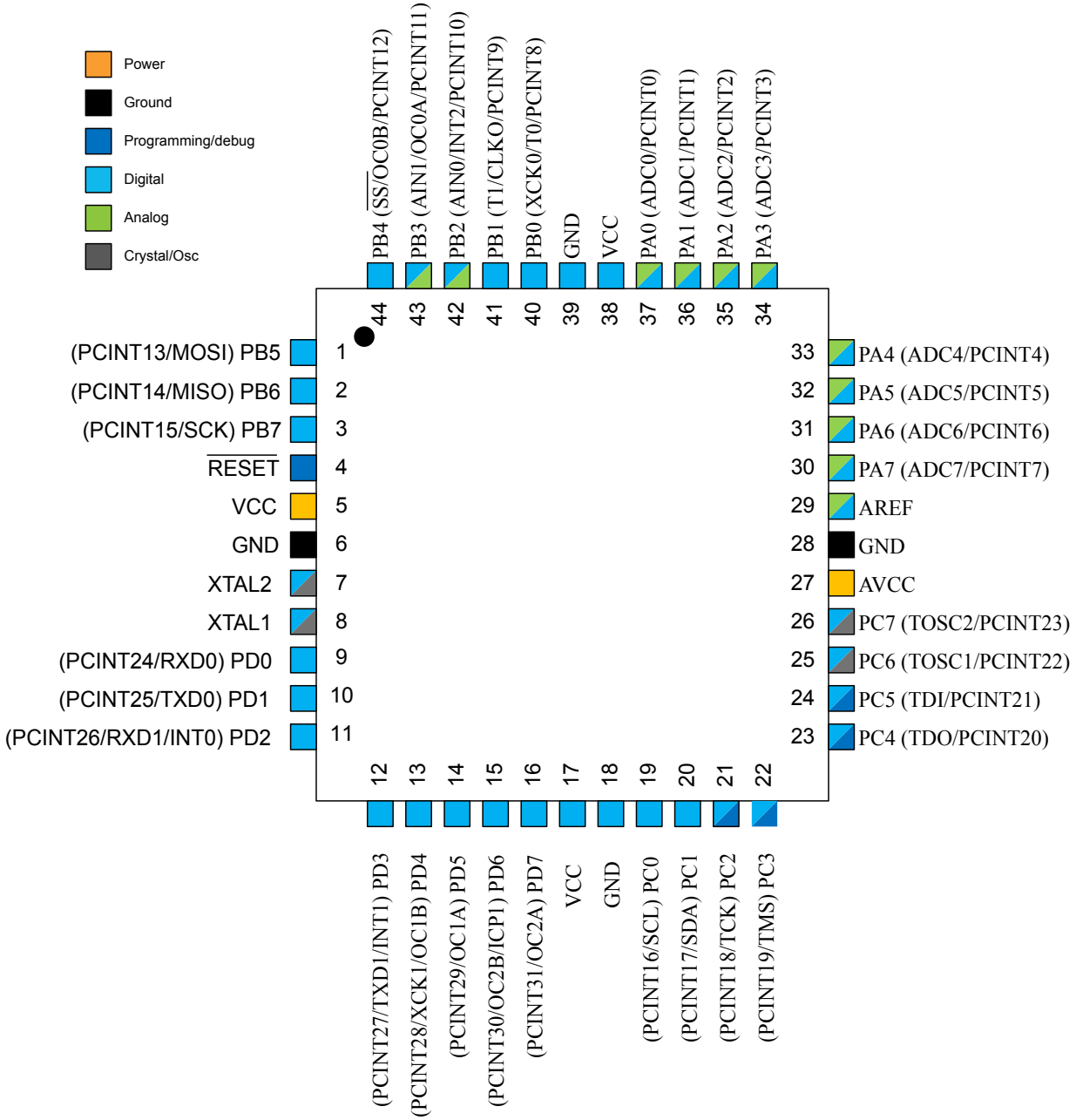
5. Pin Configurations

5.1. Pinout

5.1.1. PDIP

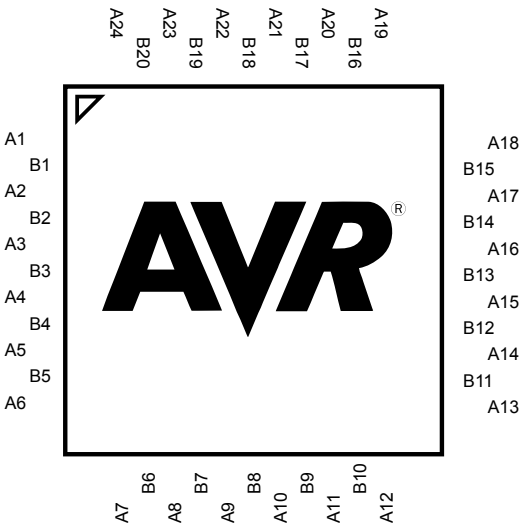


5.1.2. TQFN and QFN



5.1.3. DRQFN

Top view



Bottom view

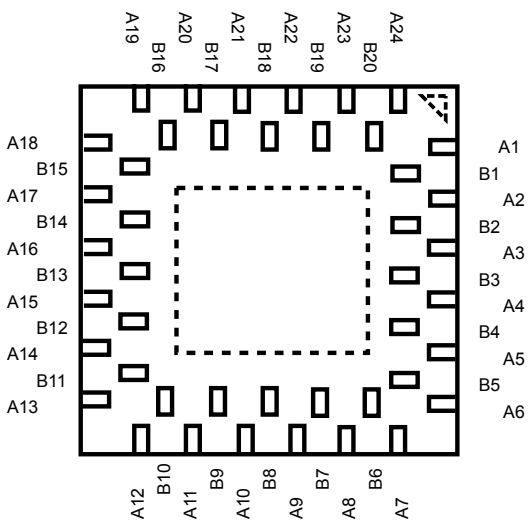
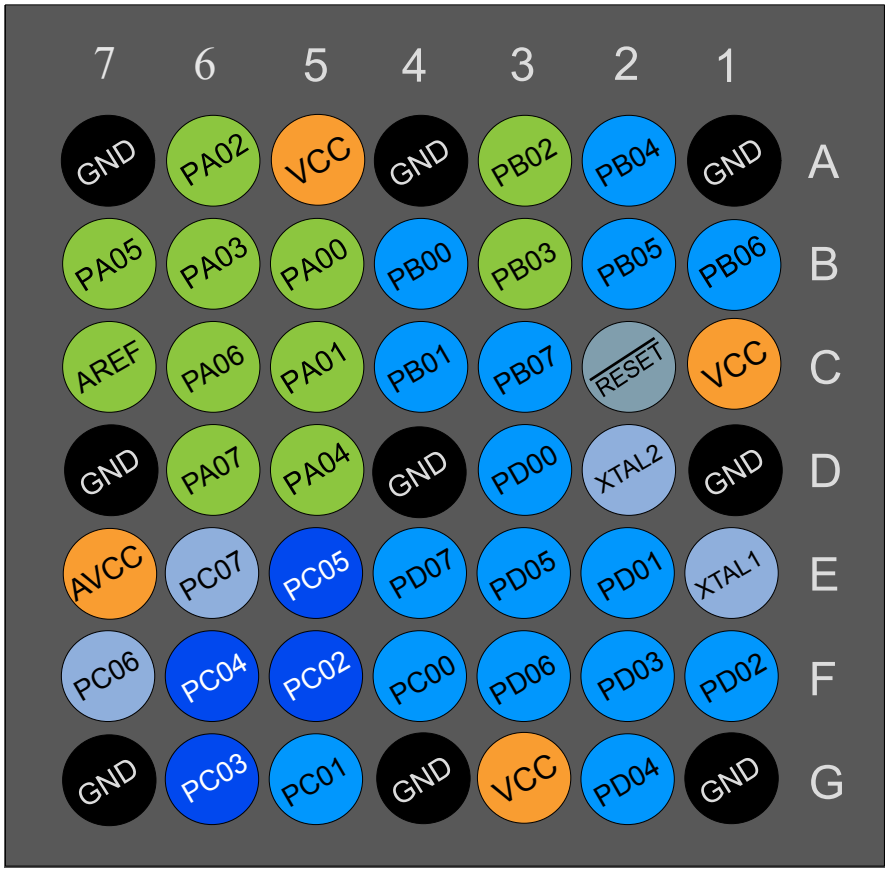


Table 5-1. DRQFN Pinout

A1	PB5	A7	PD3	A13	PC4	A19	PA3
B1	PB6	B6	PD4	B11	PC5	B16	PA2
A2	PB7	A8	PD5	A14	PC6	A20	PA1
B2	$\overline{\text{RESET}}$	B7	PD6	B12	PC7	B17	PA0
A3	VCC	A9	PD7	A15	AVCC	A21	VCC
B3	GND	B8	VCC	B13	GND	B18	GND
A4	XTAL2	A10	GND	A16	AREF	A22	PB0
B4	XTAL1	B9	PC0	B14	PA7	B19	PB1
A5	PD0	A11	PC1	A17	PA6	A23	PB2
B5	PD1	B10	PC2	B15	PA5	B20	PB3
A6	PD2	A12	PC3	A18	PA4	A24	PB4

5.1.4. VFBGA



5.2. Pin Descriptions

5.2.1. VCC

Digital supply voltage.

5.2.2. GND

Ground.

5.2.3. Port A (PA[7:0])

This port serves as analog inputs to the Analog-to-digital Converter.

This is an 8-bit, bi-directional I/O port with internal pull-up resistors, individually selectable for each bit. The output buffers have symmetrical drive characteristics, with both high sink and source capability. As inputs, the port pins that are externally pulled low will source current if pull-up resistors are activated. Port pins are tri-stated when a reset condition becomes active, even if the clock is not running.

5.2.4. Port B (PB[7:0])

This is an 8-bit, bi-directional I/O port with internal pull-up resistors, individually selectable for each bit. The output buffers have symmetrical drive characteristics, with both high sink and source capability. As inputs, the port pins that are externally pulled low will source current if pull-up resistors are activated. Port pins are tri-stated when a reset condition becomes active, even if the clock is not running.

This port also serves the functions of various special features.

5.2.5. Port C (PC[7:0])

This is an 8-bit, bi-directional I/O port with internal pull-up resistors, individually selectable for each bit. The output buffers have symmetrical drive characteristics, with both high sink and source capability. As inputs, the port pins that are externally pulled low will source current if pull-up resistors are activated. Port pins are tri-stated when a reset condition becomes active, even if the clock is not running.

This port also serves the functions of the JTAG interface, along with special features.

5.2.6. Port D (PD[7:0])

This is an 8-bit, bi-directional I/O port with internal pull-up resistors, individually selectable for each bit. The output buffers have symmetrical drive characteristics, with both high sink and source capability. As inputs, the port pins that are externally pulled low will source current if pull-up resistors are activated. Port pins are tri-stated when a reset condition becomes active, even if the clock is not running.

This port also serves the functions of various special features.

5.2.7. $\overline{\text{RESET}}$

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. Shorter pulses are not guaranteed to generate a reset.

5.2.8. XTAL1

Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

5.2.9. XTAL2

Output from the inverting Oscillator amplifier.

5.2.10. AVCC

AVCC is the supply voltage pin for Port A and the Analog-to-digital Converter. It should be externally connected to V_{CC}, even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter.

5.2.11. AREF

This is the analog reference pin for the Analog-to-digital Converter.

6. I/O Multiplexing

Each pin is by default controlled by the PORT as a general purpose I/O and alternatively it can be assigned to one of the peripheral functions.

The following table describes the peripheral signals multiplexed to the PORT I/O pins.

Table 6-1. PORT Function Multiplexing

32-pin TQFP/ QFN/ MLF Pin #	40-pin PIPD Pin #	DRQFN Pin#	VFBGA Pin#	PAD	EXTINT	PCINT	ADC/AC	OSC	T/C # 0	T/C # 1	USART	I2C	SPI	JTAG
1	6	A1	B2	PB[5]		PCINT13							MOSI	
2	7	B1	B1	PB[6]		PCINT14							MISO	
3	8	A2	C3	PB[7]		PCINT15							SCK	
4	9	B2	C2	$\overline{\text{RESET}}$										
5	10	A3	A5	VCC										
6	11	B3	A1	GND										
7	12	A4	D2	XTAL2										
8	13	B4	E1	XTAL1										
9	14	A5	D3	PD[0]		PCINT24					RxD0			
10	15	B5	E2	PD[1]		PCINT25					TxD0			
11	16	A6	F1	PD[2]	INT0	PCINT26					RxD1			
12	17	A7	F2	PD[3]	INT1	PCINT27					TXD1			
13	18	B6	G2	PD[4]		PCINT28				OC1B	XCK1			
14	19	A8	E3	PD[5]		PCINT29				OC1A				
15	20	B7	F3	PD[6]		PCINT30			OC2B	ICP1				
16	21	A9	E4	PD[7]		PCINT31			OC2A					
17	-	B8	C1	VCC							RxD2		MISO1	
18	-	A10	A4	GND							TxD2		MOSI1	
19	22	B9	F4	PC[0]		PCINT16						SCL		
20	23	A11	G5	PC[1]		PCINT17						SDA		
21	24	B10	F5	PC[2]		PCINT18								TCK
22	25	A12	G6	PC[3]		PCINT19								TMS
23	26	A13	F6	PC[4]		PCINT20								TDO

32-pin TQFP/ QFN/ MLF Pin #	40-pin PIPD Pin #	DRQFN Pin#	VFBGA Pin#	PAD	EXTINT	PCINT	ADC/AC	OSC	T/C # 0	T/C # 1	USART	I2C	SPI	JTAG
24	27	B11	E5	PC[5]		PCINT21								TDI
25	28	A14	F7	PC[6]		PCINT22		TOSC1						
26	29	B12	E6	PC[7]		PCINT23		TOSC2						
27	30	A15	E7	AVCC										
28	31	B13	D1	GND										
29	32	A16	C7	AREF			AREF							
30	33	B14	D6	PA[7]		PCINT7	ADC7							
31	34	A17	C6	PA[6]		PCINT6	ADC6							
32	35	B15	B7	PA[5]		PCINT5	ADC5							
33	36	A18	D5	PA[4]		PCINT4	ADC4							
34	37	A19	B6	PA[3]		PCINT3	ADC3							
35	38	B16	A6	PA[2]		PCINT2	ADC2							
36	39	A20	C5	PA[1]		PCINT1	ADC1							
37	40	B17	B5	PA[0]		PCINT0	ADC0							
38	-	A21	G3	VCC								SDA1		
39	-	B18	A7	GND								SCL1		
40	1	A22	B4	PB[0]		PCINT8			T0		XCK0			
41	2	B19	C4	PB[1]		PCINT9		CLKO		T1				
42	3	A23	A3	PB[2]	INT2	PCINT10	AIN0							
43	4	B20	B3	PB[3]		PCINT11	AIN1		OC0A					
44	5	A24	A2	PB[4]		PCINT12			OC0B				$\overline{SS}$	
-	-	-	D4	GND										
-	-	-	D7	GND										
-	-	-	G1	GND										
-	-	-	G4	GND										
-	-	-	G7	GND										

7. General Information

7.1. Resources

A comprehensive set of development tools, application notes, and datasheets are available for download on http://www.atmel.com/avr.

7.2. Data Retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

7.3. About Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Confirm with the C compiler documentation for more details.

For I/O Registers located in extended I/O map, “IN”, “OUT”, “SBIS”, “SBIC”, “CBI”, and “SBI” instructions must be replaced with instructions that allow access to extended I/O. Typically “LDS” and “STS” combined with “SBRS”, “SBRC”, “SBR”, and “CBR”.

7.4. Capacitive Touch Sensing

7.4.1. QTouch Library

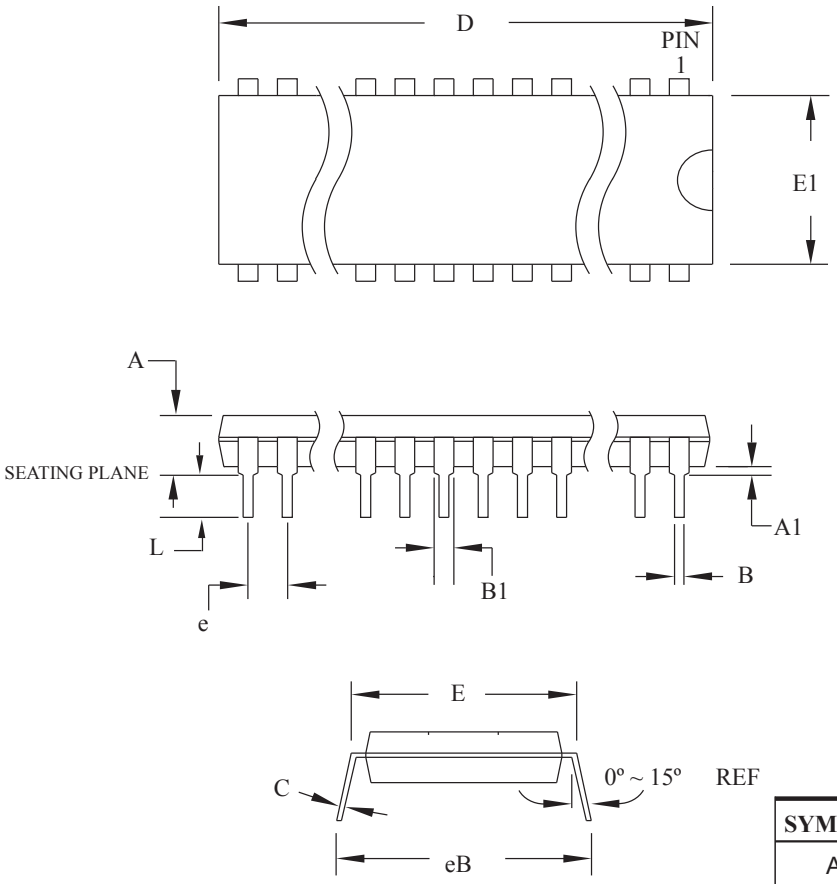
The Atmel® QTouch® Library provides a simple to use solution to realize touch sensitive interfaces on most Atmel AVR® microcontrollers. The QTouch Library includes support for the Atmel QTouch and Atmel QMatrix® acquisition methods.

Touch sensing can be added to any application by linking the appropriate Atmel QTouch Library for the AVR Microcontroller. This is done by using a simple set of APIs to define the touch channels and sensors, and then calling the touch sensing API’s to retrieve the channel information and determine the touch sensor states.

The QTouch Library is FREE and downloadable from the Atmel website at the following location: http://www.atmel.com/technologies/touch/. For implementation details and other information, refer to the Atmel QTouch Library User Guide - also available for download from the Atmel website.

8. Packaging Information

8.1. 40-pin PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

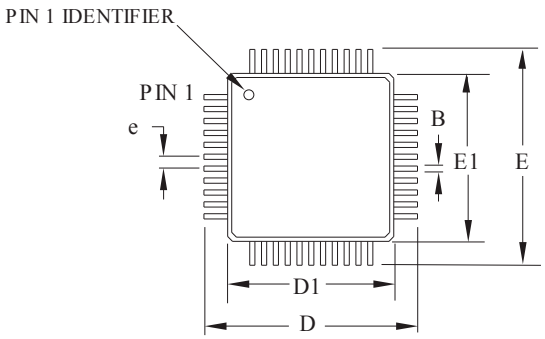
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–	–	
D	52.070	–	52.578	Note 2
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 2
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

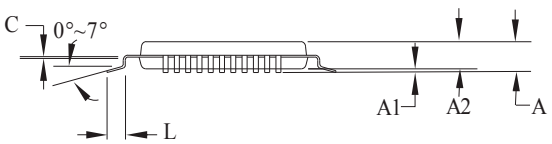
Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25mm (0.010").

13/02/2014

Package Drawing Contact: packagedrawings@atmel.com	TITLE	DRAWING NO.	REV.
	40P6, 40-lead (0.600"/15.24mm Wide) Plastic Dual Inline Package (PDIP)	40P6	C

8.2. 44-pin TQFP





COMMON DIMENSIONS
(Unit of Measure = mm)

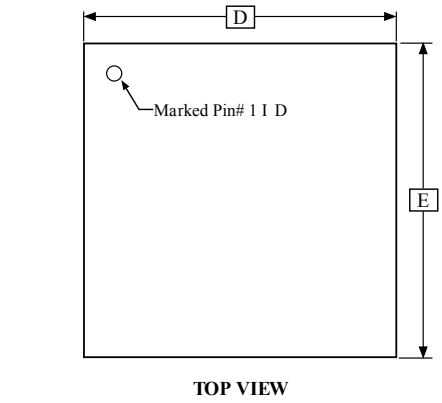
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	0.37	0.45	
C	0.09	(0.17)	0.20	
L	0.45	0.60	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

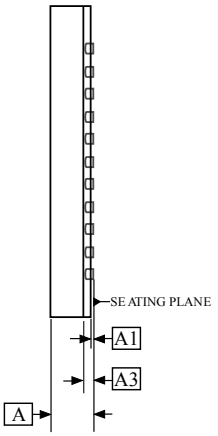
06/02/2014

	TITLE	DRAWING NO.	REV.
Atmel Package Drawing Contact: packagedrawings@atmel.com	**44A,** 44-lead, 10 x 10mm body size, 1.0mm body thickness, 0.8 mm lead pitch, thin profile plastic quad flat package (TQFP)	44A	C

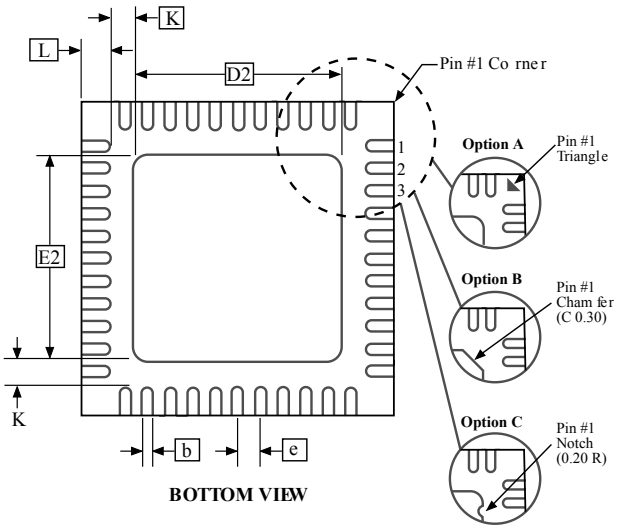
8.3. 44-pin VQFN



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Note : JEDEC Standard MO-220, Fig . 1 (S AW Singulation) VKKD-3 .

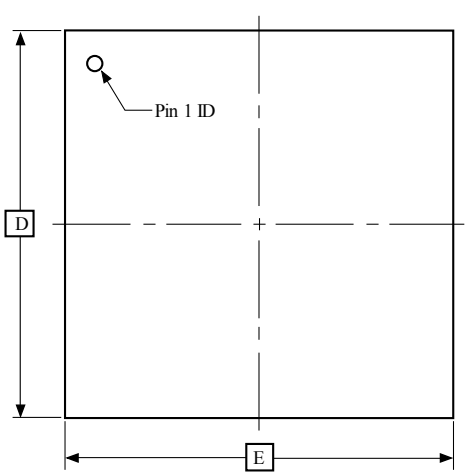
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	–	0.02	0.05	
A3		0.20 REF		
b	0.18	0.23	0.30	
D	6.90	7.00	7.10	
D2	5.00	5.20	5.40	
E	6.90	7.00	7.10	
E2	5.00	5.20	5.40	
e		0.50 BSC		
L	0.59	0.64	0.69	
K	0.20	0.26	0.41	

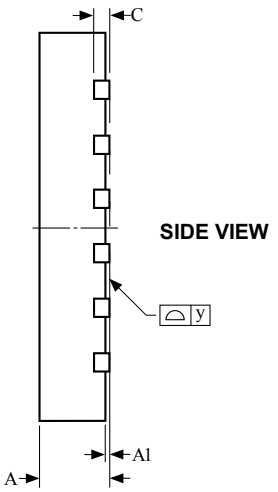
9/26/08

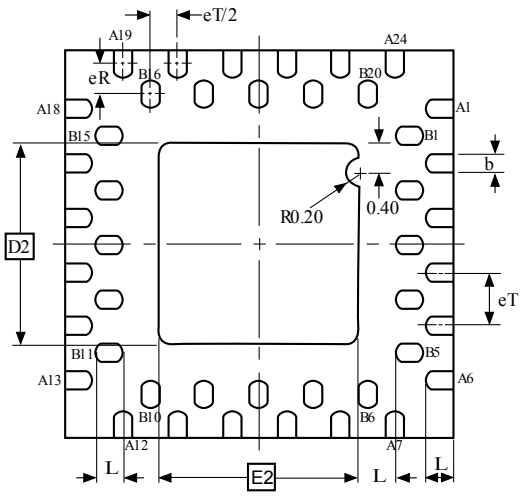
Package Drawing Contact: avr@atmel.com	TITLE	GPC	DRAWING NO.	REV.
	44M1, 44-pad, 7 x 7 x 1.0mm body, lead pitch 0.50mm, 5.20mm exposed pad, thermally enhanced plastic very thin quad flat no lead package (VQFN)	ZWS	44M1	H

8.4. 44-pin QFN



TOP VIEW





BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

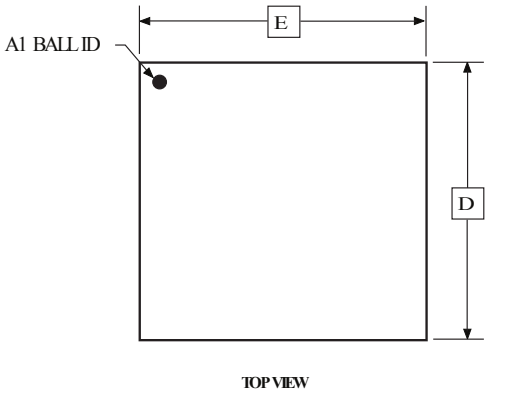
SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	
b	0.18	0.23	0.30	
C		0.20 REF		
D	4.90	5.00	5.10	
D2	2.55	2.60	2.65	
E	4.90	5.00	5.10	
E2	2.55	2.60	2.65	
eT	–	0.70	–	
eR	–	0.40	–	
K	0.45	–	–	
L	0.30	0.35	0.40	
y	0.00	–	0.075	

Note: 1. The terminal #1 ID is a Laser-marked Feature.

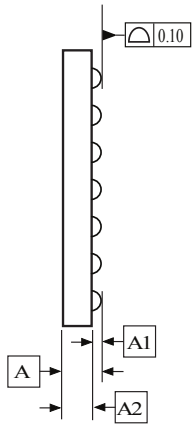
9/13/07

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE: 44MC, 44QFN (2-Row Staggered), 5 x 5 x 1.00mm Body, 2.60 x 2.60mm Exposed Pad, Quad Flat No Lead Package	DRAWING NO.: 44MC	REV.: A

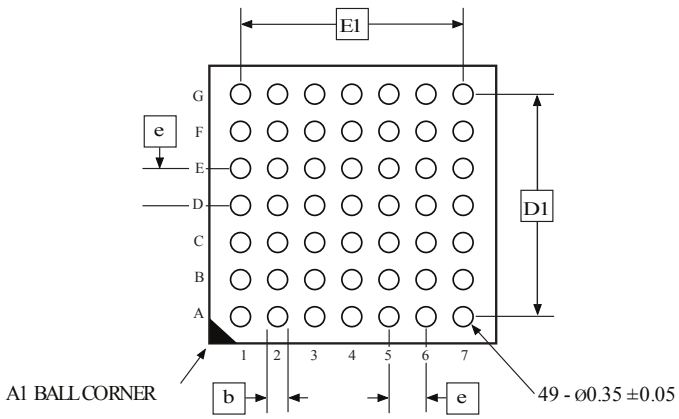
8.5. 49-pin VFBGA



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.00	
A1	0.20	–	–	
A2	0.65	–	–	
D	4.90	5.00	5.10	
D1		3.90 BSC		
E4.90	5.00	5.10		
E1		3.90 BSC		
b	0.30	0.35	0.40	
e		0.65 BSC		

3/14/08

Atmel **Package Drawing Contact:** packagedrawings@atmel.com	**TITLE** **49C2,** 49-ball (7 x 7 array), 0.65mm pitch, 5.0 x 5.0 x 1.0mm, very thin, fine-pitch ball grid array package (VFBGA)	**GPC** CBD	**DRAWING NO.** 49C2	**REV.** A

Atmel | Enabling Unlimited Possibilities®

Atmel Corporation 1600 Technology Drive, San Jose, CA 95110 USA **T:** (+1)(408) 441.0311 **F:** (+1)(408) 436.4200 | **www.atmel.com**