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Recommended Usage of Microchip I²C EERAM Devices

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INTRODUCTION

EERAM is a nonvolatile memory consisting of an SRAM with matching EEPROM as backup. Its design allows for data to be written to it quickly and as often as desired, and to be safely preserved if there is an unexpected loss of power. It can then make the data available again after power is restored.

This application note expands beyond what is found in the data sheet (DS20005371) and provides techniques to enable a more robust application which utilizes EERAM devices.

MODES OF OPERATION

The SRAM allows for fast reads and writes and unlimited endurance. As long as power is present, the data stored in the SRAM can be updated as often as desired.

To preserve the SRAM image, the AutoStore function copies the entire SRAM image to an EEPROM array whenever it detects that the voltage drops below a predetermined level. The power for the AutoStore process is provided by the externally connected VCAP capacitor.

Upon power-up, the entire memory contents are restored by copying the EEPROM image to the SRAM. This automatic restore operation is completed in milliseconds after power-up, at the same time as when other devices would be initializing.

There is no latency in writing to the SRAM. The SRAM can be written to starting at any random address, and can be written continuously throughout the array, wrapping back to the beginning after the end is reached. There is a small delay, specified as TWC in the data sheet, when writing to the nonvolatile configuration bits of the STATUS Register (SR).

Besides the AutoStore function, there are two other methods to store the SRAM data to EEPROM:

- One method is the Hardware Store, initiated by a rising edge on the HS pin.
- The other method is the Software Store, initiated by writing the correct instruction to the COMMAND register via I²C.

For users who wish to use the manual store methods only, the device can be configured for use without a VCAP capacitor. In this case, the AutoStore feature should be disabled by clearing the ASE bit in the STATUS Register and the VCAP pin should be connected to VCC.

If the AutoStore operation is disabled, then the device will not automatically backup the SRAM data. Therefore, upon power loss, any data written to the SRAM since the previous store operation may be lost. As such, the application must initiate store operations often enough to minimize the loss of data, but not so often as to exceed the EEPROM's endurance.

PCB LAYOUT CONSIDERATIONS

The EERAM device should have a bypass capacitor at the VCC pin, just like any CMOS integrated circuit. A good value is 0.1 µF from VCC to VSS, placed close to the device.

Layout for VCAP connections is less critical, but should allow for the capacitor to be mounted nearby the IC with the traces as short as possible, preferably within an inch or two away. The VCAP line should not be tapped off or shared with any other circuit. The VCAP capacitor should never be replaced with a battery.

The current required to initially charge the VCAP capacitor upon power-up can be significantly larger than normal operation current (peak VCAP charge current can reach or exceed 50 mA), so the ground connection of the EERAM and the VCAP capacitor negative side should be at a low-impedance to the system ground, preferably connecting each to a ground plane, in order to prevent voltage drops that might be mistaken for logic-level signals.

The I²C lines, SDA and SCL, should be routed away from noise sources to prevent disturbing the bus.

CHIP ADDRESS INPUTS

To allow the simultaneous connections to up to four EERAM devices on the same I²C bus, address pins A1 and A2 are provided. These pins can be connected to VCC or VSS. The logic level corresponds to the address bits in the control byte. If left unconnected, they default to logic low through a weak internal pull-down, but where external noise is likely, it is still recommended to deliberately tie these pins to VCC or VSS to increase their noise immunity.

BUS PULL-UP RESISTORS

The I^2C signals, SDA and SCL, should be connected to the bus with pull-up resistors of an appropriate value related to the top speed of the bus. Up to a bus speed of 400 kHz, 10 kΩ pull-ups are recommended. For the maximum speed of 1 MHz bit rate, pull-ups of 2 kΩ are recommended. Refer to the I^2C Interfacing section of the data sheet for more details.

HARDWARE STORE PIN

The HS pin is provided to allow detection of external events and for the hardware initiation of a Store. When a rising edge on the HS pin is detected (if the SRAM array has been modified, as indicated by the AM bit being high in the STATUS Register), then a Hardware Store will be initiated. Also, the nonvolatile Event bit in the STATUS Register will be set. If the SRAM array is not modified, thus the AM bit is not set, the rising edge on the HS pin will still initiate the writing of the Event bit in the STATUS Register. Since the Event bit is non-volatile, it can be checked later to see if it was triggered, so it can be useful for storing an external event. The Event bit is cleared in software by a write to the STATUS Register.

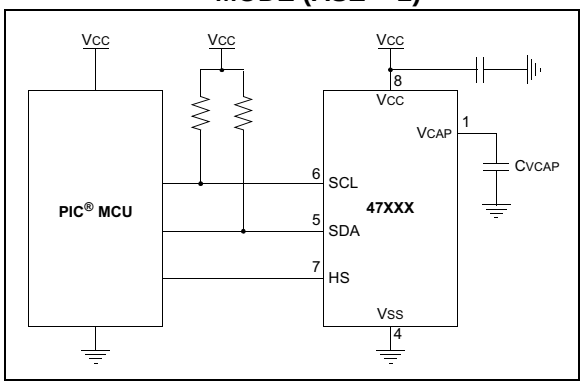
UTILIZING AutoStore

A capacitor on the VCAP pin and ground provides power for AutoStore operation. The capacitor is charged by the EERAM device from the VCC pin.

The data sheet provides a list of required minimum capacitance to use. Capacitor tolerance can vary, so always choose a capacitor that meets the minimum capacitance requirements even at the low end of its tolerance range.

When using the VCAP capacitor, the AutoStore Enable (ASE) bit must be set in the STATUS Register to allow the store to happen on power-down. For details, see the **"STATUS Register"** section.

FIGURE 1: TYPICAL APPLICATION SCHEMATIC AutoStore MODE (ASE = 1)



AVOIDING USE OF EXTERNAL CAPACITOR

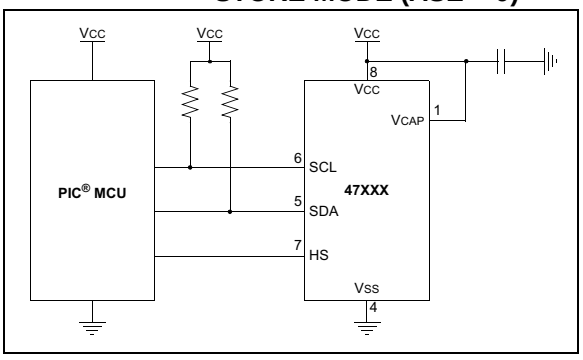
If it is desired to avoid using an external capacitor, the VCAP pin must be connected to the VCC pin. A bypass capacitor is still recommended on VCC. To prevent the AutoStore feature from being activated on power-down (which could result in data corruption), the ASE bit in the STATUS Register must be cleared to '0'.

A Store can still be performed by using the Hardware Store (HS) pin, or by issuing a Software Store command by writing to the COMMAND register.

Using manual stores only does allow for the chance of data corruption if there is a power loss during a manual store. The store operation must first erase the EEPROM array before writing the SRAM image, so a power loss during this operation may result in some or all of the data to be lost.

When utilizing manual store methods, one must remember the trade-offs between how often the data is backed up, with the endurance of the EEPROM. The EEPROM array in the EERAM is similar to that of a regular EEPROM. Updating the SRAM data often is still available, but deciding on how often the image is backed up to EEPROM is no longer automatic, so the scheduling should not be so often so as to exceed the maximum specified Store cycles before the expected lifespan of the application.

FIGURE 2: TYPICAL APPLICATION SCHEMATIC MANUAL STORE MODE (ASE = 0)



WRITE-PROTECT FEATURE

The EERAM devices include a write-protect feature, whereby some portion of the array can be protected from being modified by the user. Memory regions ranging from the upper 1/64th, to larger fractions up to the entire memory, can be protected. The three Block Protect bits are set in the STATUS Register.

This protection applies as write attempts are made to the SRAM and can be detected by a NACK returned when any byte write is attempted in the protected region. The NACK is returned after the data bytes are clocked in, not after the address bytes.

Protected data regions of the SRAM are still written to the backup EEPROM by store operations to ensure data remains synchronized. This means that if a VCAP capacitor is not used, a store operation that is interrupted by a power loss can result in corrupted data, even for protected regions.

POWER SUPPLY

The VCC voltage range is listed in the data sheet for nominal 3.3V or 5V operation. Note that the rise and fall rates of VCC are critical with this device and must be observed to ensure proper operation of the AutoStore and Recall functions. Per the data sheet specifications, very fast fall and rise rates should be avoided and slower rates are acceptable; the rise should be monotonic to avoid unnecessary Store or Recall events. Power supplied to the EERAM device is expected to be clean DC with a low ripple component and without sagging caused by other loads. This is important due to the fact that the EERAM is constantly monitoring the VCC voltage to know when to begin an AutoStore operation. If even a brief excursion in the VCC falls below the VTRIP level, it may cause AutoStore operations to begin, blocking I^2C communication for the store time. So, it is recommended that the power supply be stable, that Switch Mode Power Supplies (SMPS) be filtered to keep ripple at a minimum, and preferably set in the mid to upper regions of the VCC recommended operating range to prevent accidentally tripping the AutoStore function.

The fact that the EERAM is sensitive to voltage variations is not unique, as many devices carry brown-out detection circuits. What should be noted, however, is that the levels at which this happens may be different between devices, so it is possible that the EERAM will detect a dip before or after the host microcontroller does, or at a different time than another I^2C device does. In any of these cases, there could be problems with the I^2C bus experiencing errors, so the microcontroller should be prepared to deal with it, such as performing a software Reset of the bus when it sees the bus not responding as expected.

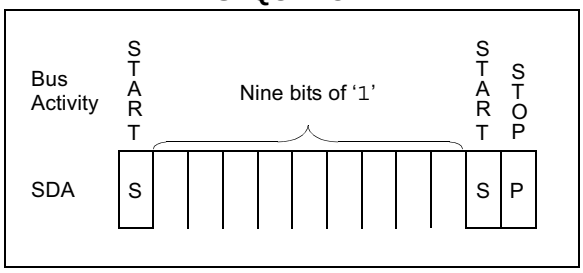
SOFTWARE RESET SEQUENCE

At times it may become necessary to perform a software Reset sequence to ensure the serial EERAM is in a correct and known state. This could be useful, for example, if there are conflicts on the I^2C bus, or if the EERAM has entered into an unknown state (due to excessive bus noise, or power supply fluctuations, etc.) or if the microcontroller is reset during communication.

The following sequence can be sent in order to ensure that the serial EERAM device is properly reset (Figure 3):

- Start bit
- Clock in nine bits of '1'
- Start bit
- Stop bit

FIGURE 3: SOFTWARE RESET SEQUENCE



The first Start bit will cause the device to reset from a state in which it is expecting to receive data from the microcontroller. In this mode, the device is monitoring the data bus in Receive mode and can detect the Start bit, which forces an internal Reset. The nine bits of '1' are used to force a Reset of those devices that could not be reset by the previous Start bit. This occurs only if the device is in a mode where it is either driving an Acknowledge on the bus (low) or is in an Output mode and is driving a data bit of '0' out on the bus. In both of these cases, the previous Start bit (defined as SDA going low while SCL is high) could not be generated due to the device holding the bus low. By sending nine bits of '1', it is ensured that the device will see a NACK (i.e., the microcontroller does not drive the bus low to Acknowledge data sent by the EERAM), which also forces an internal Reset.

DETECTING I²C COMMUNICATION ERRORS

One of the many benefits of I²C communication is the Acknowledge bit transmitted after every byte is received. Except during Store, Recall and STATUS write cycles, the EERAM will always transmit this bit low after receiving each byte, assuming a valid Start bit and control byte were already received, unless attempting to write to a protected region of the memory array. Due to this, the master can monitor the ACK bit received throughout an operation to detect any errors that may occur. It is always good practice to check if a logic '1' is received for the ACK during transmission, which would indicate that the EERAM did not respond. At that point, an error handling routine would be required to determine why the device did not respond, and if necessary, to perform a software Reset sequence.

ACKNOWLEDGE POLLING

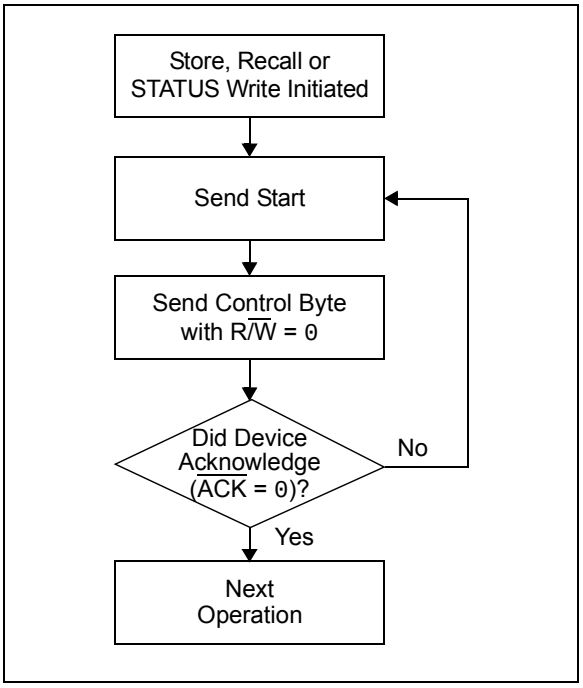
Write operations on serial EERAMs do not require that a write cycle time be observed for writing data, since the data is being written directly to SRAM. But, during writes to the nonvolatile STATUS Register, and during Store and Recall operations, the EERAM I²C communication is disabled, and any attempts by the master to access the device will be ignored.

Therefore, it is important that the master wait for any of these busy cycles to end before attempting to access the EERAM again.

Each device has a specified worst-case Store time, typically listed as TSTORE, and a STATUS write time, specified as TWC and a Recall time as TRECALL. A simple method for ensuring that the write, Store or Recall time is observed is to perform a delay for the amount of time specified before accessing the EERAM again. However, it is not uncommon for a device to complete these operations in less than the maximum specified time. As such, using the fixed delay method may result in waiting longer than necessary.

In order to eliminate this extra period of time and therefore, operate more efficiently, it is highly recommended to take advantage of the Acknowledge polling feature. Since Microchip's I²C serial EERAM devices will not Acknowledge during a Store, Recall or STATUS write cycle, the device can continuously be polled until an ACK bit is received, thus indicating that the operation is complete.

FIGURE 4: ACKNOWLEDGE POLLING FLOW



PROCEDURE

Once the Store, Recall or STATUS write operation is started, ACK polling can be initiated immediately. This involves the master sending a Start condition, followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the operation, then no ACK will be returned. If no ACK is returned, then the Start bit and control byte must be sent again. If the operation is complete, the device will return the ACK and the master can then proceed with the next read or write command. See Figure 4 for details.

SOFTWARE OPERATIONS

The EERAM has available two special registers to enable special features of the device, the STATUS Register and COMMAND register.

STATUS Register

The STATUS Register contains both volatile and nonvolatile bits, useful for controlling and detecting important behavior. Changing the settings to the STATUS Register is done by writing to the entire register and should be done as a Read-Modify-Write in order to preserve the settings of other bits.

The Block Protect bits (BP<2:0>) are used for protecting regions of memory, from 1/64 in fractions up to the entire array.

The ASE bit is used to enable the AutoStore function, which is normally set to '1' when a VCAP capacitor is used and set to '0' when one is not.

The AM bit is volatile and read-only, and it indicates when the array has been modified since the last Store or Recall operation by writing to the SRAM array. The AM bit will indicate if it is necessary for the Hardware Store and AutoStore operations to work. If the AM bit is '0', then the SRAM already is equal to the EEPROM data, so no AutoStore or Hardware Store is performed (the one exception is that Software Store can still be performed). Once a Store or Recall is performed by any source, the AM bit is cleared to '0'. The AM bit is set as soon as any data is written to the SRAM, even if the new data value matches the existing data in the SRAM and does not cause any delay in the SRAM writes.

Finally, the EVENT bit is set whenever the HS pin experiences a rising edge to a logic high. The EVENT bit is set even if the AM bit was '0' and no Hardware Store is actually executed. In this way, the Event bit can be used as an indication that an "event" happened on the HS pin, whether it involved a Store or not. So, this may be useful for detecting changes in a system where the microcontroller is asleep, when it may not need to immediately service the event, but does need to know that something has happened.

COMMAND Register

The other special register is the COMMAND register. The COMMAND register is where the Software Store and Software Recall instructions are initiated. The software commands can initiate Store and Recall functions independent of the state of the AM bit.

Because the I^2C bus must be operational in order to write to the COMMAND register, it is not possible to initiate a Store operation if VCC is below the VTRIP level. So, even though AutoStore operations can be initiated as they enter this region, manual Store operations cannot be initiated here. However, if the command is completed before the VCC passes below VTRIP, then the Store operation will continue as long as the voltage is available long enough to complete the operation (such as when a VCAP capacitor is present). It is not recommended to rely on the I^2C bus being available during a power fail, as was mentioned, different devices reacting at different brown-out levels could disrupt the entire bus.

In the event that the AM bit is equal to '1', indicating that the SRAM image has been written to since the last Recall or Store event, the SRAM may not match the EEPROM backup image. If a Software Recall instruction is given at this time, the SRAM image is overwritten with the backup image from the EEPROM, so any of the changes to the SRAM since the last Store will be lost.

As stated, the AM bit in the STATUS Register need not be equal to '1' in order for the Software Store operation to work through the COMMAND register, but when a Software Store is performed, the AM bit will be set '0'. The Software Store command should be used with care in order to prevent unnecessary writes to the EEPROM and its premature wear.

The COMMAND register will ignore any values which do not match the specified Software Store and Recall commands.

SUMMARY

This application note described the basic usage considerations of the Microchip EERAM devices. This also covered the PCB layout, bypassing and signal connections. Descriptions of the STATUS Register and Control register were given in some detail, and potential I^2C bus issues were described and preventative options offered. These recommendations fall in line with how Microchip designs, manufactures, qualifies and tests its serial EERAMs, and will allow the devices to operate within the data sheet specifications. It is suggested that the concepts detailed in this application note be incorporated into any system which utilizes an I^2C serial EERAM.

APPENDIX A: REVISION HISTORY

Revision A (01/2016)

Initial release of this document.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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